Summer Fellowship Report

On

Subciruits in eSim

Submitted by

Katakam V N Manikanta Bhargav

and

Padigepati Mallikarjuna Reddy

Under the guidance of

Prof.Kannan M. Moudgalya
Chemical Engineering Department
IIT Bombay

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Contents

Chapter 1

Introduction

eSim is a free and open source EDA tool. It is an acronym forElectronicsSimulation.eSim is created using open source software packages, such as KiCad, Ngspice and Python. Using eSim, one can create circuit schematics, perform simulations and designPCB layouts. It can create or edit new device models, and create or edit subcircuits for simulation.Because of these reasons, eSim is expected to be useful for students, teachers another professionals who would want to study and/or design electronic systems. eSim is also useful for entrepreneurs and small scale enterprises who do not have the capability to invest in heavily priced proprietary tools.

Chapter 2

Analog Circuits

2.1 LM7805 Voltage Regulator

Voltage sources in a circuit may have fluctuations resulting in not providing fixed voltage outputs. A voltage regulator IC maintains the output voltage at a constant value. 7805 IC, a member of 78xx series of fixed linear voltage regulators used to maintain such fluctuations, is a popular voltage regulator integrated circuit (IC).

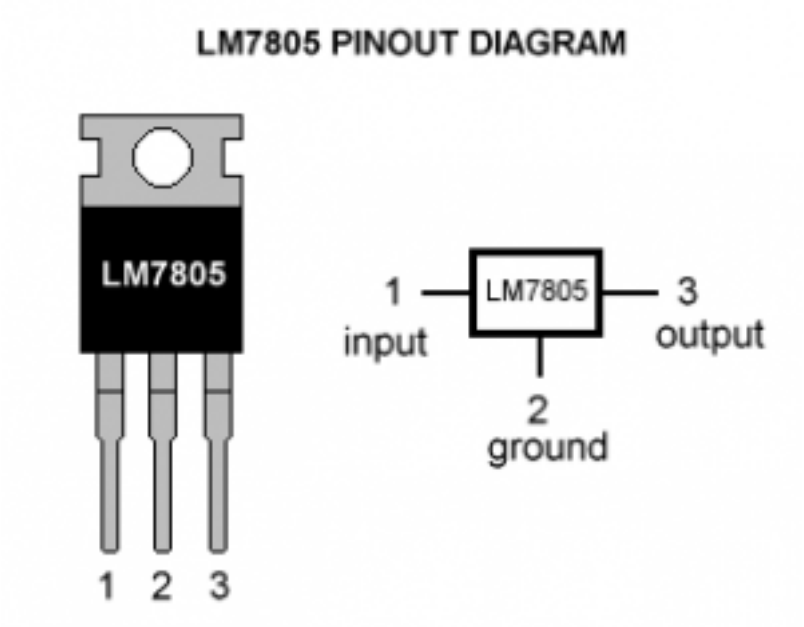

Figure 2.1: LM7805

2.1.1 Schematic Diagram

LM7805 consists of three pins IN,GND,OUT .The subcircuit of LM7805 is shown Fig. 2.2 and added in eSim_Subckt library named as LM_7805.The circuit of Voltage Regulator using LM7805 is shown in Fig. 2.3.

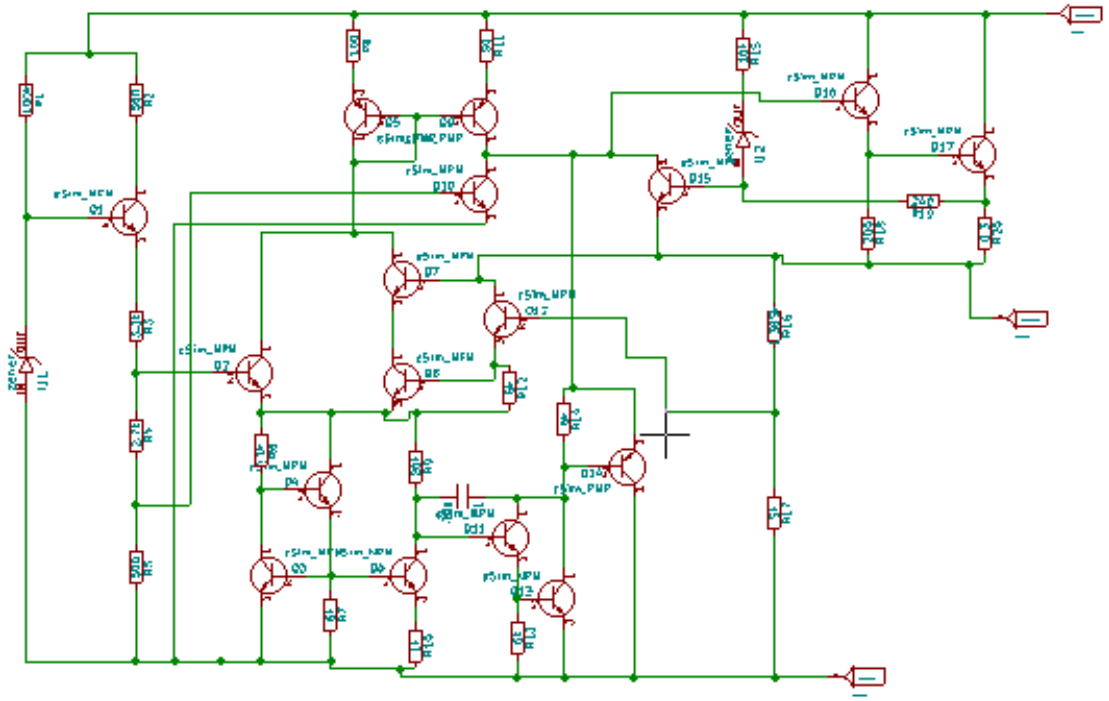

Figure 2.2: LM7805 Subcircuit

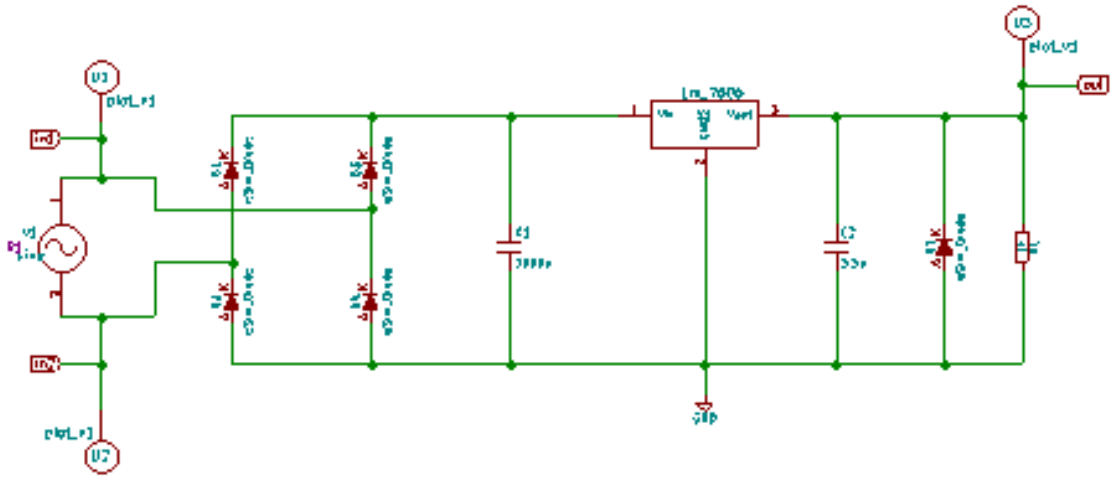

Figure 2.3: LM7805 Schematic Diagram

Reference: www.datasheets360.com/pdf/-4269426527738729779

2.1.2 Ngspice Plots

Input Plots

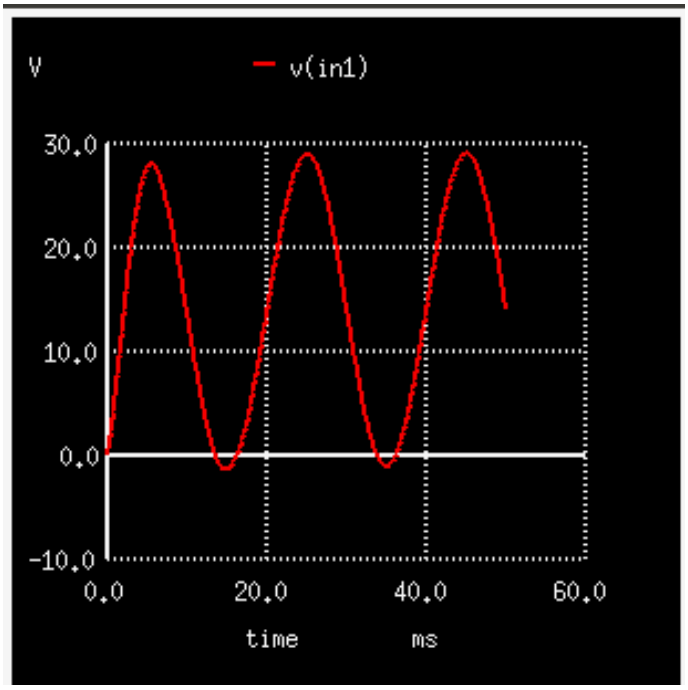

Figure 2.4: Sine Waveform

Output Plots

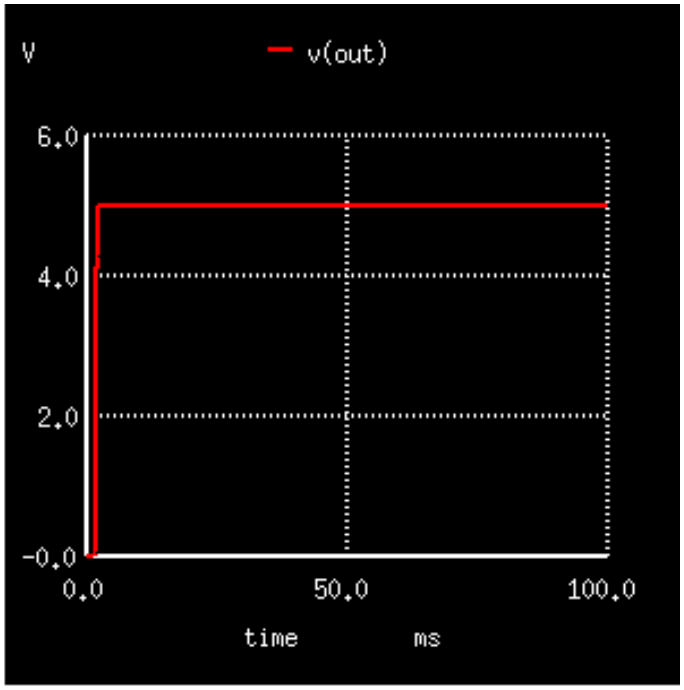

Figure 2.5: Output

2.2 LM7812 Voltage Regulator

7812 is a 12V Voltage Regulator that restricts the voltage output to 12V and draws 12V regulated power supply. The 7812 is the most common, as its regulated 12-volt supply provides a convenient power source for most TTL components. It consists of three pins namely IN,GND,OUT.The pin diagram of LM7812 is attached in Fig. 2.6.

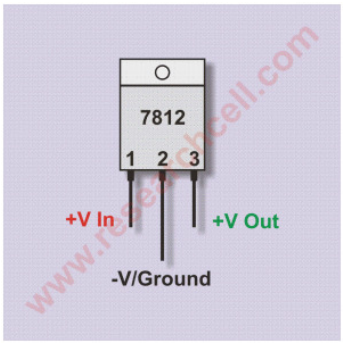

Figure 2.6: Pin Diagram of LM7812

2.2.1 Schematic Diagram

The subcircuit of LM7812 is shown in Fig. 2.7 and added in eSim_Subckt library named as LM_7812.The test circuit is shown in Fig. 2.8.

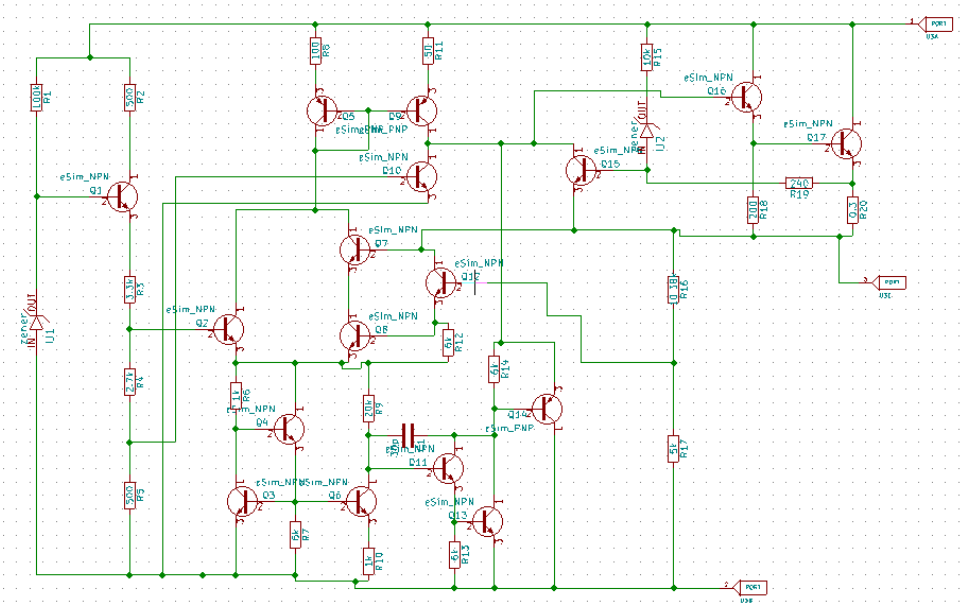

Figure 2.7: LM7812 Subcircuit Diagram

Reference: www.datasheets360.com/pdf/-4269426527738729779

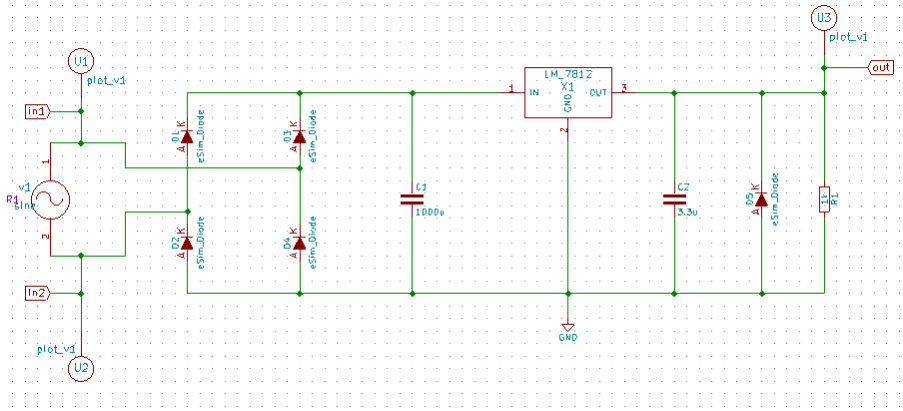

Figure 2.8: Schematic Diagram of LM7812

2.2.2 Ngspice Plots

Input Plots

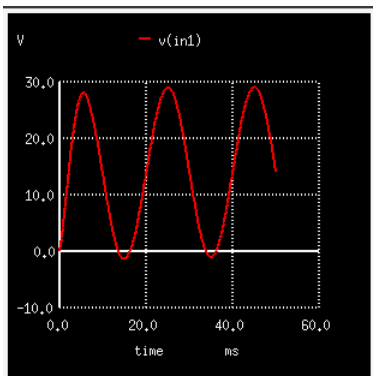

Figure 2.9: Sine Waveform

Output Plots

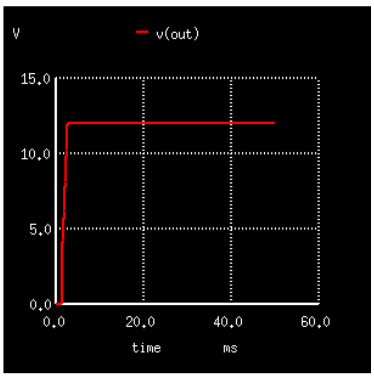

Figure 2.10: Output Plot of LM7812

2.3 Unipolar Junction Transistor(UJT)

A unijunction transistor (UJT) is a three-lead electronic semiconductor device with only one junction that acts exclusively as an electrically controlled switch.
The UJT is not used as a linear amplifier. It is used in free-running oscillators, synchronized or triggered oscillators, and pulse generation circuits at low to moderate frequencies (hundreds of kilohertz). It is widely used in the triggering circuits for silicon controlled rectifiers. The pin diagram is shown in the Fig. 2.11.

Figure 2.11: Pin Diagram of UJT

2.3.1 Schematic Diagram

The subcircuit of UJT is designed and added in eSim_Subckt library and named as UJT.The subcircuit is shown in Fig. 2.12 and the circuit of oscillator using UJT is shown in Fig. 2.13.

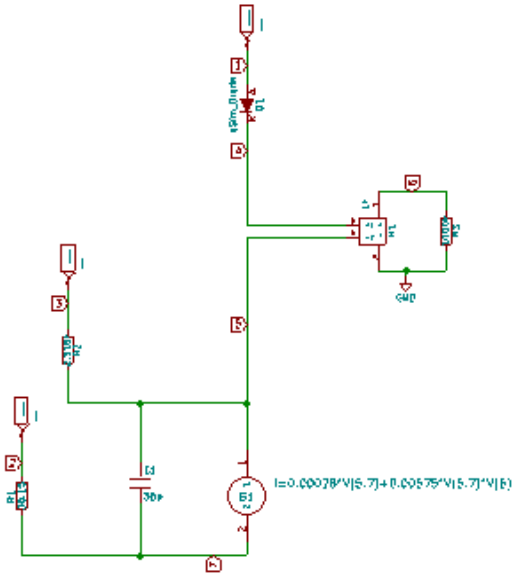

Figure 2.12: Subcircuit of UJT

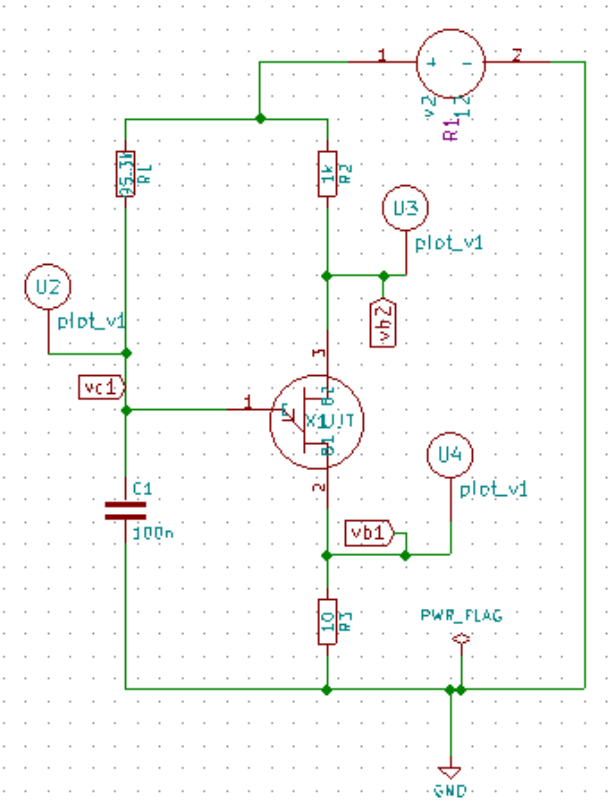

Figure 2.13: Test circuit of UJT

Reference:www.electronics-tutorials.ws/power/unijunction-transistor.html

2.3.2 Ngspice Plots

Output Plots

2.4 Opto Isolator Switch

An opto-isolator (also called an optocoupler, photocoupler, or optical isolator) is an electronic component that transfers electrical signals between two isolated circuits by using light.
Opto-isolators prevent high voltages from affecting the system receiving the signal.A common type of opto-isolator consists of an LED and a phototransistor in the same opaque package.It consists of four pins and the pin diagram is shown in Fig. 2.15.

2.4.1 Schematic Diagram

The subcircuit of Opto Isolator switch is designed and added in eSim_Subckt library.The subcircuit of Opto Isolator siwitch is shown in Fig. 2.16 and the test circuit is shown in Fig. 2.17.

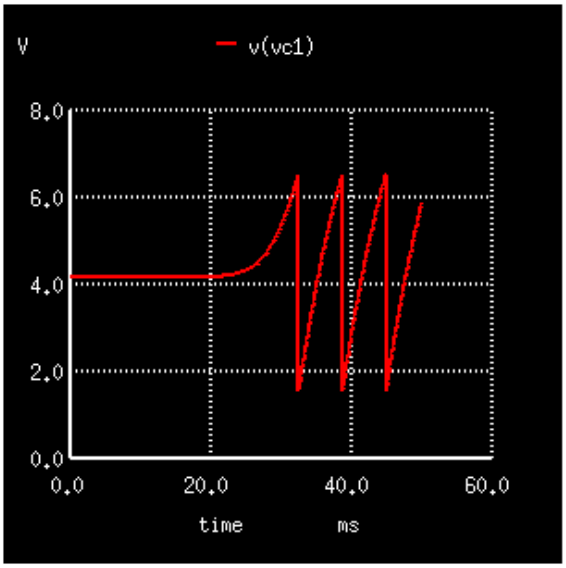

Figure 2.14: Test circuit of UJT

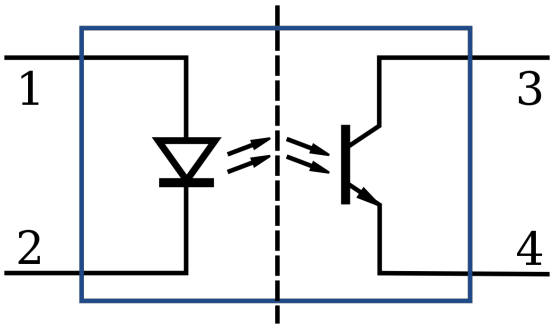

Figure 2.15: Pin Diagram of Opto Isolator Switch

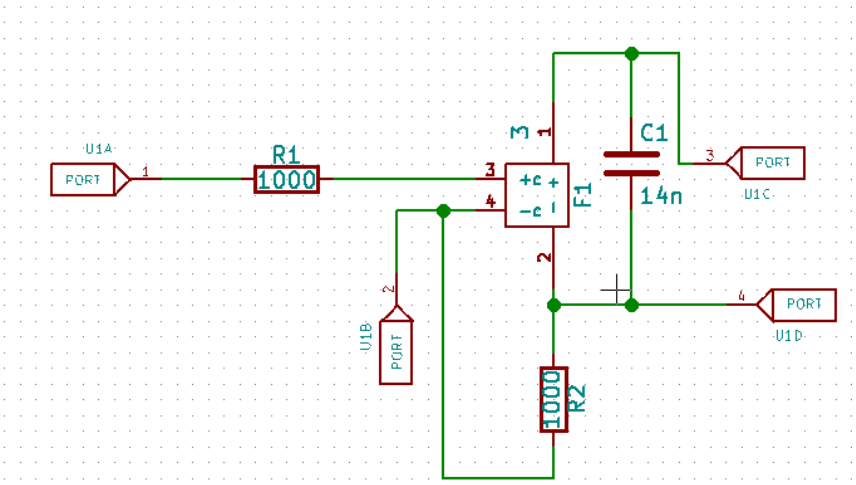

Figure 2.16: Subcircuit of Opto Isolator Switch

Reference: www.cel.com/pdf/appnotes/AN3005.pdf

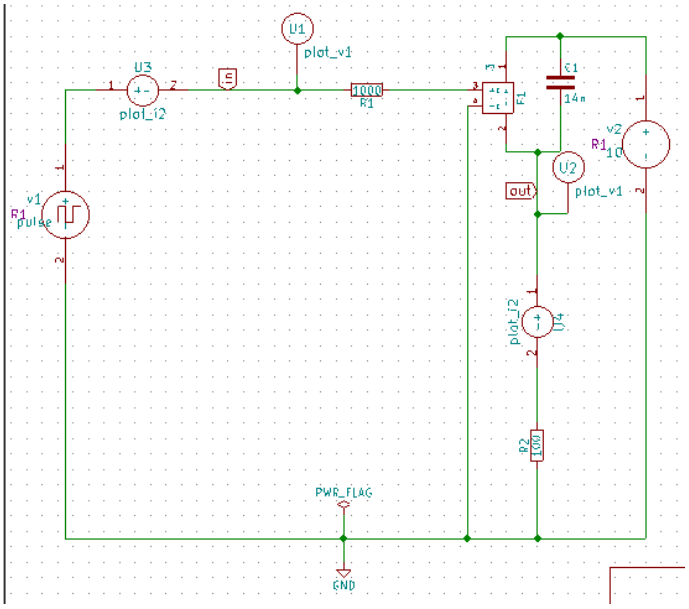

Figure 2.17: Test circuit of Opto Isolator Switch

2.4.2 Ngspice Plots

Input Plots

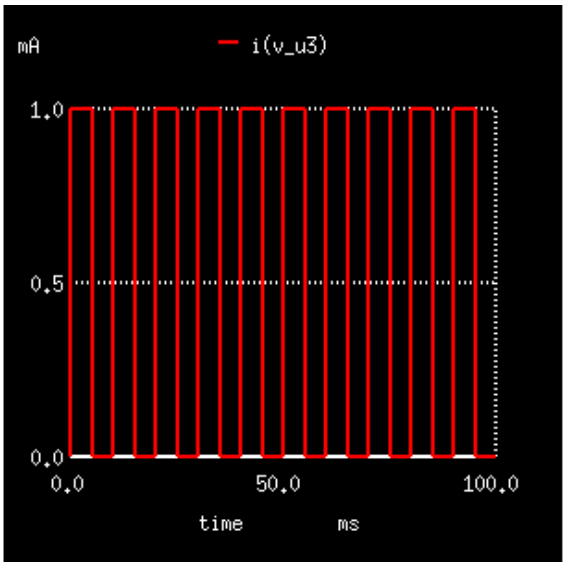

Figure 2.18: Input Current Waveform

Output Plots

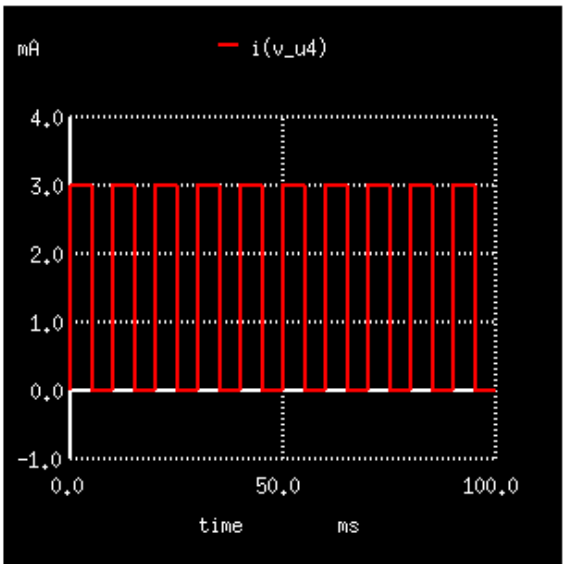

Figure 2.19: Output Current Waveform

2.5 RLC Equivalent Speaker Circuit

Speaker is the main component for all the Audio Amplifier circuits, mechanically, a speaker work with lots of physical components. A good speaker can override the noises and can provide a smooth output whereas a bad speaker can destroy your all efforts even the rest of the circuit is exceptionally good.

The circuit we designed is IB3858 Woofer Speaker and I can design any kind of speaker with desired parameters of Measured Voice Coil Resistance, Measured Voice Coil Inductance, Resonant Frequency, Mech Suspension control measurement (Surround and Spider), Electrical Suspension control measurement (Voice coil and Magnet).

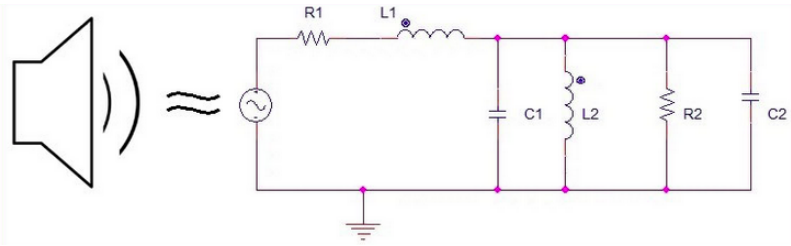

Figure 2.20: Speaker Equivalent Circuit

2.5.1 Schematic Diagram

The subcircuit is designed and added in eSim_Subckt library and named as speaker.It consists of two pins.The subcircuit is shown in Fig. **??** and the test circuit is shown in Fig. **??**.

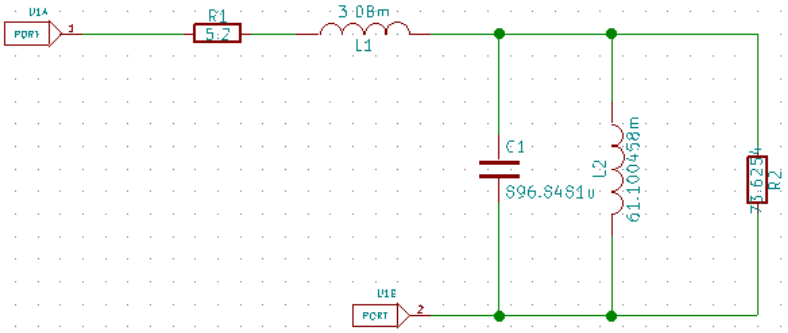

Figure 2.21: Subcircuit of Speaker IB3858

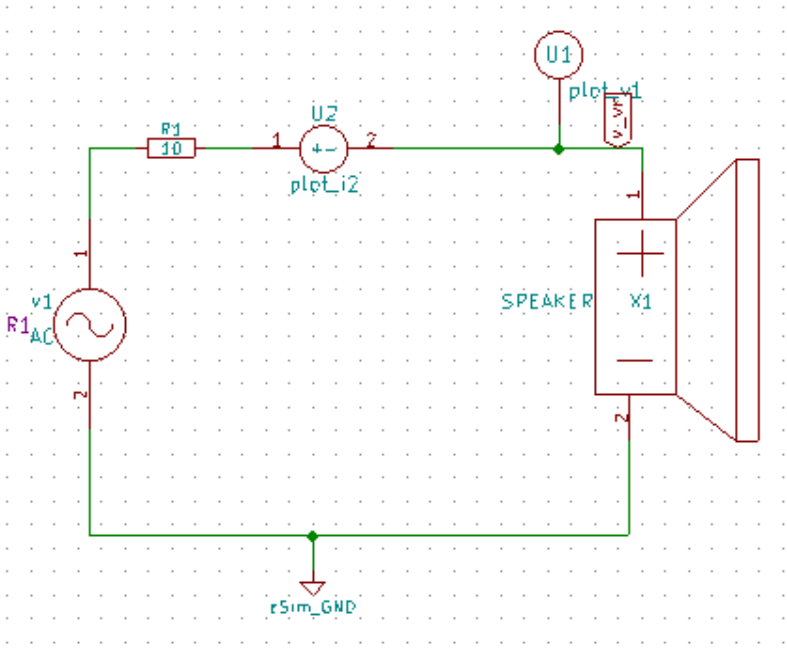

Figure 2.22: Subcircuit of Speaker IB3858

Reference: www.electro-tech-online.com/threads/ltspice-model-loudspeaker.142634/

2.6 LM 741 Operational Amplifier

The LM741 series are general-purpose operational amplifiers which feature improved performance over industry standards like the LM709.It is an 8 PIN OP AMP.
The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output,no latch-up when the common-mode range is exceeded.It has many applications like summer,comparators,multivibrators,integrators,differe filters. It is named as lm_741 under **eSim_subcircuit** library.The pin diagram is shown in the Fig. 2.23

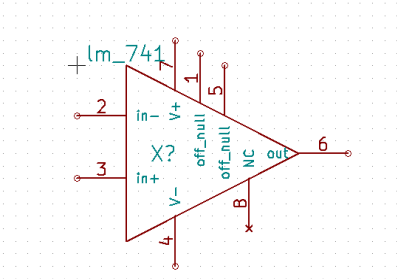

Figure 2.23: Pin diagram of lm_741

2.6.1 Schematic Diagram

The subcircuit schematic for lm_741 is shown in the Fig. 2.24

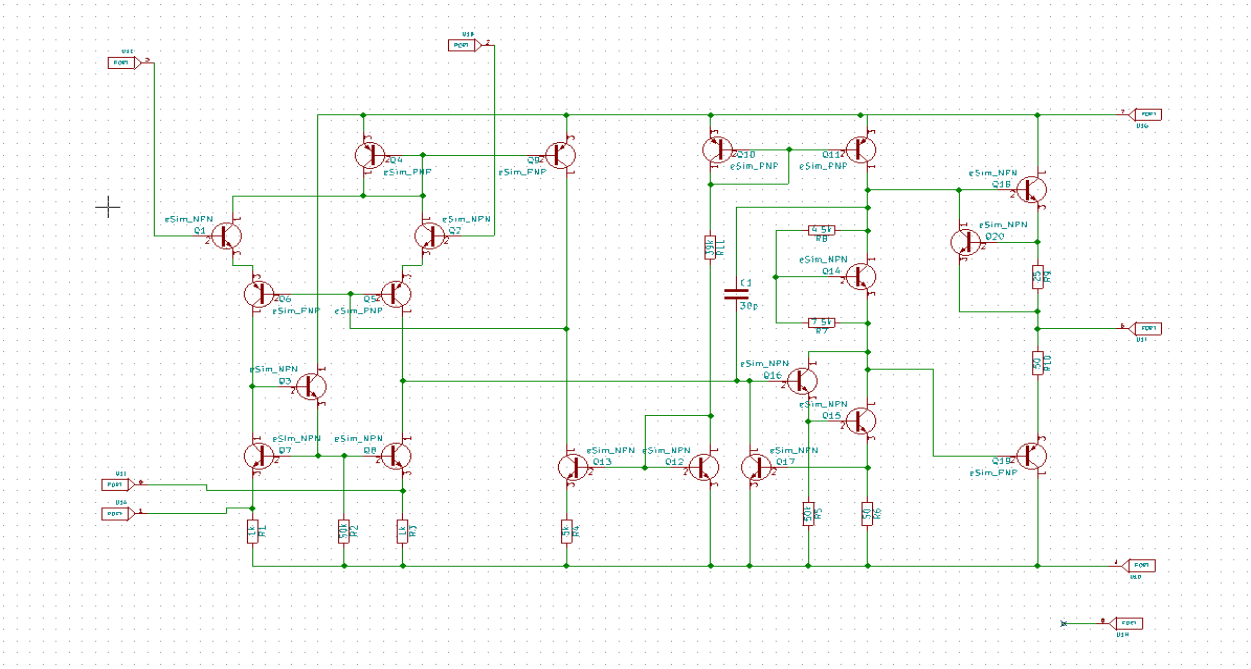

Figure 2.24: Subcircuit schematic of lm_741

Reference:-http://www.ti.com/lit/ds/symlink/lm741.pdf

2.6.2 Integrator using lm_741 OP AMP

Integrator is made using the lm_741 OP AMP as shown in the Fig. 2.25.

Schematic Diagram of Integrator

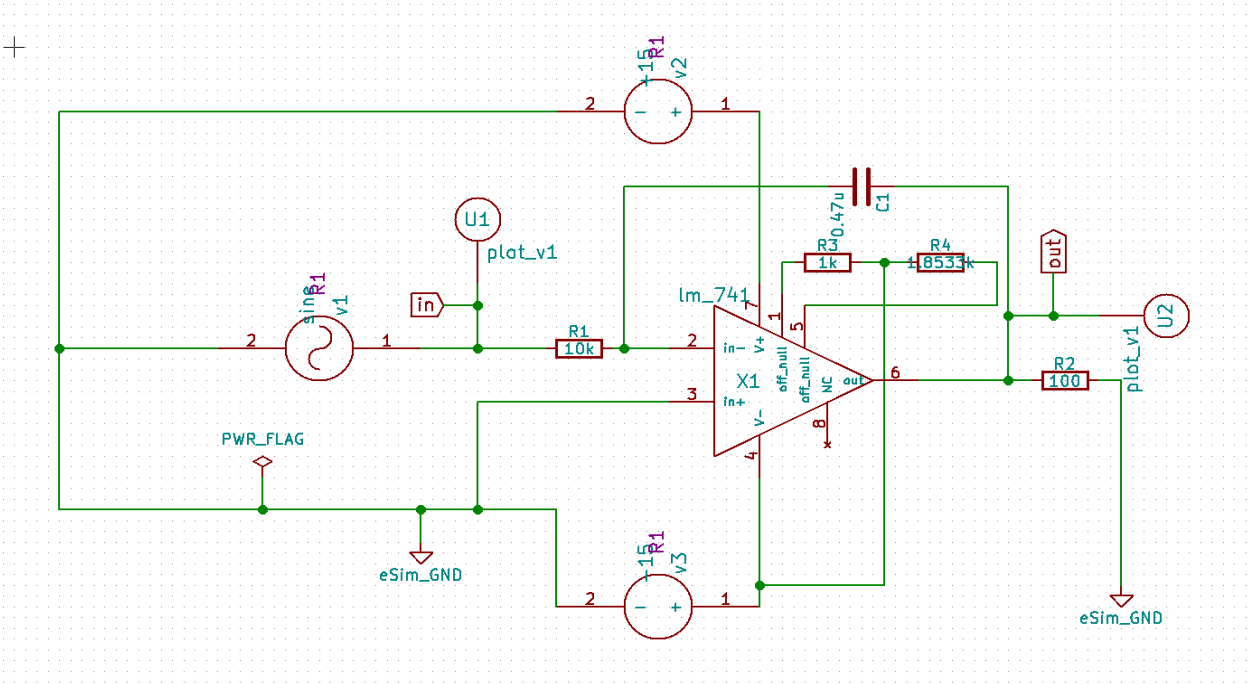

Figure 2.25: schematic for Integrator

2.6.3 Ngspice Plots

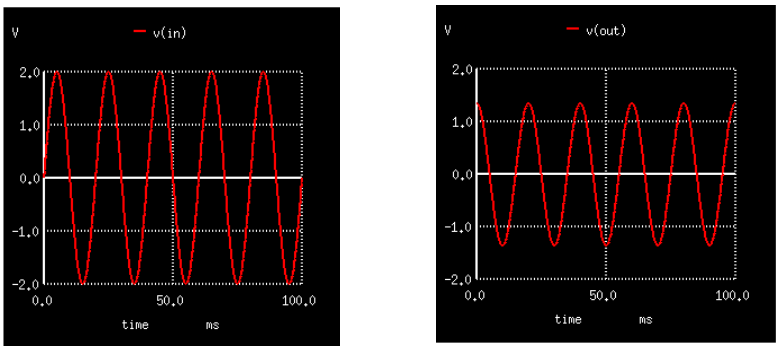

Figure 2.26: Input and Output plots of Integrator

NOTE:-To remove the offset connect two resistances as shown in the Fig. 2.27.Fix the resistance(R1) value connected to pin 5 of lm_741 and vary the resistance(R2) value connected to pin 1,such that if you want to shift the output up,increase the R2 value a little and to shift the output down ,decrease R2 value a little.

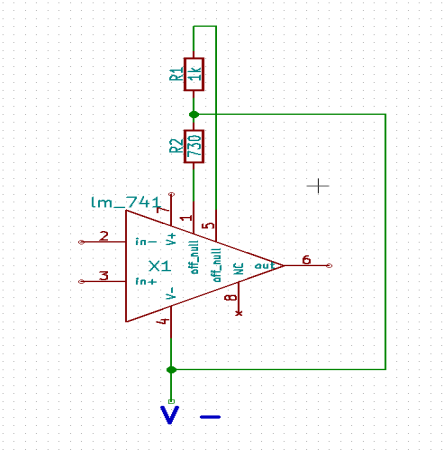

Figure 2.27: offset removing in lm_741

2.7 Instrumentation Amplifier AD620

Instrumentation amplifier is a kind of differential amplifier with additional input buffer stages. The addition of input buffer stages makes it easy to match (impedance matching) the amplifier with the preceding stage. Instrumentation are commonly used in industrial test and measurement application. The instrumentation amplifier also has some useful features like low offset voltage, high CMRR (Common mode rejection ratio), high input resistance, high gain etc.
The Instrumentation amplifier is present in the **esim_subcircuit** library named as AD620.The pin diagram of AD620 is shown in the Fig. 2.28.

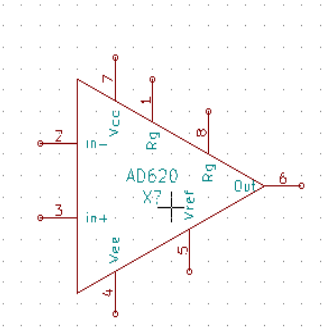

Figure 2.28: pin diagram of AD620

in- and in+ are the inverting and non-inverting terminals,depending on the resistance(Rg) value connected between pin 1 and 5, the gain(A) of the instrumentation amplifier varies.

- for Rg = 46.8 ohm Gain(A)= 1000
- for Rg = 499 ohm Gain(A)= 100
- for Rg = 56.7 Kohm Gain(A)= 10

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Any offet in the output can be nullified by connecting Vref to some other value(either positive or negative voltage).

2.7.1 Schematic Diagram

The subcircuit schematic for AD620 is shown in the Fig. 2.29 and the test circuit for AD620 is shown in the Fig. 2.30.

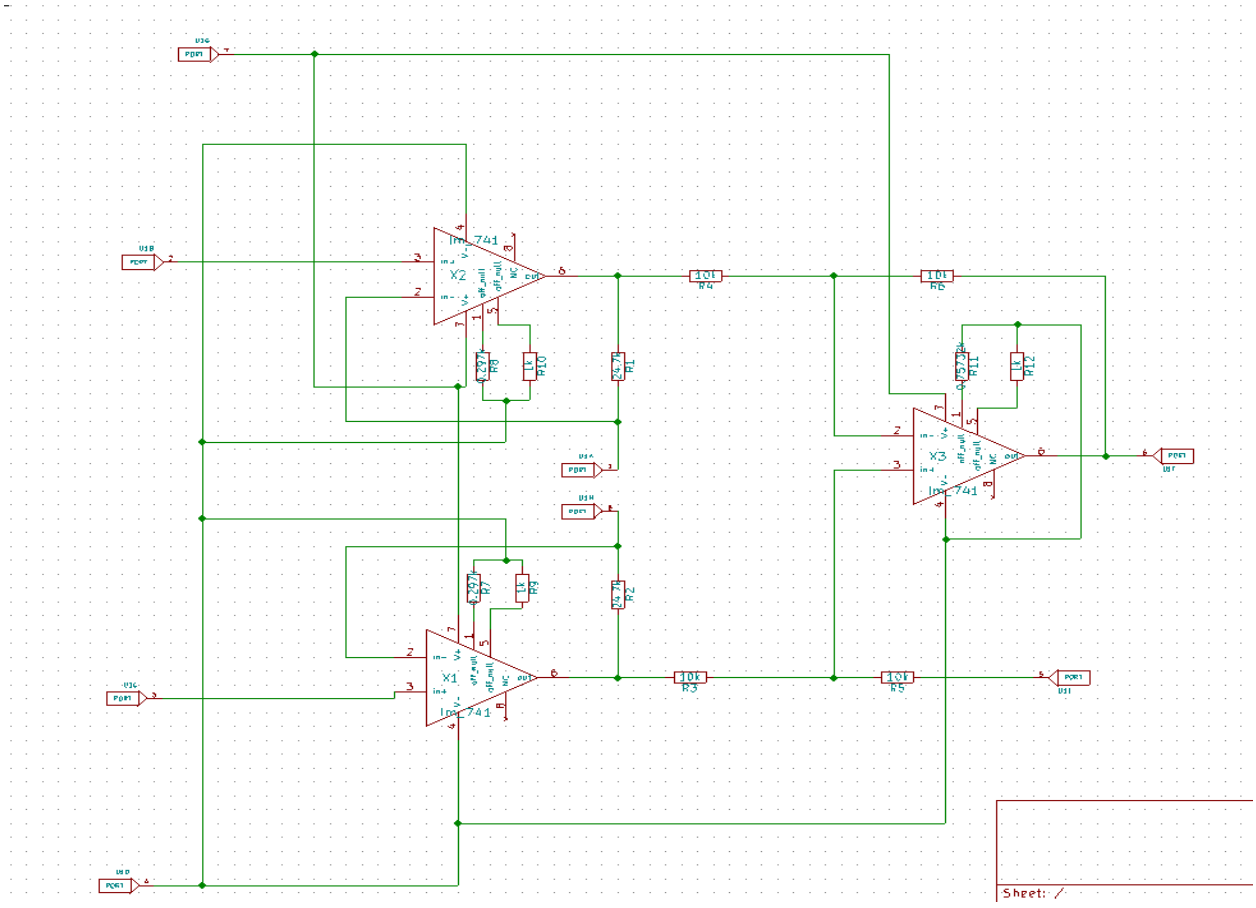

Figure 2.29: Subcircuit schematic for AD620

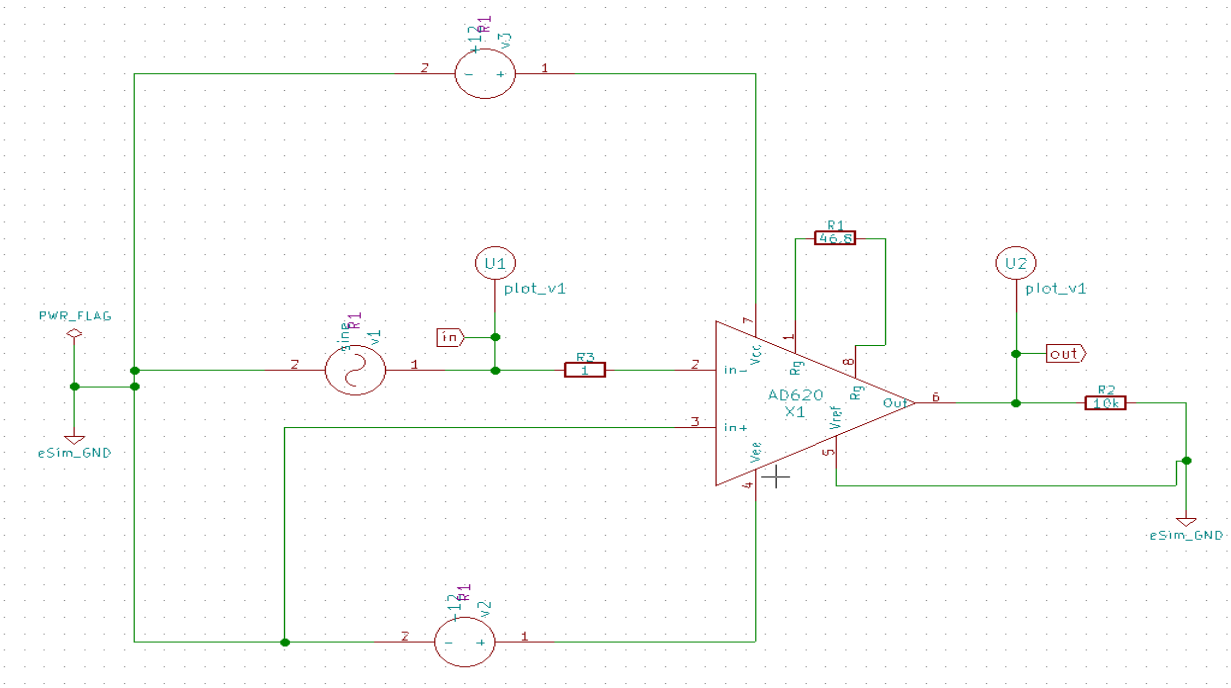

Figure 2.30: Test circuit schematic of AD620

2.7.2 Ngspuice Plots

The input and output plots for the test circuit is shown in the Fig. 2.31
Here Rg(i.e. R1) = 46.8 Ohm ,So gain = 1000.
Input is 1 mV sine wave of 100 Hz and Output is 1 V sine wave of 100 Hz

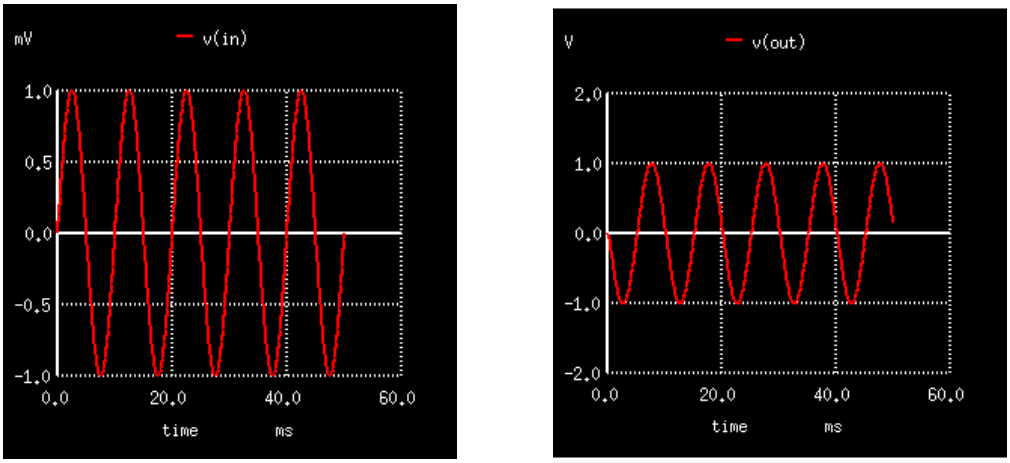

Figure 2.31: Input and Output plots of AD620 test circuit

References:-

1)https://www.analog.com/media/en/technical-documentation/data-sheets/AD620.pdf
2)https://www.cypress.com/file/51291/download

2.8 Schmitt Trigger using lm_741

A Schmitt trigger circuit is also called a regenerative comparator circuit. The circuit is designed with a positive feedback and hence will have a regenerative action which will make the output switch levels. Also, the use of positive voltage feedback instead of a negative feedback, aids the feedback voltage to the input voltage, instead of opposing it. The use of a regenerative circuit is to remove the difficulties in a zero-crossing detector circuit due to low frequency signals and input noise voltages.

Schmitt trigger circuit is shown in the Fig. 2.32. It is basically an inverting comparator circuit with a positive feedback. The purpose of the Schmitt trigger is to convert any regular or irregular shaped input waveform into a square wave output voltage or pulse. Thus, it can also be called a squaring circuit.

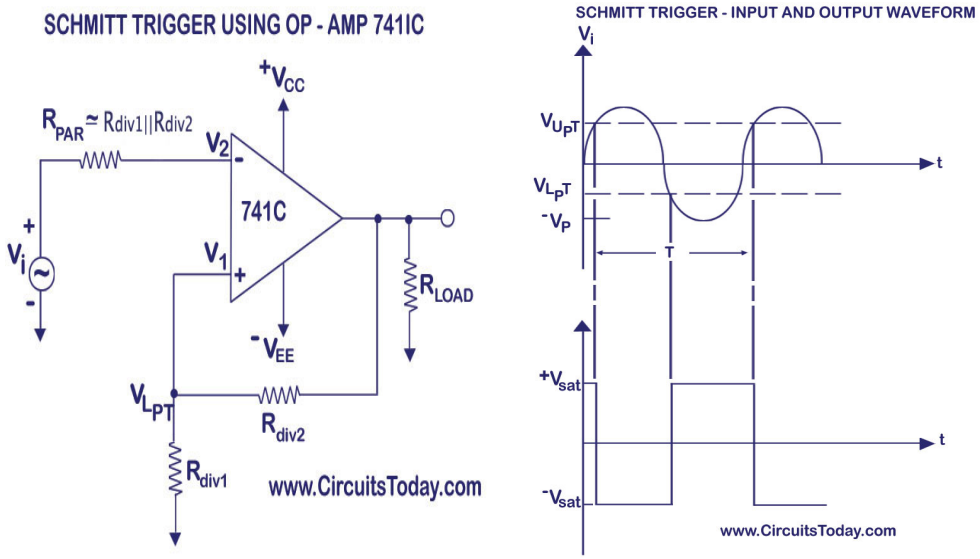

Figure 2.32: Schmitt trigger circuit and plot

Upper Threshold Voltage, Vupt = +Vsat (Rdiv1 / [Rdiv1 + Rdiv2])
Lower Threshold Voltage, Vlpt = -Vsat (Rdiv1 / [Rdiv1 + Rdiv2])

2.8.1 Schematic Diagram

The schmitt trigger schematic is shown in the Fig. 2.33
In the schematic Fig. 2.33 , Rdiv1 = 10 K Ohm and Rdiv2 = 10 K Ohm, Rpar = 1 Ohm, Vcc = + 10 V, Vee = - 10 V , Vi = sine wave of amplitude 10 V and 100 Hz.
From the plots +Vsat = 9.348 V and -Vsat = - 8.68 V.
Therefore Vupt = 4.674 V and Vlpt = - 4.34 V

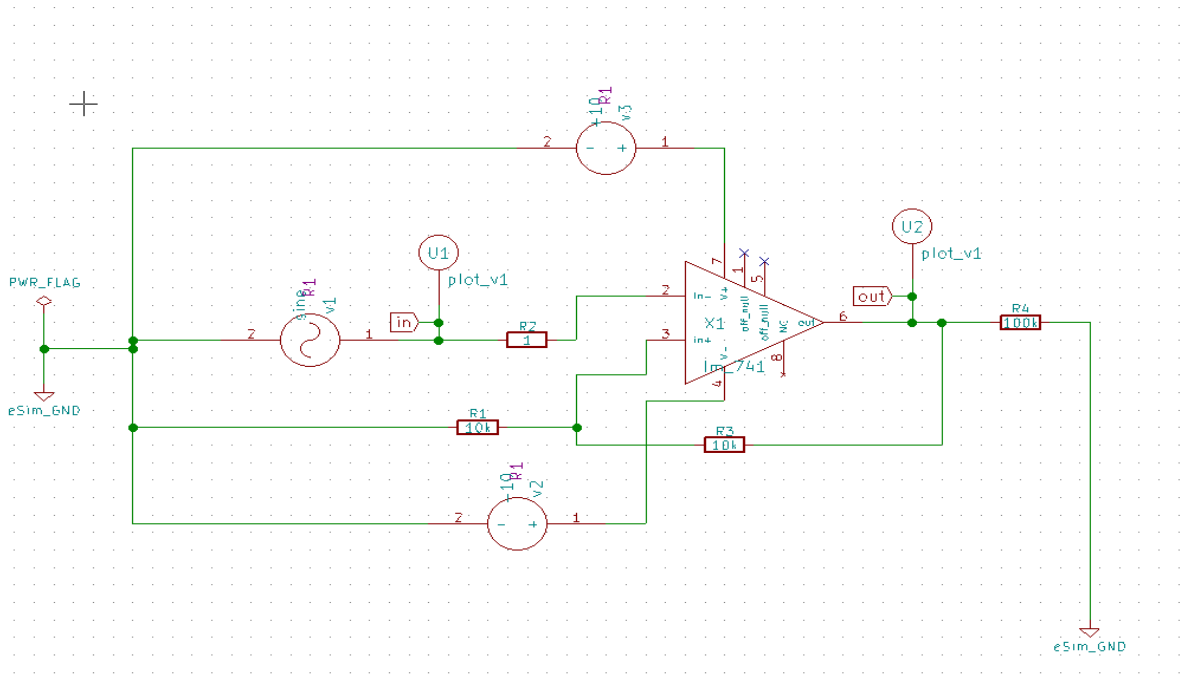

Figure 2.33: Schmitt trigger circuit schematic

2.8.2 Ngspice Plots

The input and output plots are shown in the Fig. 2.34.

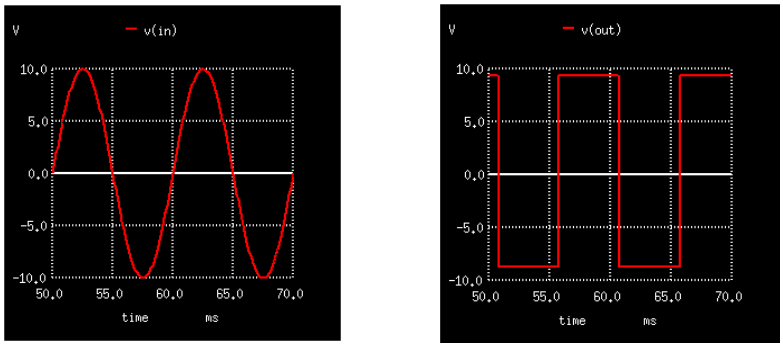

Figure 2.34: Input and Output plots of Schmitt trigger

Reference:-http://www.circuitstoday.com/schmitt-trigger-using-op-amp

Chapter 3

Digital Circuits

3.1 4002 IC

The 4002 is a member of the 4000 Series CMOS range, and contains two **independent NOR gates**, each with four inputs. The pinout diagram, shown in Fig. 3.1, is the standard four-input CMOS logic gate IC layout. Here 4012 IC is named as **IC_4012** under **eSim_Subcircuit.lib**.

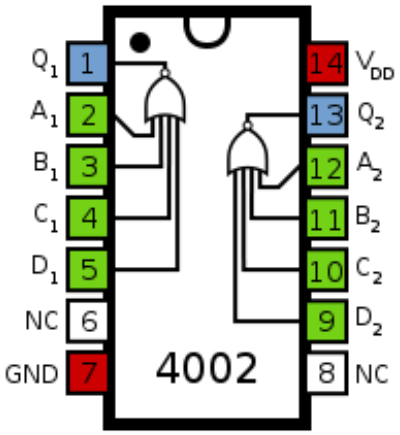

Figure 3.1: Pin Diagram of 4002 IC

3.1.1 Schematic Diagram

The subcircuit diagram is shown in Fig. 3.2 and the test circuit is shown in Fig. 3.3.

Reference: www.ti.com/lit/ds/symlink/cd54hc4002.pdf .
Note : Since we did not use MOSFET Model no need to connect Vcc and GND.

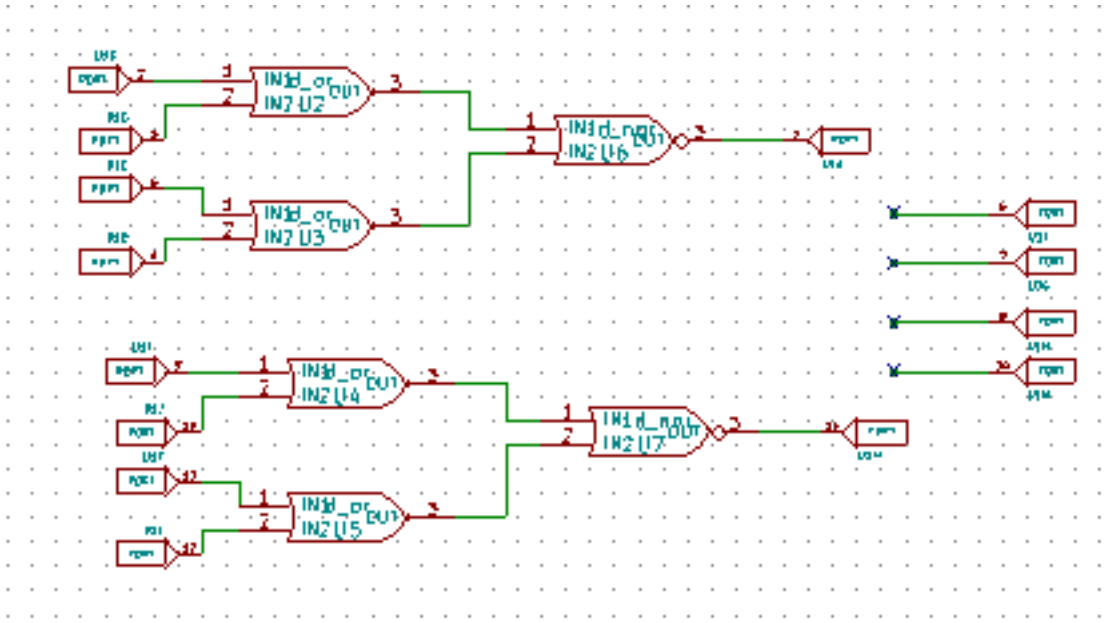

Figure 3.2: 4002 IC Subcircuit

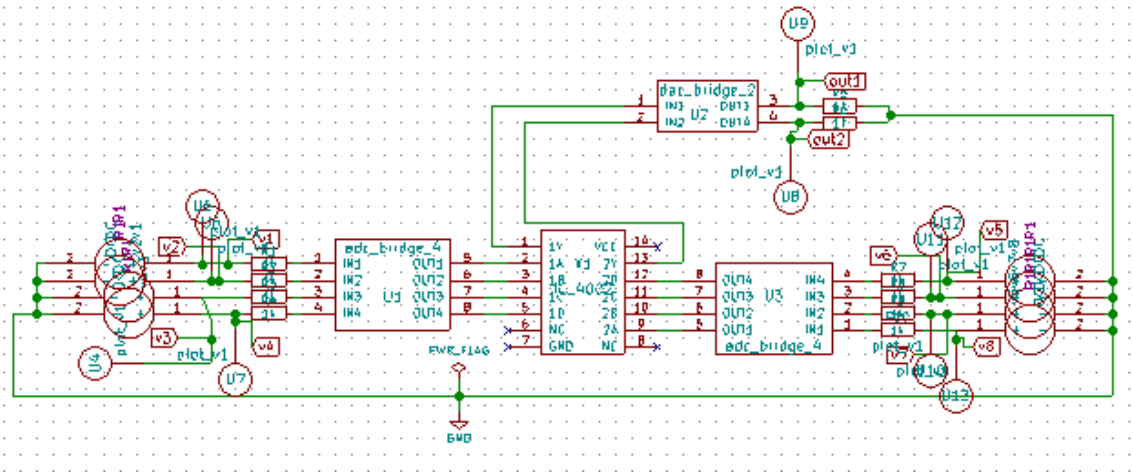

Figure 3.3: Test Circuit of IC 4002

3.1.2 Ngspice Plots

Input Plots

Inputs are: a0 =0;a1=0;a2=0;a3=0.Output y1:5.
b0 =0;b1=5;b2=0;b3=0.Output y2:0.

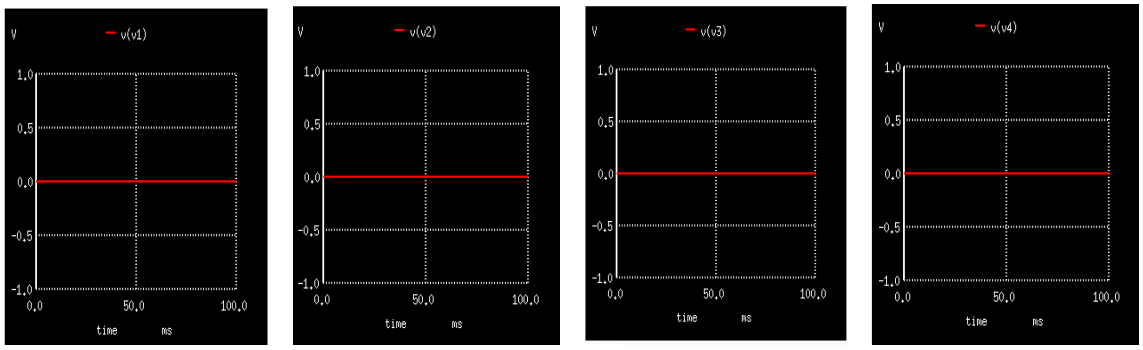

Figure 3.4: Inputs for Nor Gate 1

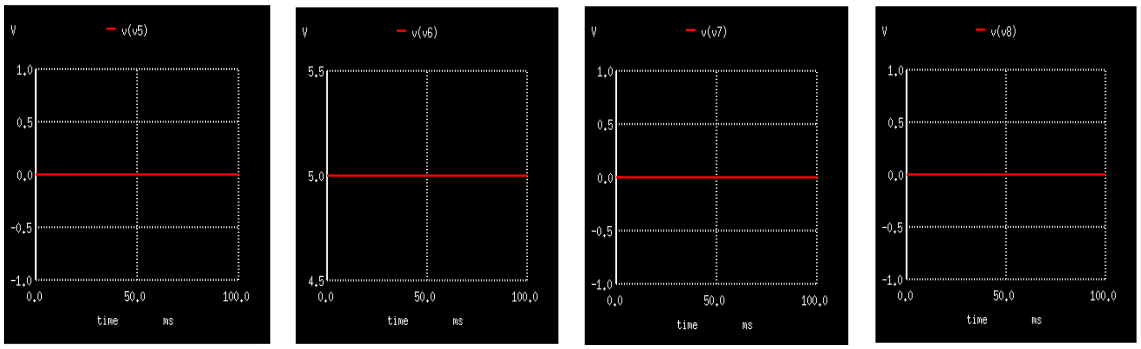

Figure 3.5: Inputs for Nor Gate 2

Output Plots

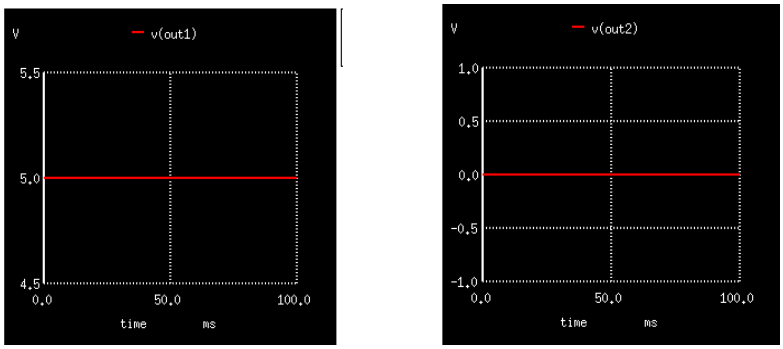

Figure 3.6: Outputs for Nor Gates 1 & 2

3.2 4025 IC

The 4025 is a member of the 4000 Series CMOS range, and contains three **independent NOR gates**, each with three inputs. The pinout diagram, shown in Fig. 3.7, is the standard four-input CMOS logic gate IC layout. Here 4025 IC is named as **IC_4025** under **eSim_Subcircuit.lib**.

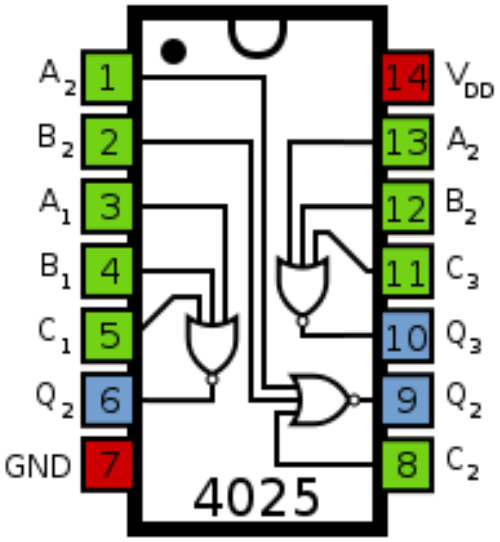

Figure 3.7: Pin Diagram of 4025 IC

3.2.1 Schematic Diagram

The subcircuit diagram is shown in Fig. 3.8 and the test circuit is shown in Fig. 3.9.

Reference: http://www.sycelectronica.com.ar/semiconductores/CD4025.pdf

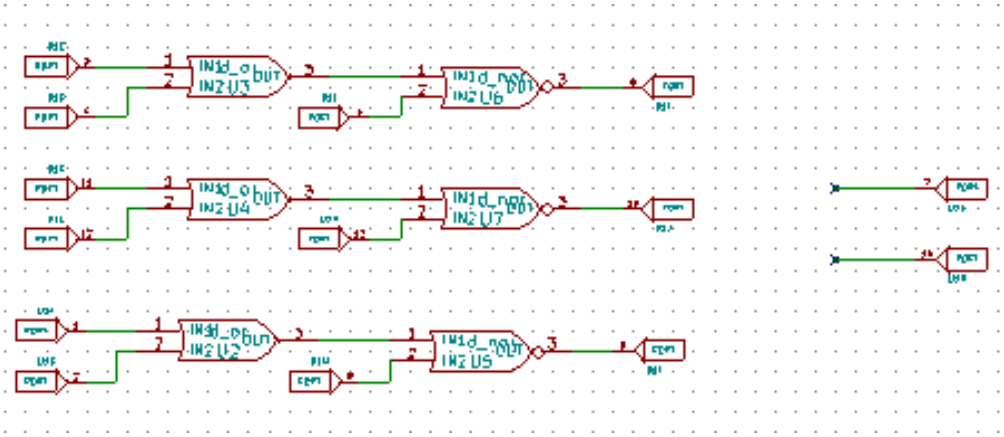

Figure 3.8: 4025 IC Subcircuit

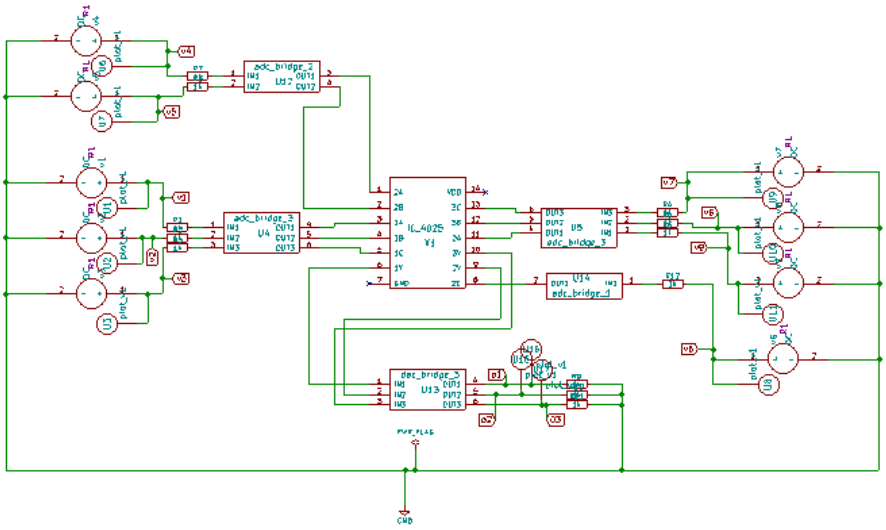

Figure 3.9: Schematic Diagram of IC 4025

3.2.2 Ngspice Plots

Input Plots

Inputs are

a1= ’5’,b1= ’5’,c1= ’5’ Output q1=’0’

a2= ’0’,b2= ’0’,c2= ’0’ Output q2=’5’

a3= ’0’,b3= ’5’,c3= ’0’ Output q3=’0’

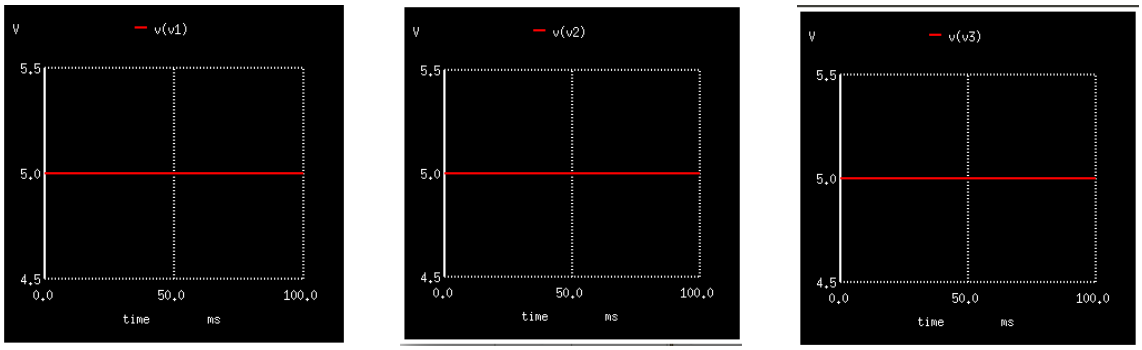

Figure 3.10: Inputs of Nor Gate 1

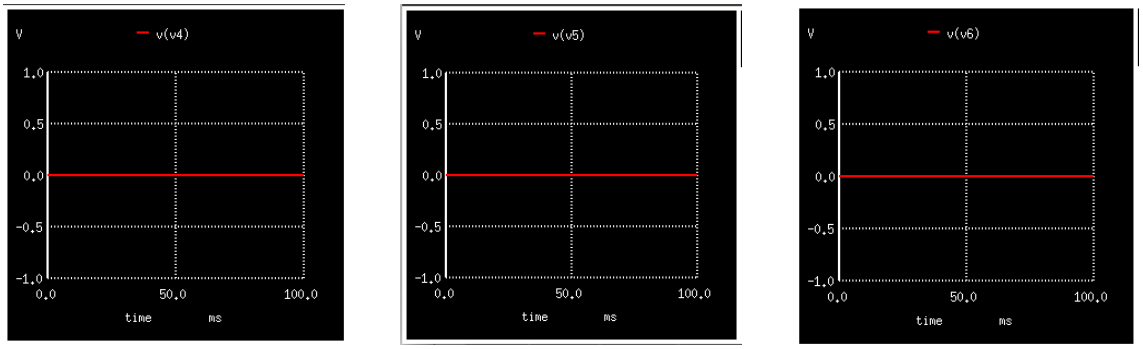

Figure 3.11: Inputs of Nor Gate 1

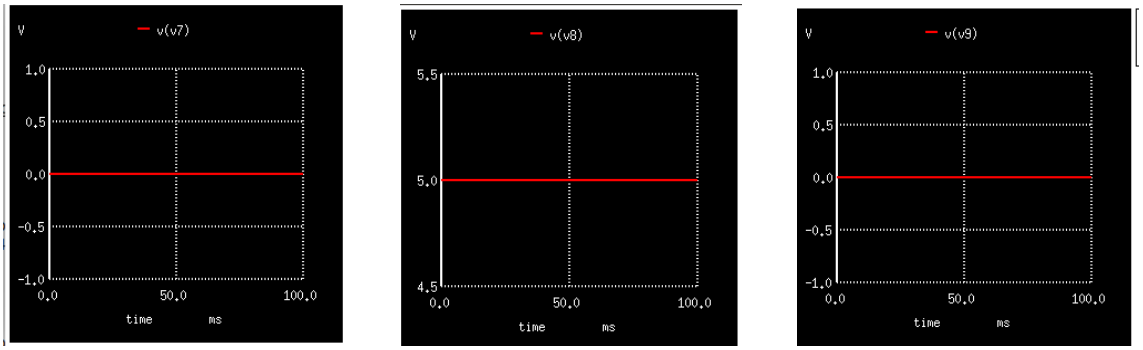

Figure 3.12: Inputs of Nor Gate 1

Output Plots

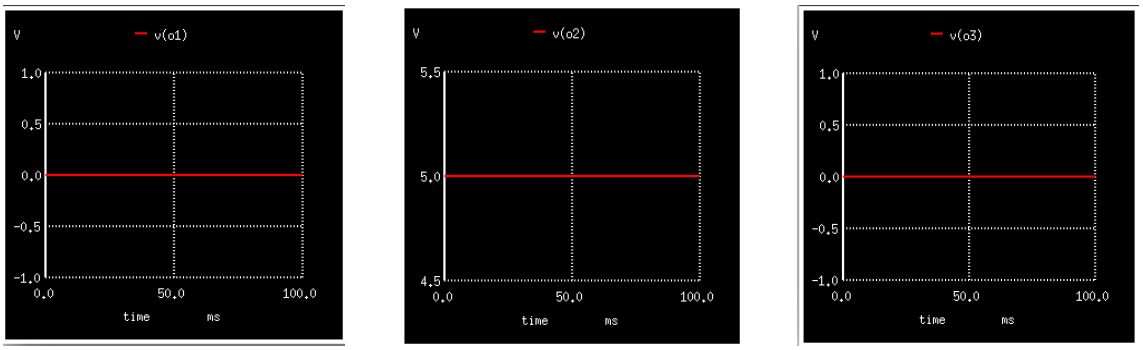

Figure 3.13: Outputs of Nor Gates of IC 4025

3.3 4012 IC

The 4012 is a member of the 4000 Series CMOS range, and contains two **independent NAND gates**, each with four inputs. The pinout diagram, shown in Fig. 3.14, is the standard four-input CMOS logic gate IC layout. Here 4012 IC is named as **IC_4012** under **eSim_Subcircuit.lib**

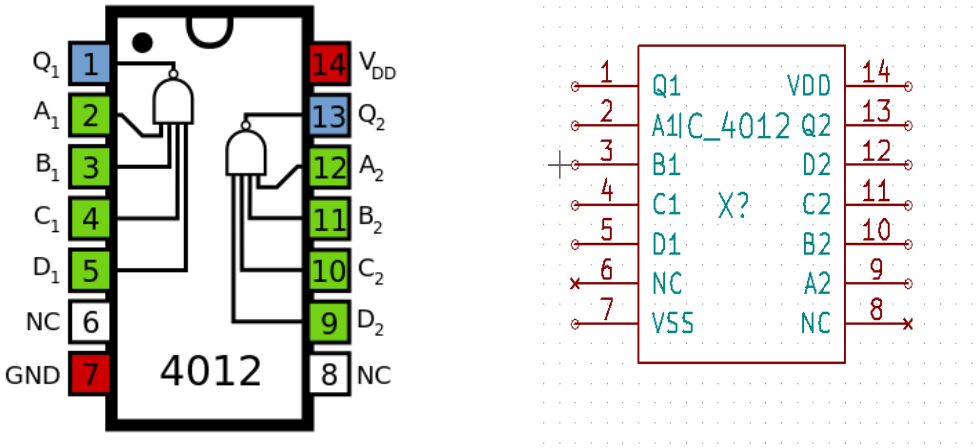

Figure 3.14: PIN Diagram of 4012 IC

3.3.1 Schematic Diagram

4012 IC subcircuit is shown in the Fig. 3.15 and test circuit for 4012 IC is shown in Fig. 3.16

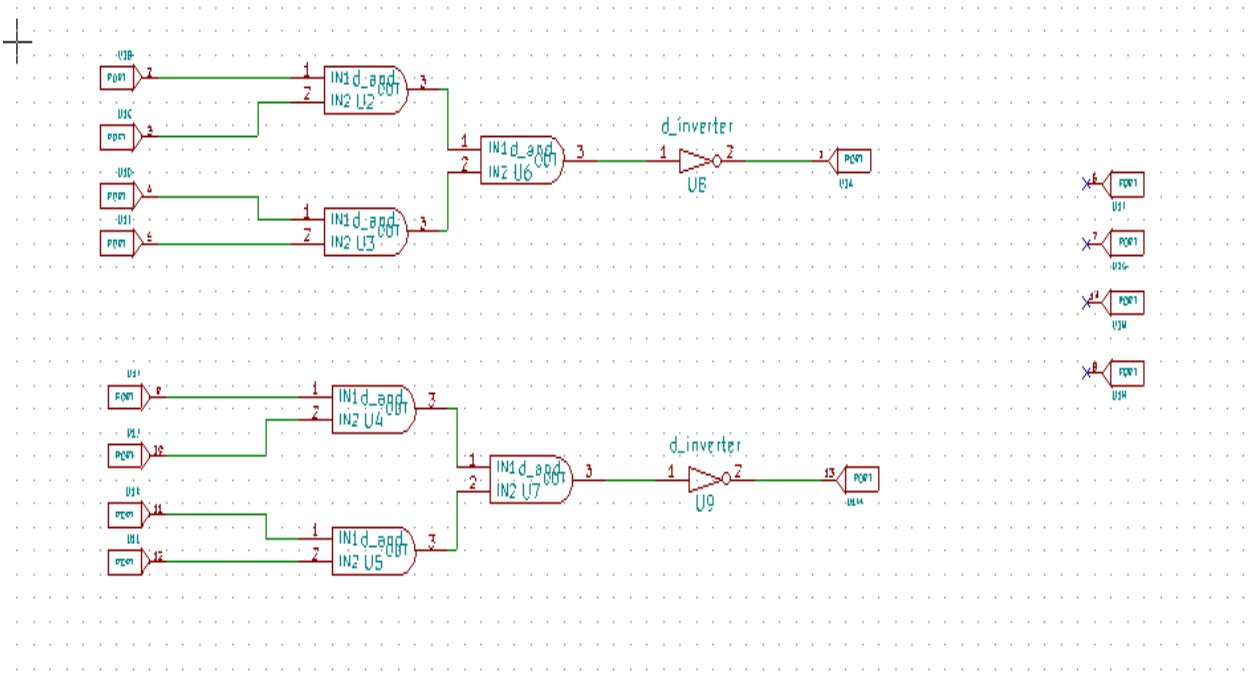

Figure 3.15: Subcircuit for 4012

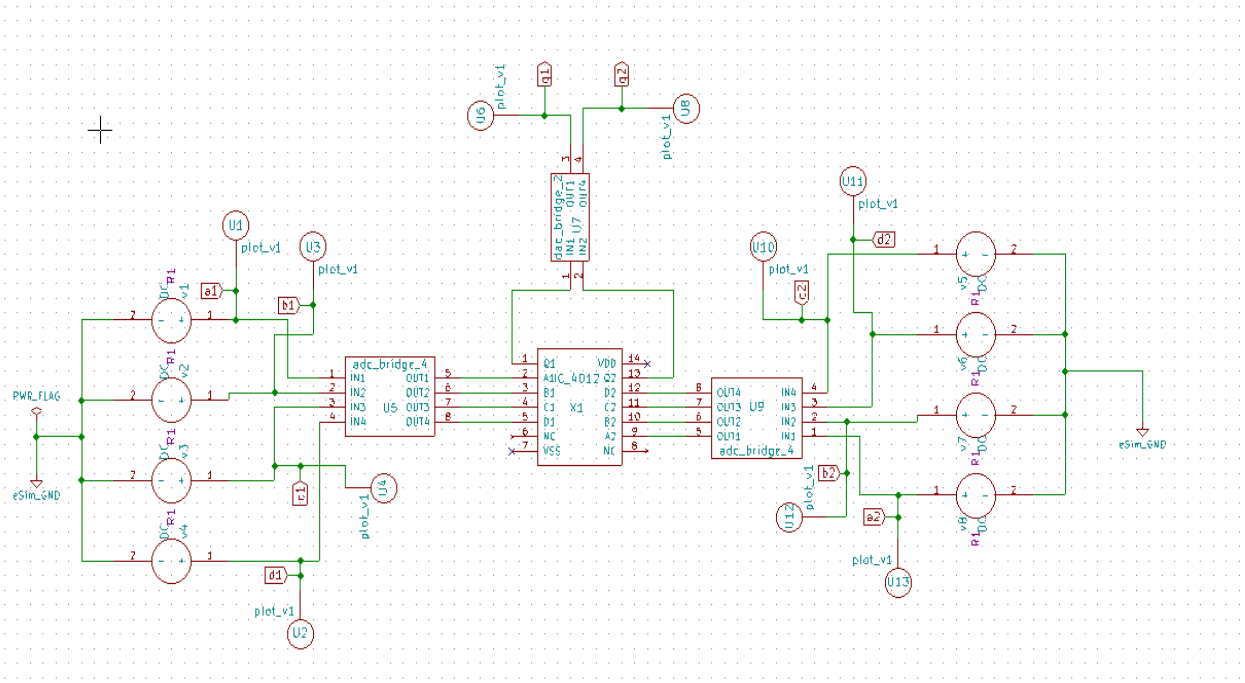

Figure 3.16: Test circuit for 4012

3.3.2 Ngspice Plots

Inputs and Outputs are
a1='1' b1='1' c1='1' d1='1' ==> q1='0'
a2='0' b2='1' c2='0' d2='0' ==> q1='1'

Input Plots

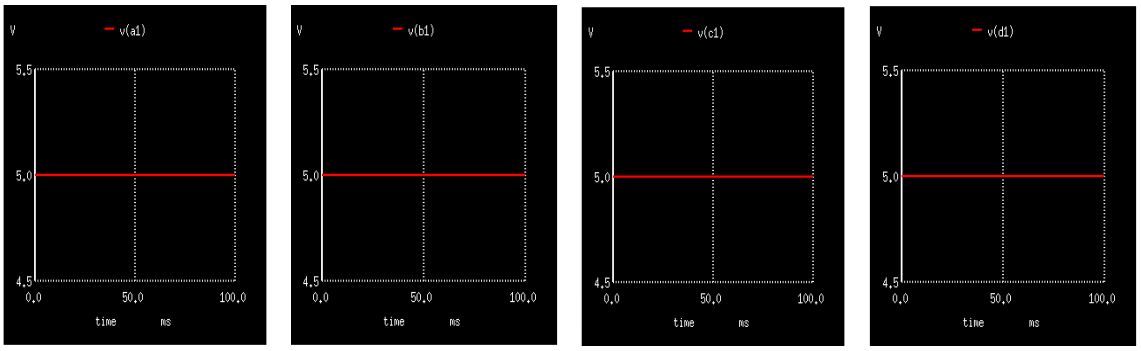

Figure 3.17: Inputs for Nand Gate 1

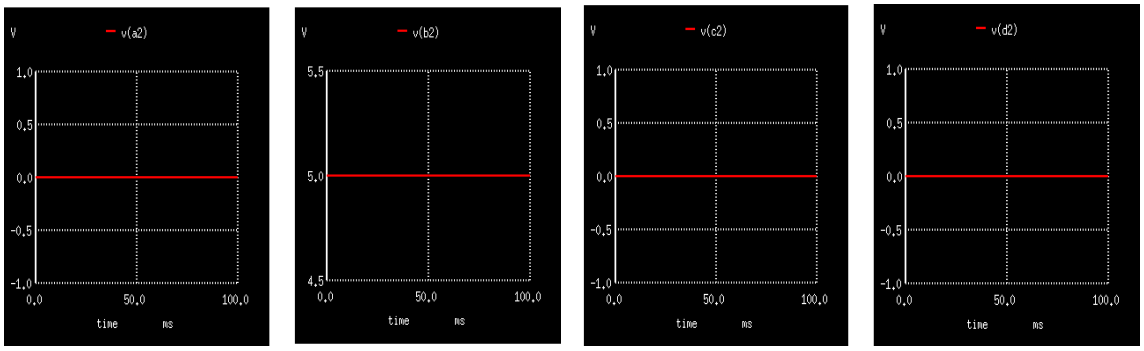

Figure 3.18: Inputs for Nand Gate 2

Output Plots

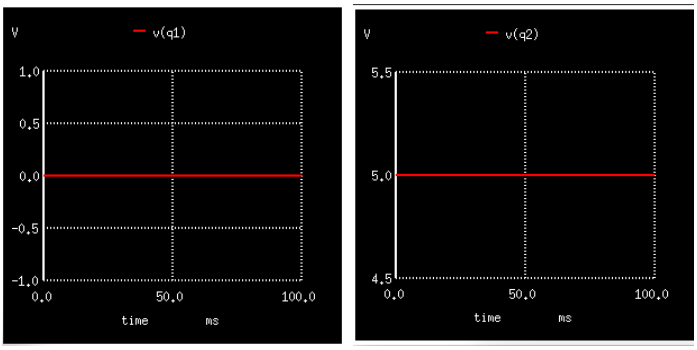

Figure 3.19: Outputs for Nand gates 1 & 2

Reference:-http://www.ti.com/lit/ds/symlink/cd4012b.pdf

3.4 4023 IC

The 4023 is a member of the 4000 Series CMOS range, and contains three **independent NAND gates**, each with three inputs. The pinout diagram, shown in Fig. 3.20, is the standard four-input CMOS logic gate IC layout. Here 4023 IC is named as **IC_4023** under **esim_Subcircuit.lib**

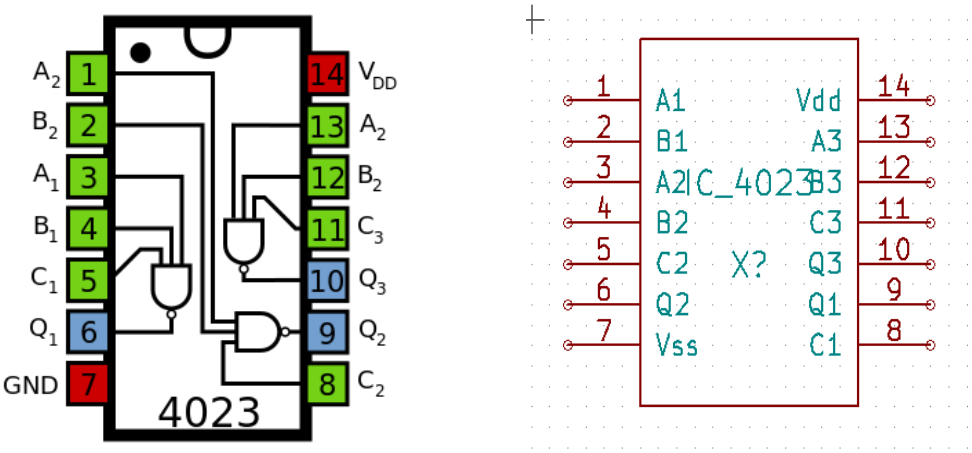

Figure 3.20: PIN Diagram of 4023 IC

3.4.1 Schematic Diagram

4023 IC subcircuit is shown in the Fig. 3.21 and test circuit for 4023 IC is shown in Fig. 3.22

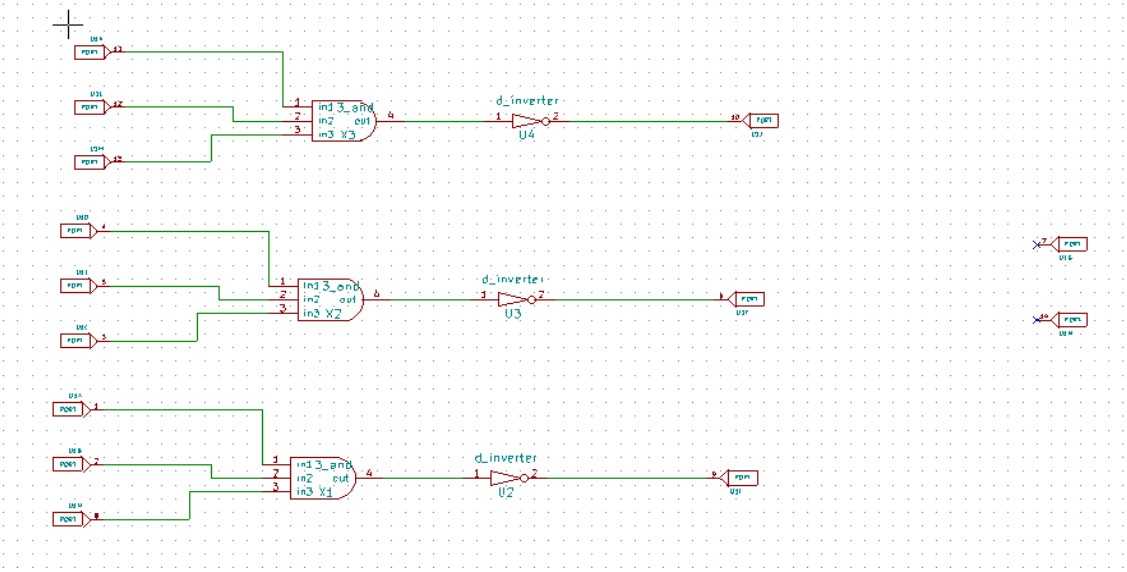

Figure 3.21: Subcircuit for 4023

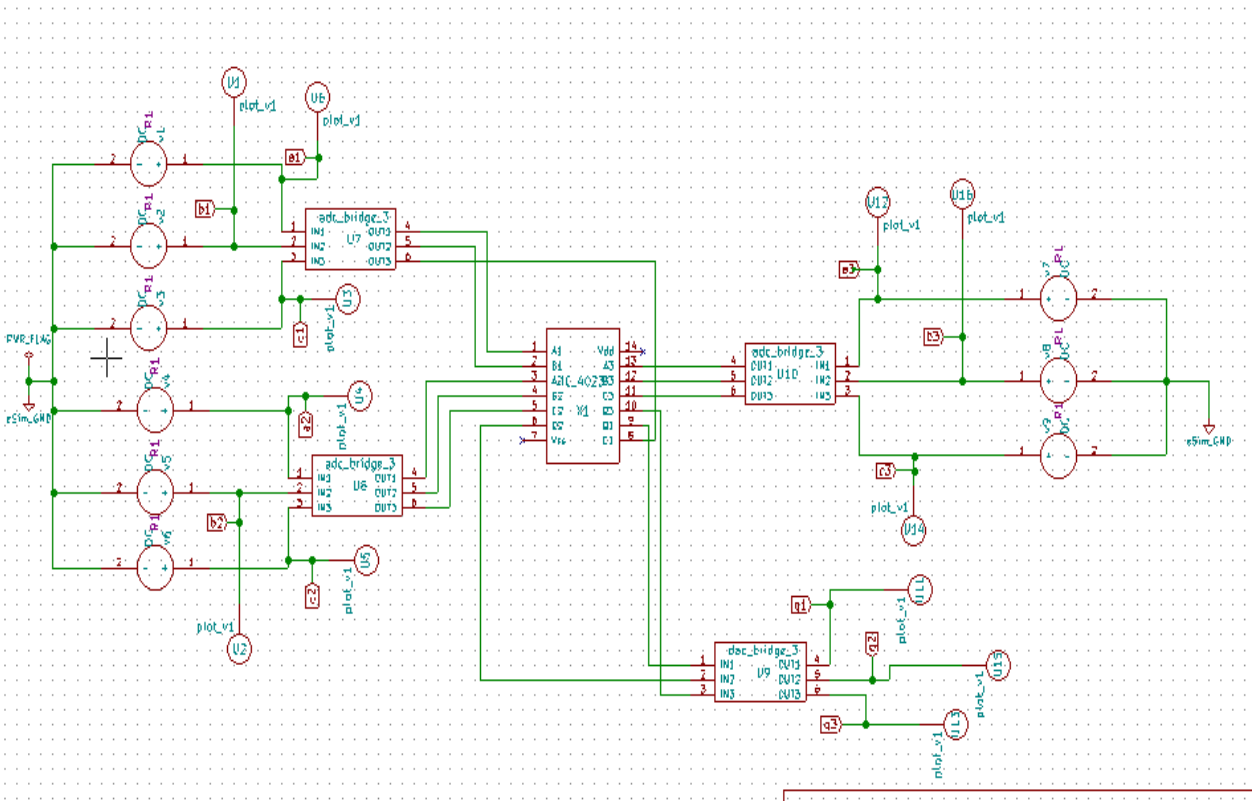

Figure 3.22: Test circuit for 4023

3.4.2 Ngspice Plots

Inputs and outputs are
a1= '0',b1= '1',c1= '0' ==> q1='1'
a2= '0',b2= '0',c2= '1' ==> q2='1'
a3= '1',b3= '1',c3= '1' ==> q3='0'
Input Plots

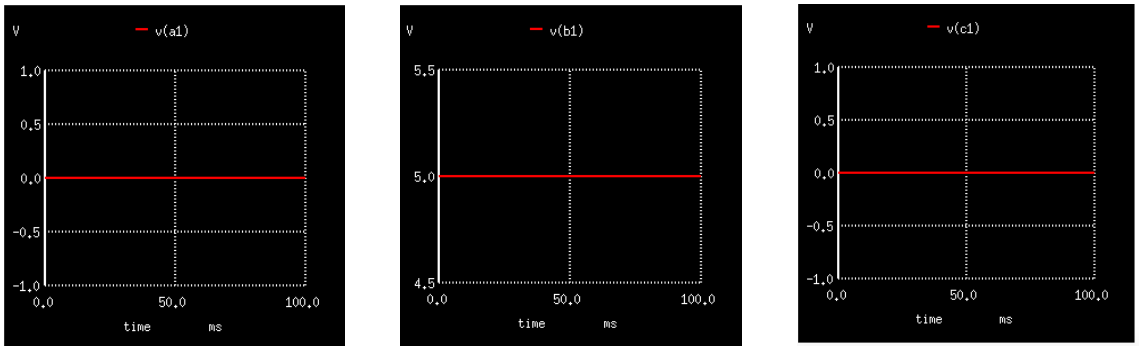

Figure 3.23: Inputs for Nand Gate 1

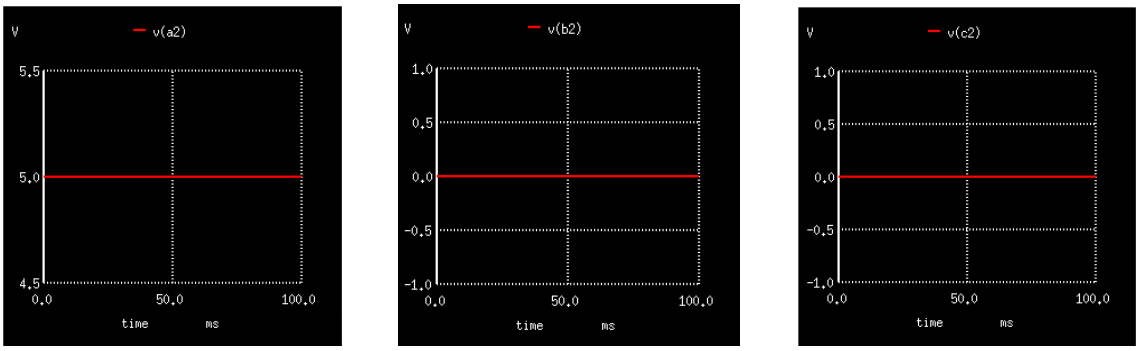

Figure 3.24: Inputs for Nand Gate 2

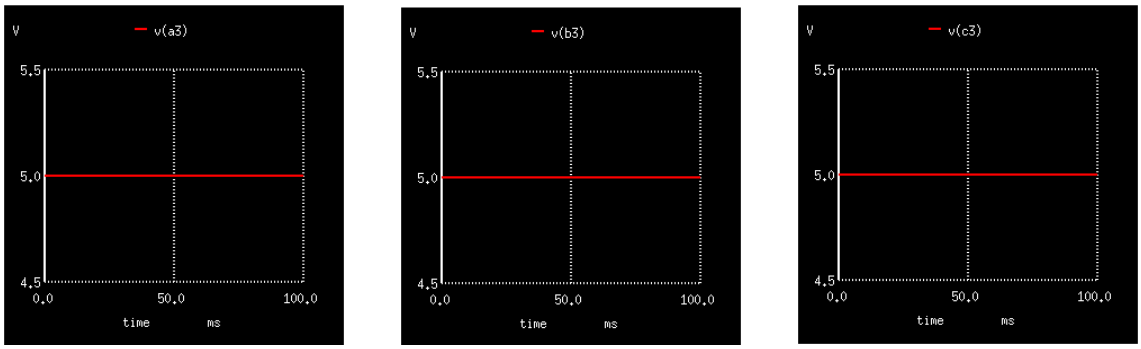

Figure 3.25: Inputs for Nand Gate 3

Output Plots

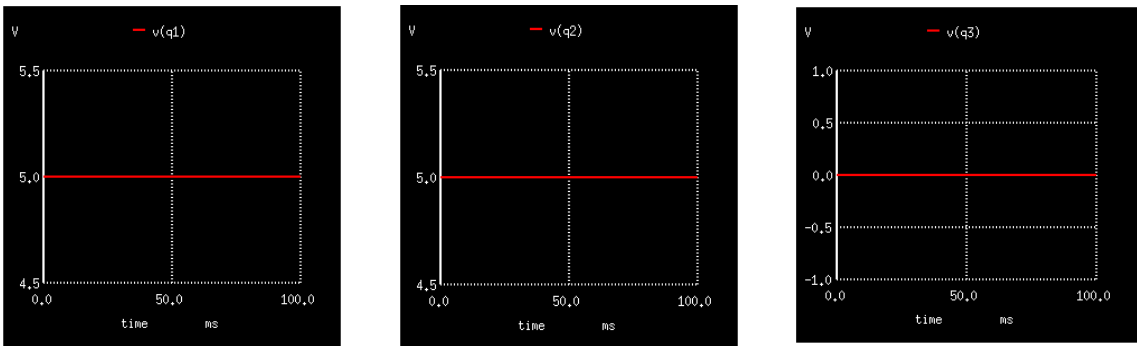

Figure 3.26: Outputs for Nand Gate 1 2 and 3

Reference:-http://www.ti.com/lit/ds/symlink/cd4012b.pdf

3.5 4028 IC

4028 IC is a BCD-to-decimal or binary-to-octaldecoder consisting of 4 inputs(A3..A0), decoding logic gates, and 10 active high outputs(Q9..Q0). A BCD code applied to the four inputs, A3 to A0, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A0 through A3 is decoded in octal code at output Q0 to Q7 if A3 = '0'.Pin diagram of 4028 is shown in Fig. 3.27

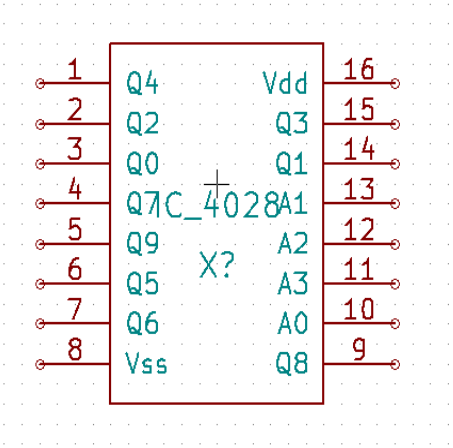

Figure 3.27: pin diagram for 4028

3.5.1 Schematic Diagram

4028 IC subcircuit is shown in the Fig. 3.28 and test circuit for 4028 IC is shown in Fig. 3.29

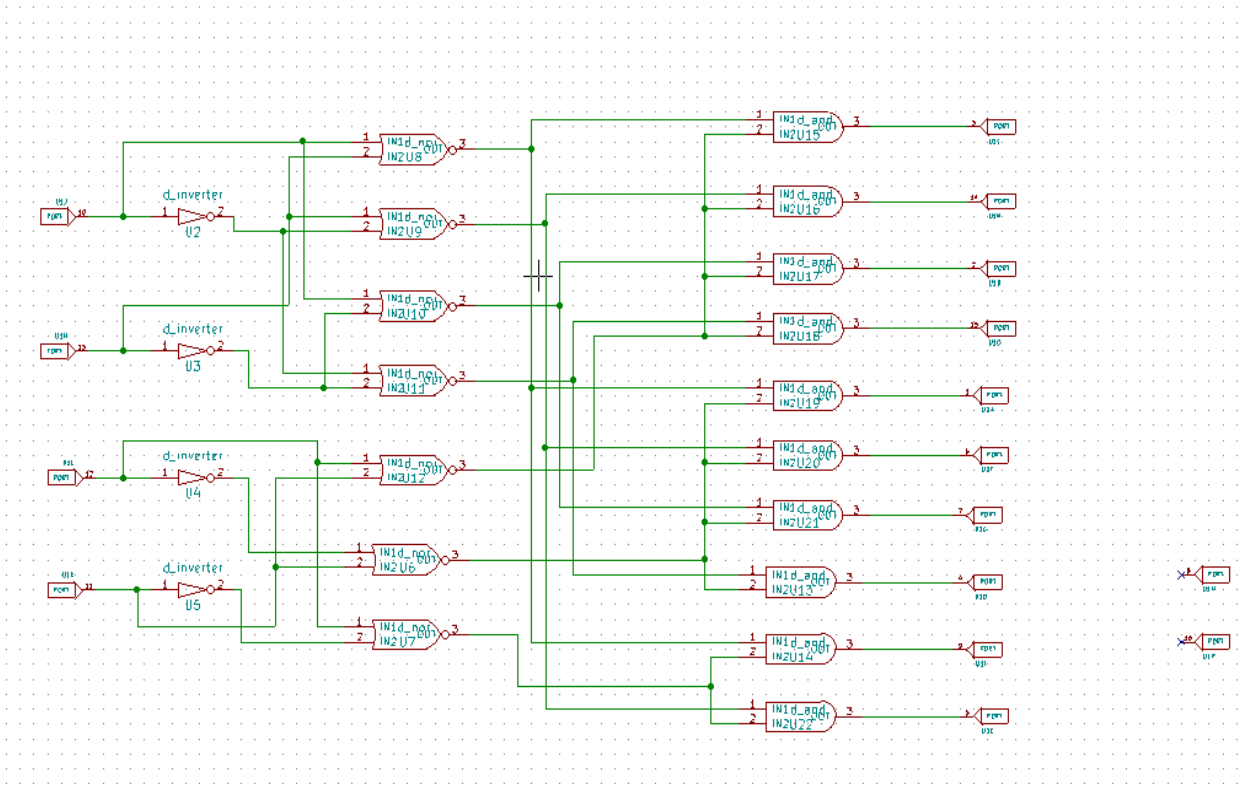

Figure 3.28: Subcircuit for 4028

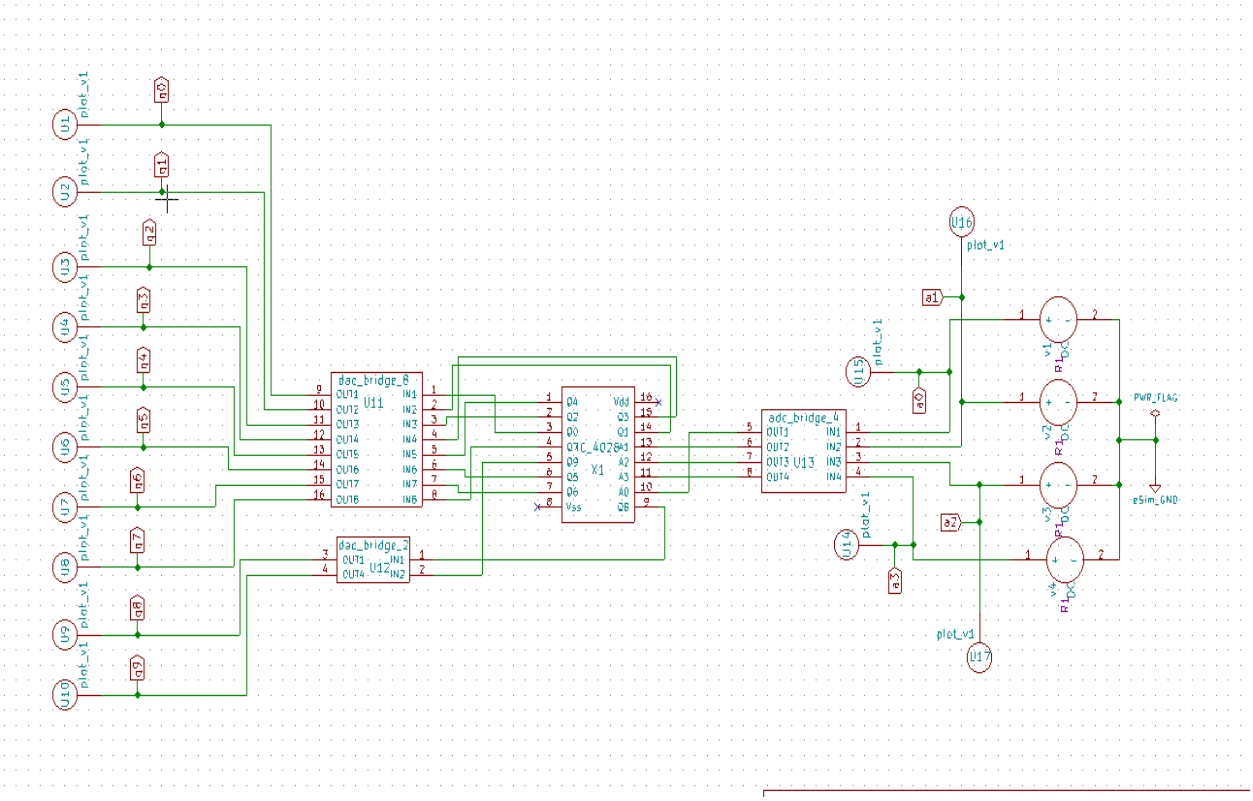

Figure 3.29: Test circuit for 4028

3.5.2 Ngspice Plots

Inputs and outputs are
[a3...a0]='0 0 1 0'
[q9.....q0]='0 0 0 0 0 0 0 0 1 0 0' i.e. q2 is high.
Input plots

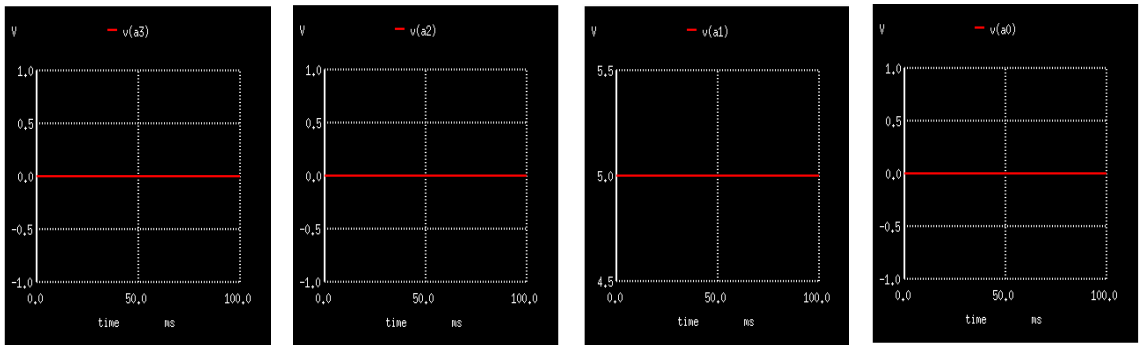

Figure 3.30: inputs [a3...a0]

Output plots

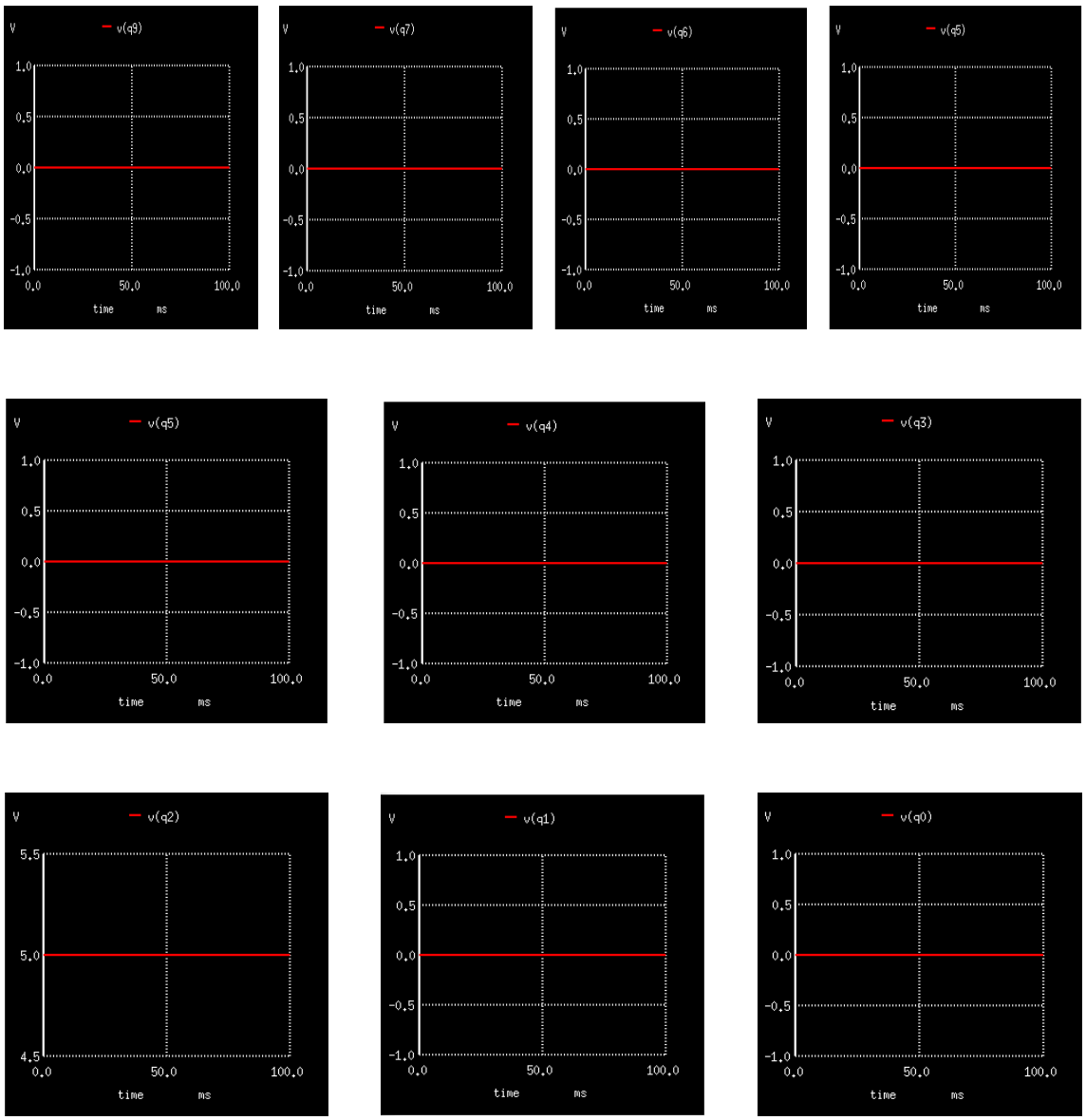

Figure 3.31: Outputs [Q9....Q0]

Reference:-https://www.renesas.com/us/en/www/doc/datasheet/cd4028bms.pdf

3.6 4073 IC

The 4073 is a member of the 4000 Series CMOS range, and contains three **independent AND gates**, each with three inputs. The pinout diagram, shown in Fig. 3.32, is the standard three-input CMOS logic gate IC layout. Here 4073 IC is named as **IC_4073** under **esim_Subcircuit.lib**

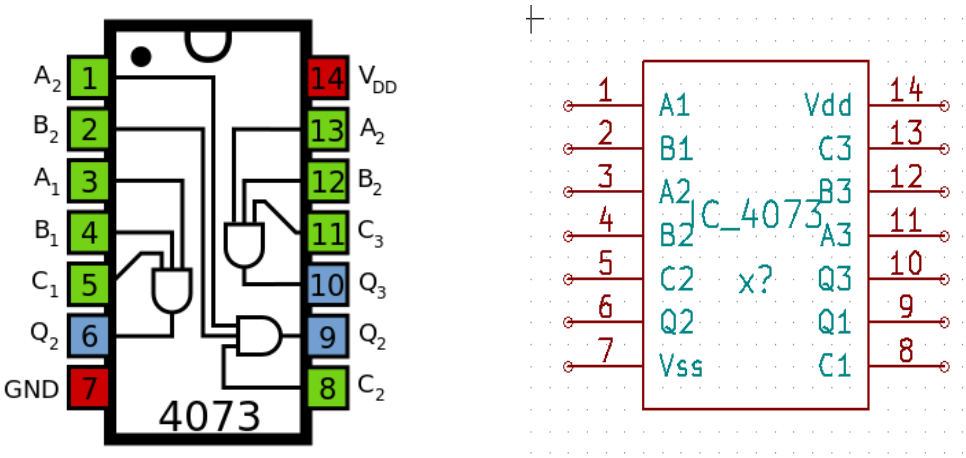

Figure 3.32: PIN Diagram of 4073 IC

3.6.1 Schematic Diagram

4073 IC subcircuit is shown in the Fig. 3.33 and test circuit for 4073 IC is shown in Fig. 3.34

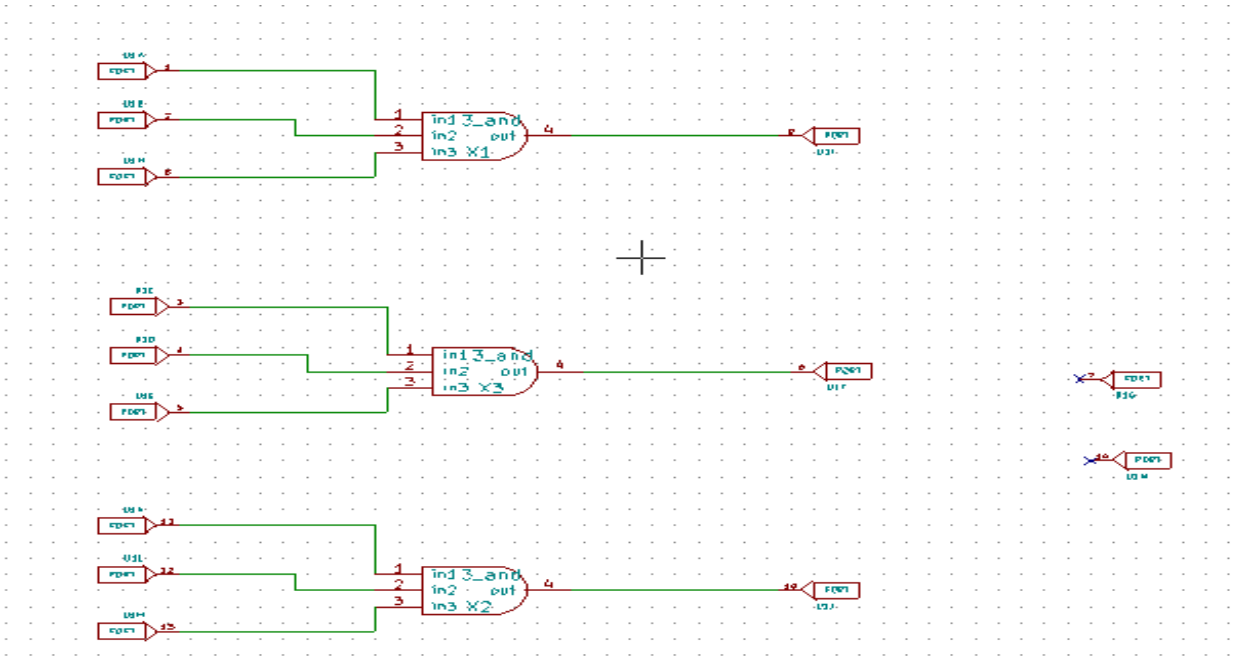

Figure 3.33: Subcircuit for 4073

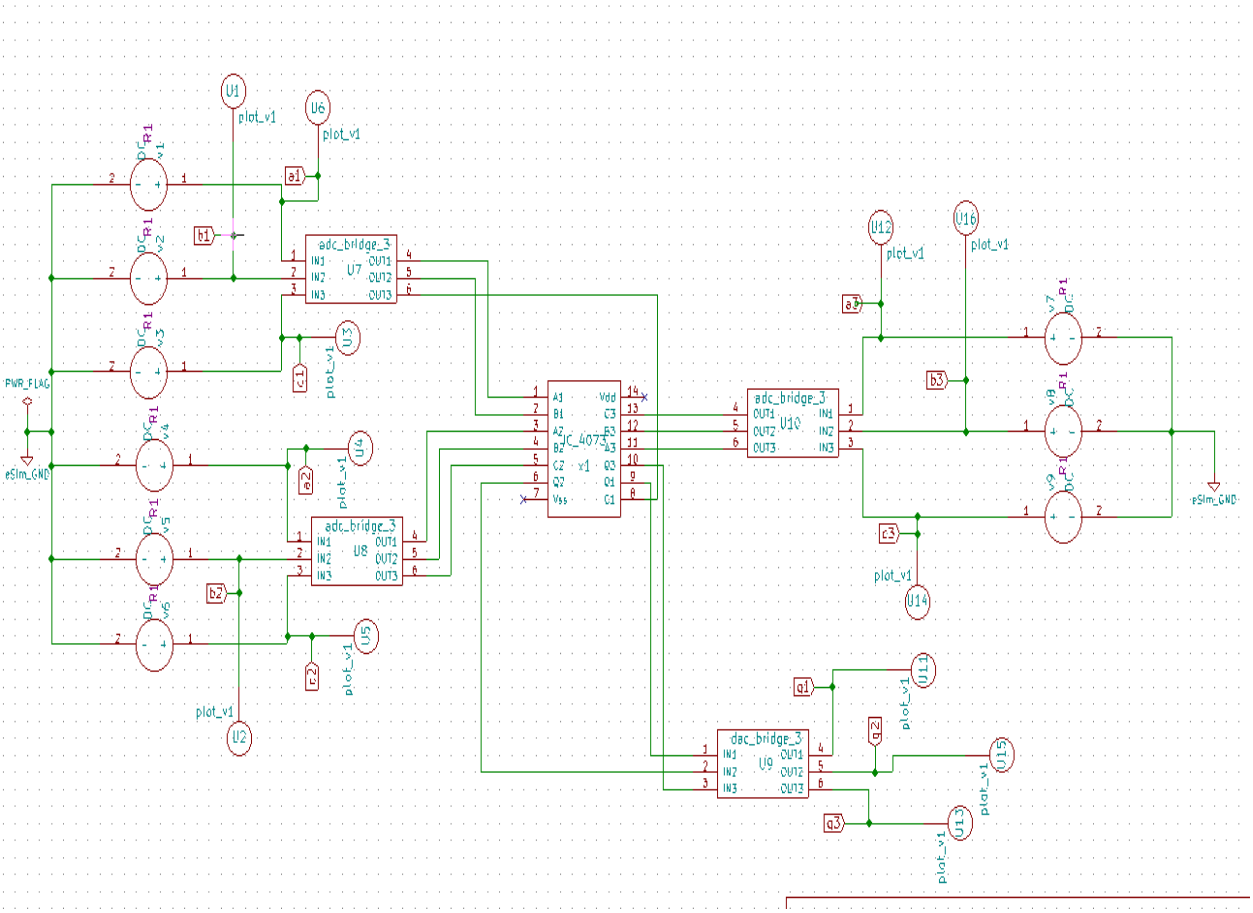

Figure 3.34: Test circuit for 4073

3.6.2 Ngspice Plots

Inputs and outputs are
a1= '1',b1= '1',c1='1' ==> q1='1'
a2= '0',b2= '1',c2= '0' ==> q2='0'
a3= '1',b3= '1',c3= '0' ==> q3='0'

Input Plots

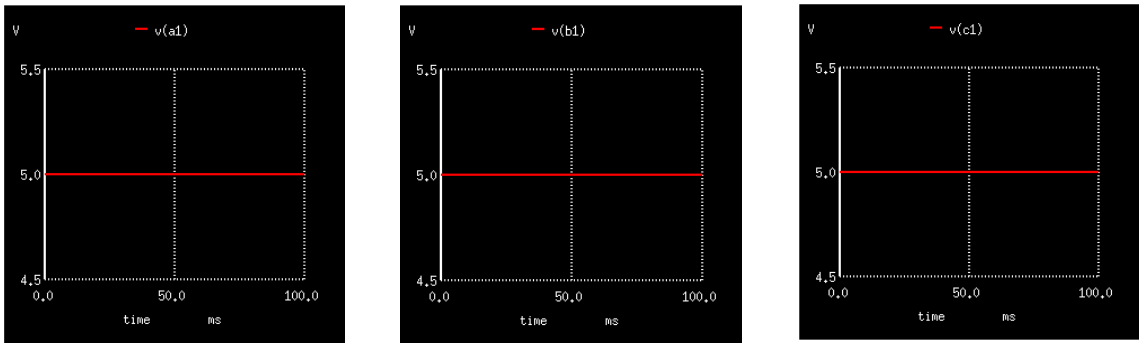

Figure 3.35: Inputs for And Gate 1

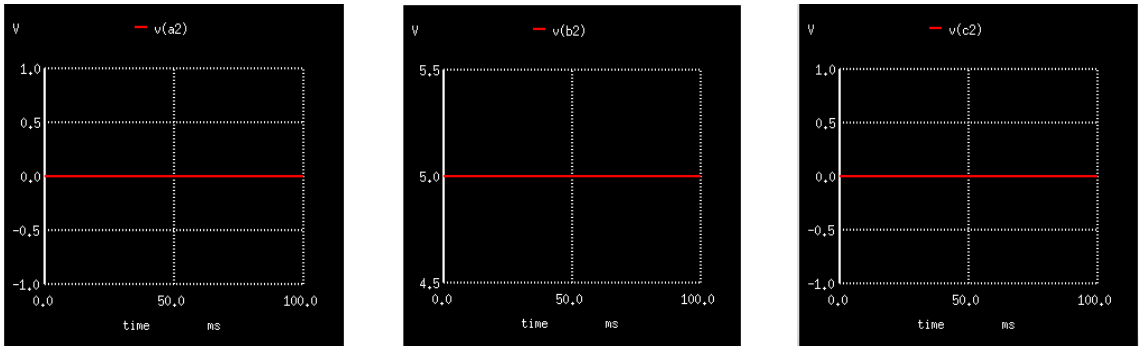

Figure 3.36: Inputs for And Gate 2

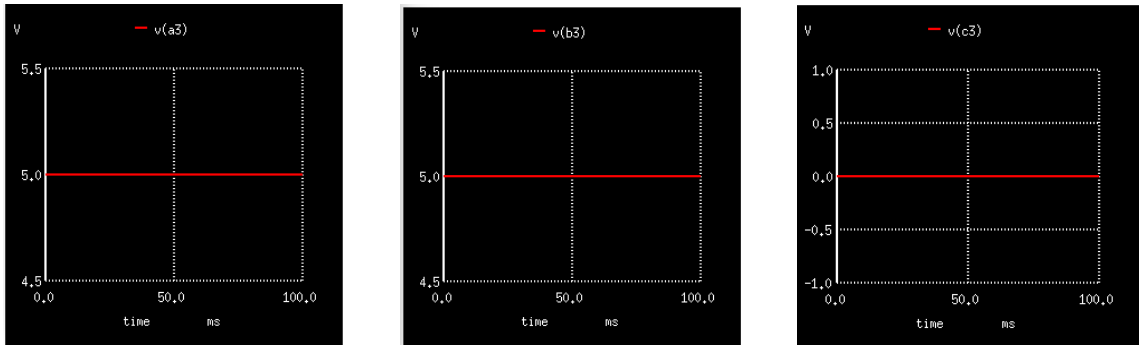

Figure 3.37: Inputs for And Gate 3

Output Plots

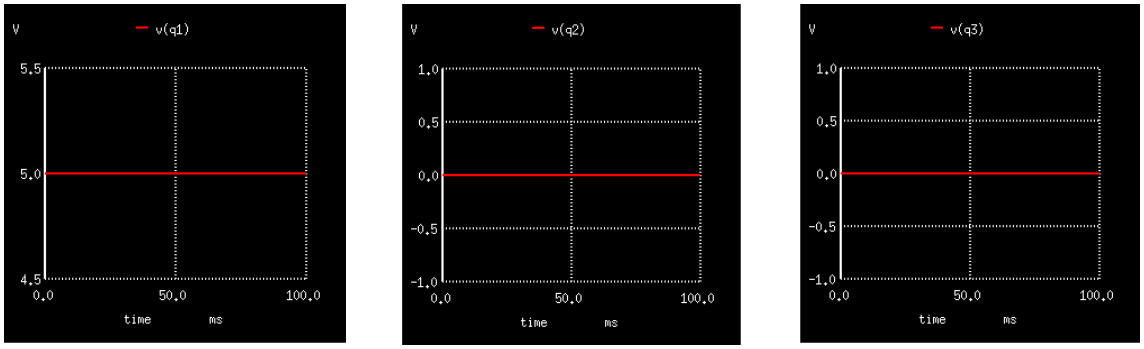

Figure 3.38: Outputs for And Gate 1 2 and 3

Reference:-http://www.ti.com/lit/ds/symlink/cd4073b.pdf

3.7 4072 IC

The 4072 is a member of the 4000 Series CMOS range, and contains two **independent OR gates**, each with four inputs. The pinout diagram, shown in Fig. **??**, is the standard three-input CMOS logic gate IC layout. Here 4072 IC is named as **IC_4072** under **esim_Subcircuit.lib**.

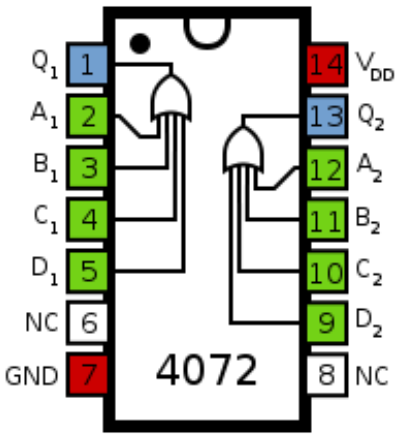

Figure 3.39: Pin Diagram of 4072 IC

3.7.1 Schematic Diagram

4072 IC subcircuit is shown in the Fig. 3.40 and test circuit for 4072 IC is shown in Fig. 3.41.
Reference: http://www.ti.com/lit/ds/symlink/cd4017b.pdf

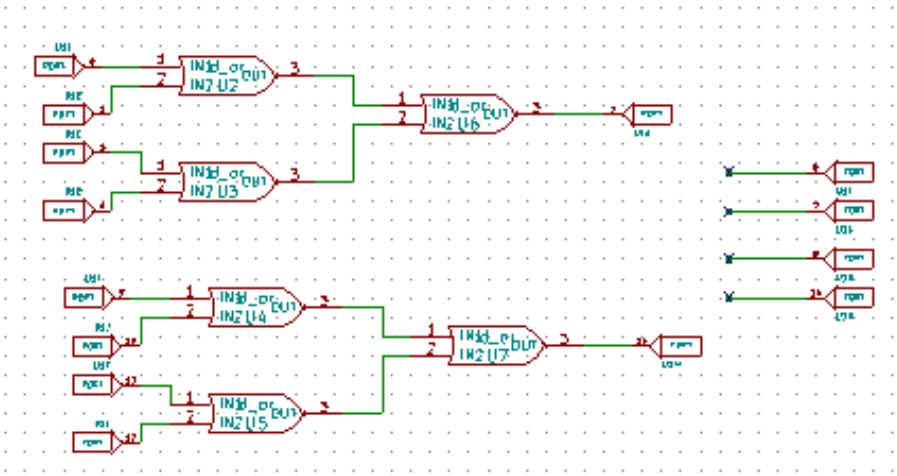

Figure 3.40: Subcircuit of 4072 IC

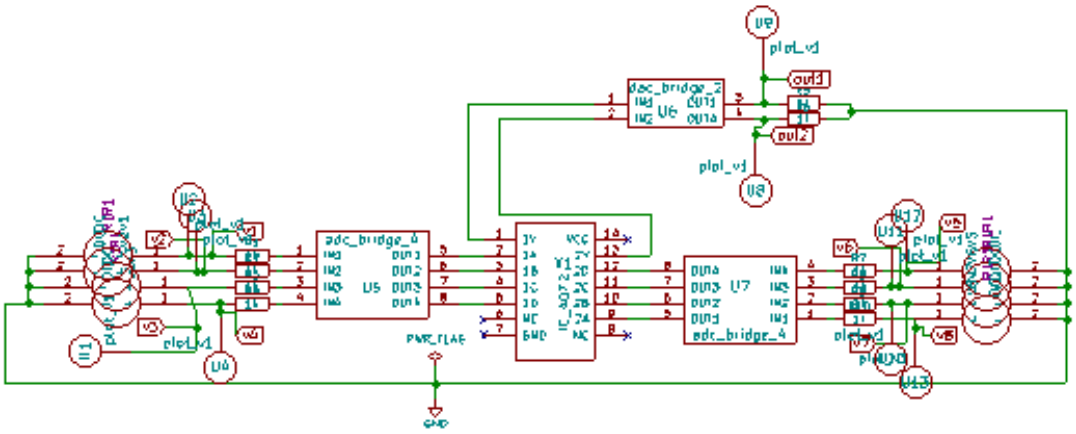

Figure 3.41: Testcircuit of 4072 IC

3.7.2 Ngspice Plots

Input Plots

Inputs are:
a0 =0;a1=0;a2=0;a3=0.Output y1:0.
b0 =0;b1=5;b2=0;b3=5.Output y2:5.

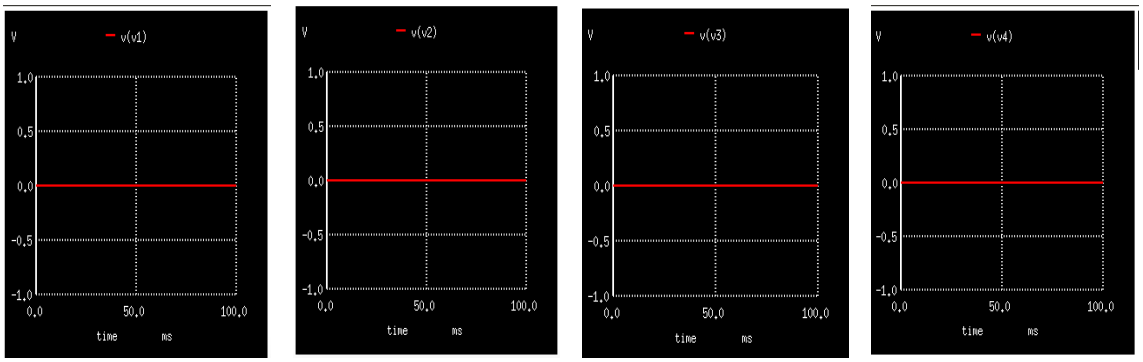

Figure 3.42: Inputs of OR Gate 1

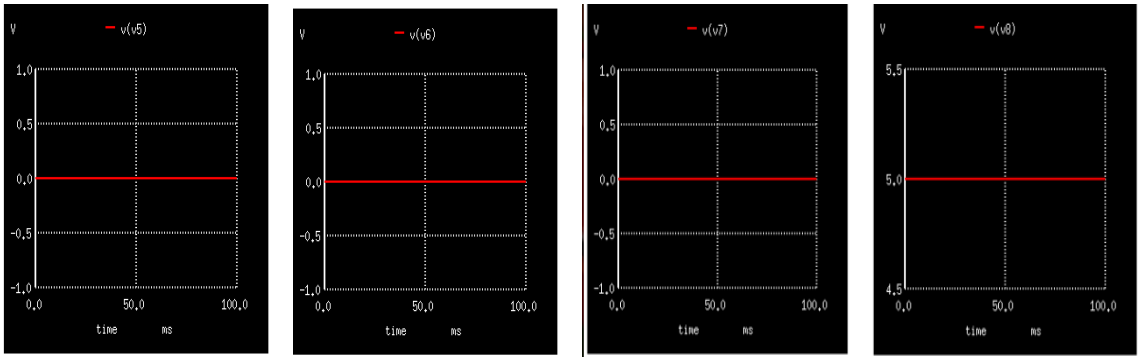

Figure 3.43: Inputs of OR Gate 2

Output Plots

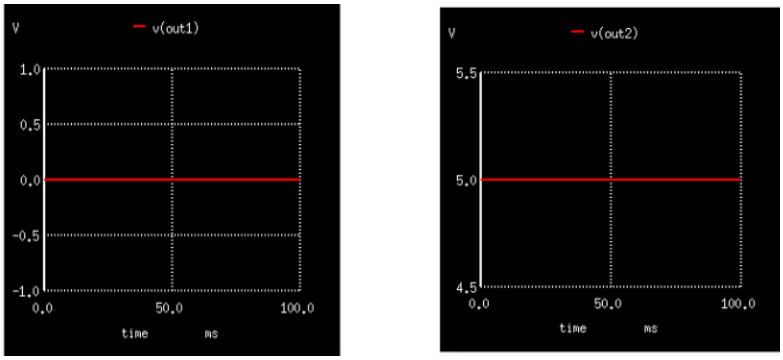

Figure 3.44: Outputs for Or Gates 1 & 2

3.8 4017 IC

4017 IC is a 5-stage Johnson counter having 10 decoder outputs.Inputs include CLOCK,RESET and CLOCK INHIBIT signal.Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times. The counter 4017 is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low.Counter advancement via the clock line is inhibited when CLOCK INHIBIT is high.A high RESET signal makes the counter clear to zero.
The pin diagram of 4017 IC is shown in Fig. 3.45 and added in eSim_Subckt library and named as IC_4017.
Reference: http://www.ti.com/lit/ds/symlink/cd4017b.pdf

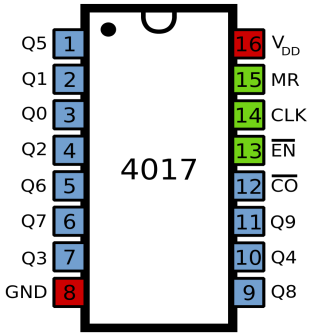

Figure 3.45: Pin Diagram of 4017 IC

3.8.1 Schematic Diagram

4017 IC subcircuit is shown in the Fig. 3.46 and test circuit for 4017 IC is shown in Fig. 3.47.

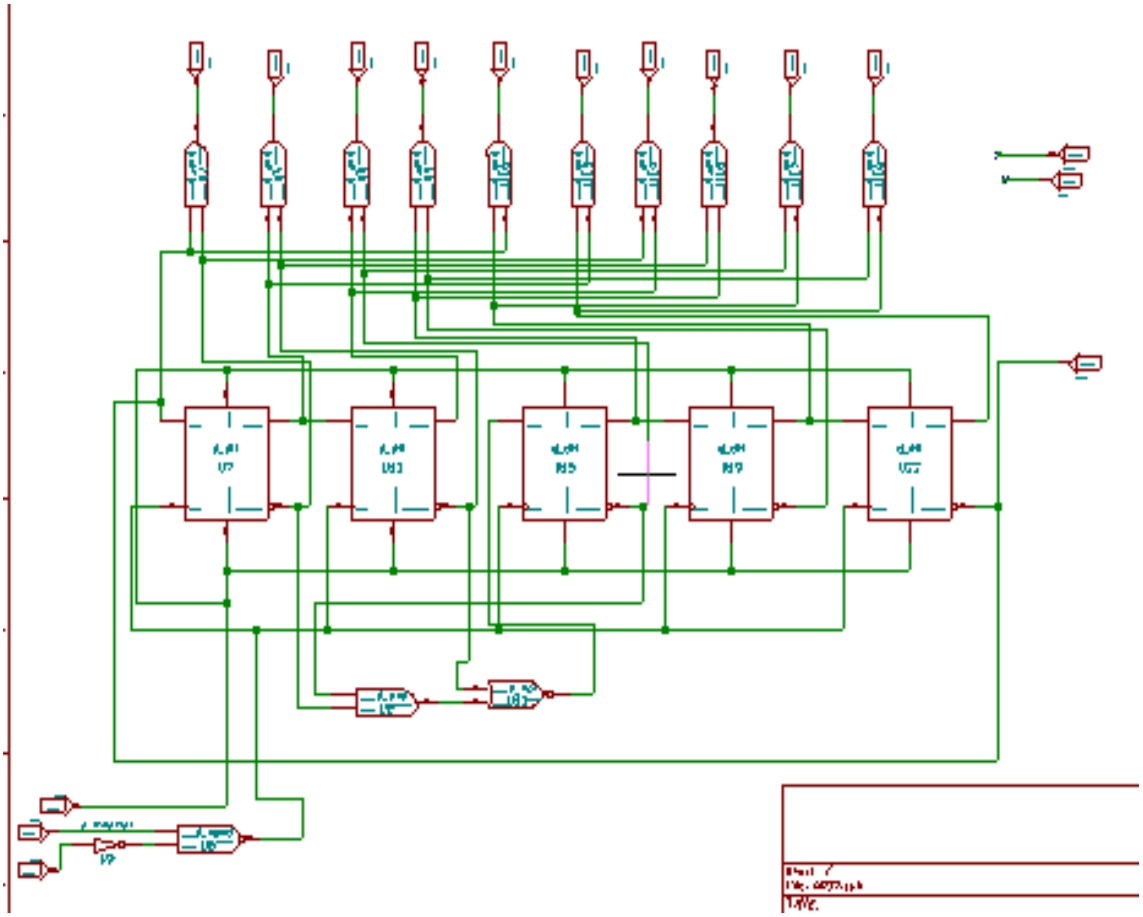

Figure 3.46: Subcircuit of 4017 IC

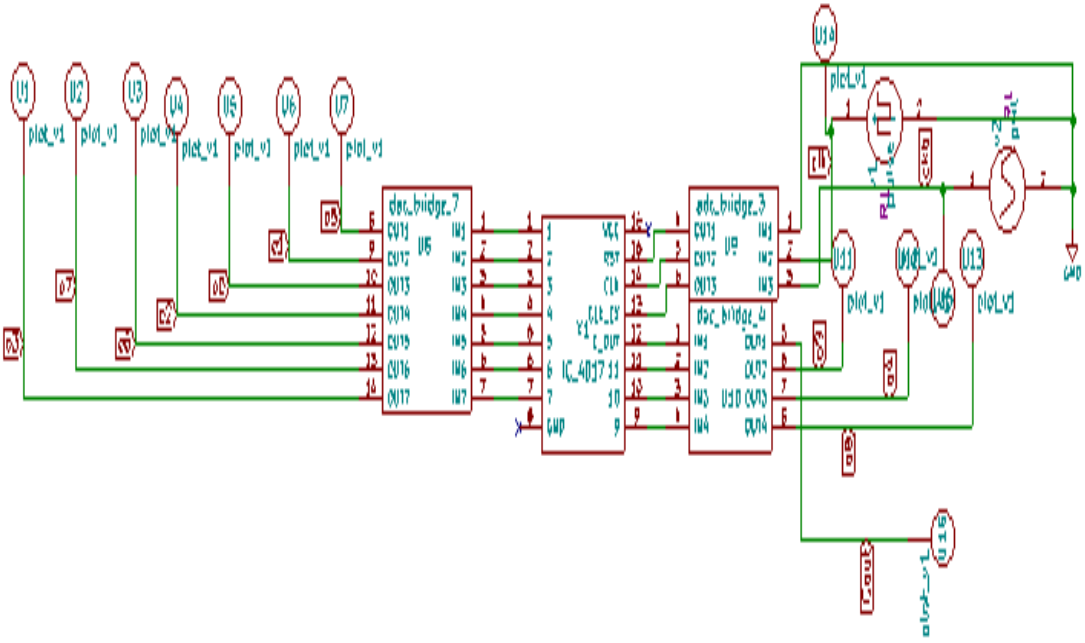

Figure 3.47: Test Circuit of 4017 IC

3.9 Ngspice Plots

Input Plots

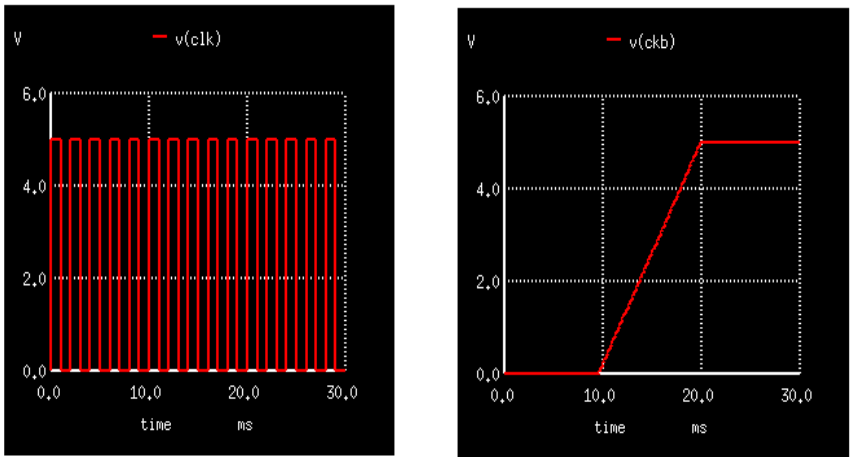

Figure 3.48: Inputs of CLOCK and CLOCK INHIBIT

Output Plots

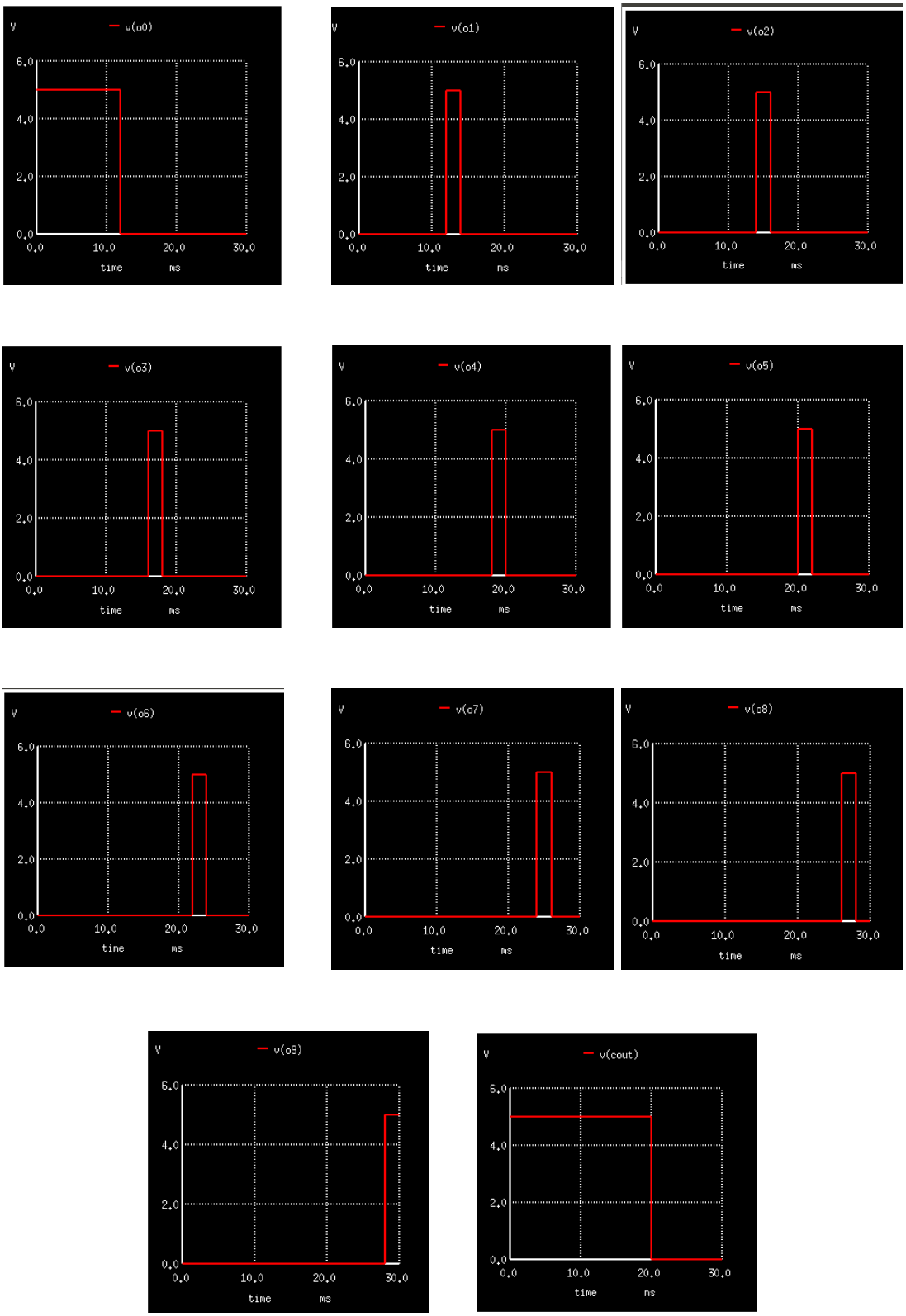

Figure 3.49: Output plots of 4017 IC

Chapter 4

Digital Models

4.1 D_RAM

The RAM model in the **eSim_digital** library has a size of (2^8X4) i.e. it has 8 address lines(A1...A8) and 4 data lines(4 input lines(DIN1...DIN4) and 4 output lines(DOUT1....DOUT4)). It also has 3 active high chip select lines (CS1,CS2,CS3) and a read/write enable pin(WR_EN).
For WRITE operation WR_EN ='0'
For READ operation WR_EN ='0'
The data should be first written into the RAM , then read operaton should be done ,otherwise without writing data ,if you try to read data from RAM ,there will be unknown values occur at the output lines. Most importantly depending on the binary values of (CS3 CS2 CS1),the select value in the ngspice model should be given(i.e. decimal value of (CS3 CS2 CS1)) while converting KiCAD to NGSPICE. For example , if CS3 = '1' , CS2 = '1' , CS1 = '0',
select value = 6 . You can see this in the Fig. 4.2.In the Fig. 4.2 select value = 7 i.e. [CS3..CS1]='111' .

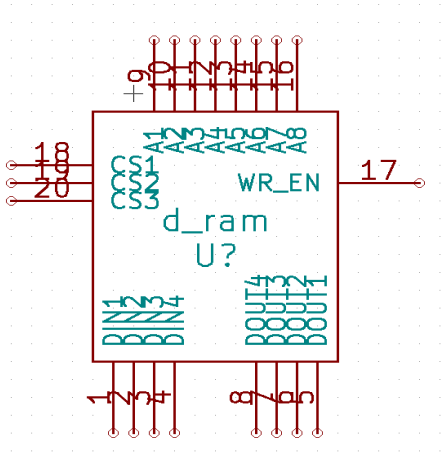

Figure 4.1: pin diagram for d_ram

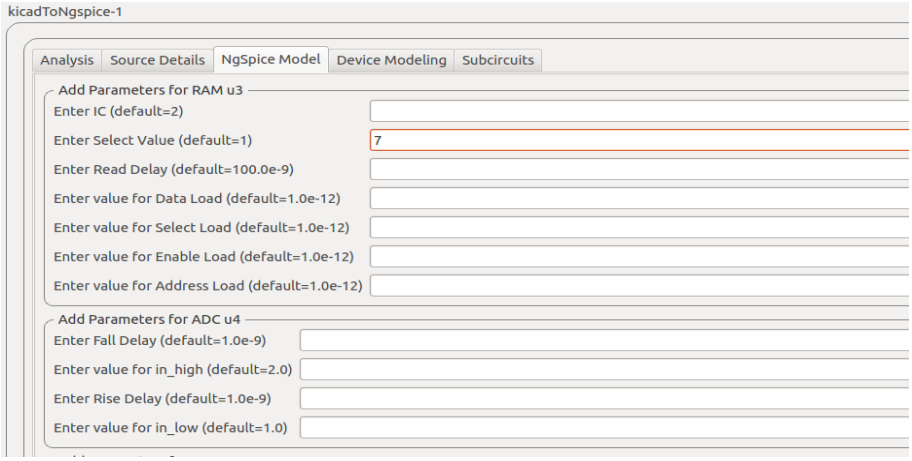

Figure 4.2: Kicad to Ngspice window

4.1.1 Schmatic Diagram

The test circuit for d_ram is shown in the figure below

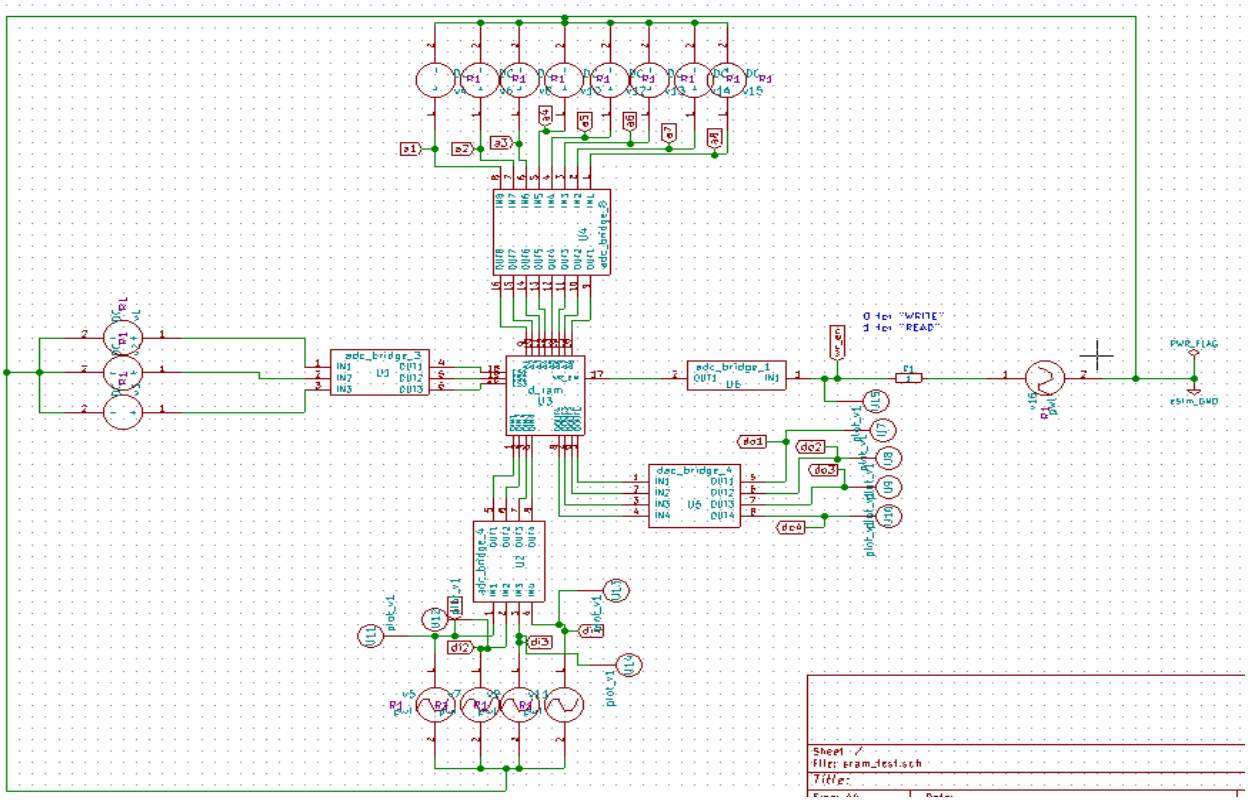

Figure 4.3: d_ram test circuit

4.1.2 Ngspice Plots

In the test circuit above Address lines [A1....A8]= '00001111', The plots for data input lines are shown in the Fig. 4.4 From 0 to 4ms DIN1='1' DIN1='0' DIN1='1'

DIN1=’0’ From 4 to 8ms DIN1=’0’ DIN1=’1’ DIN1=’0’ DIN1=’1’

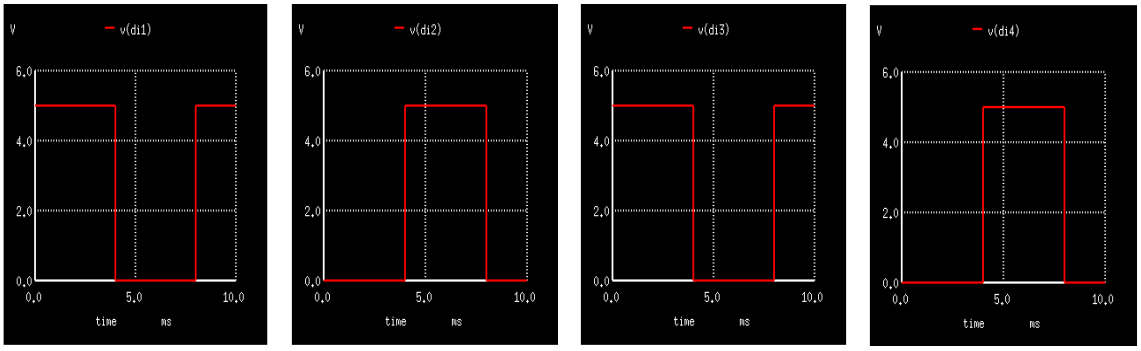

Figure 4.4: Data input lines for [DIN1...DIN4]

The plot for WR_EN pin shown in the Fig. 4.5 In this case

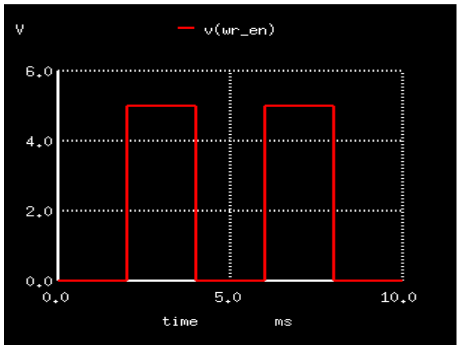

Figure 4.5: plot for WR_EN

From 0ms to 2 ms data will be written into the RAM
From 2 ms to 4 ms data will be read from the RAM
From 4ms to 6 ms data will be written into the RAM
From 6 ms to 8 ms data will be read from the RAM

Output Plots

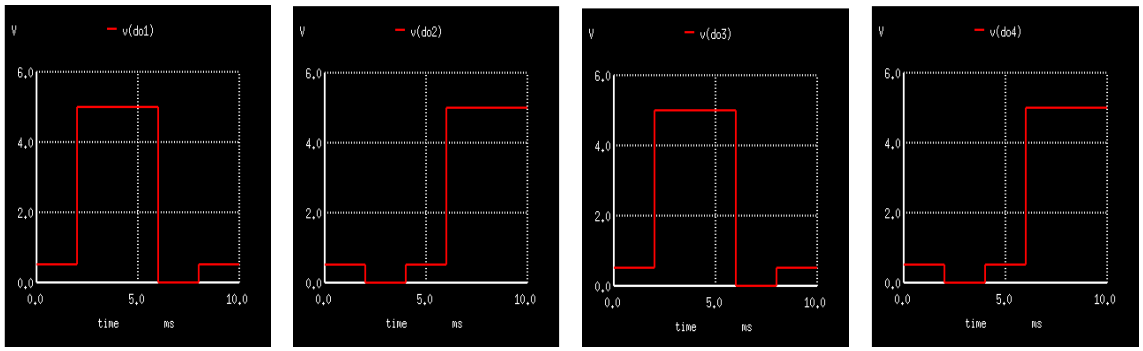

Figure 4.6: Data output lines for [DOUT1...DOUT4]

For first 2 ms data is write into the RAM so the output from 0ms to 2ms is UNKNOWN values (dont care)

From 2ms to 4ms data is read from the RAM we get the outputs
From 4ms to 6ms ,again data is write into the RAM so the output from 4ms to 6ms is UNKNOWN values (dont care)
From 2ms to 4ms data is read from the RAM we get the outputs

4.2 D_PULL UP/DOWN

Digital Pull up and Down are predefined ngspice models which makes the pin value High and Low respectively.
When pull up is connected to a pin it makes the pin to **high** and similarly by connecting pull down to a pin it makes the pin **low**.
It is a digital value and no need to use analog to digital converter. These models are present in eSim_Digital library.The shape of pull up and down are shown in Fig. 4.9

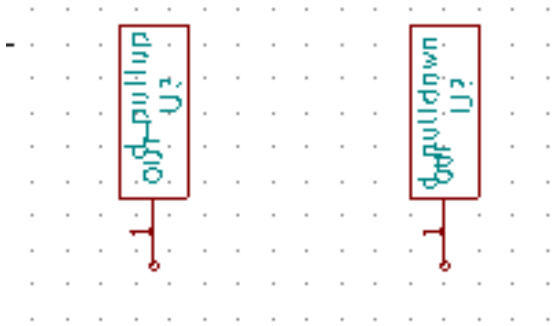

Figure 4.7: Diagrams of Pull up and Down

4.2.1 Schematic Diagram

The example for pull up and down are shown in the Fig. 4.8.In this a two input and gate is connected to pull up and pull down .So the inputs are **1 and 0** So we will get the output **'0'**.
Reference: http://ngspice.sourceforge.net/docs/ngspice-manual.pdf

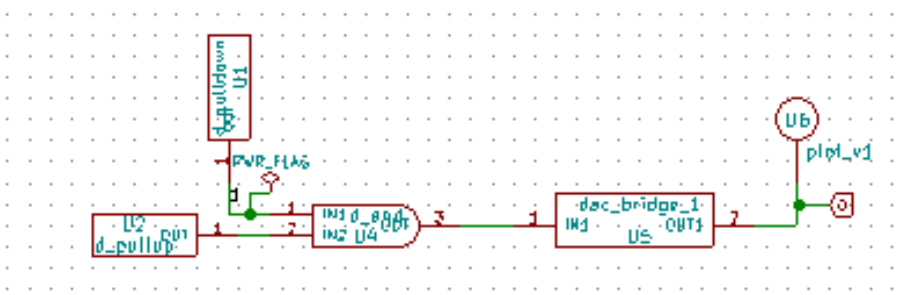

Figure 4.8: Example of Pull up and Down

4.2.2 Ngspice Plots

Output Plots

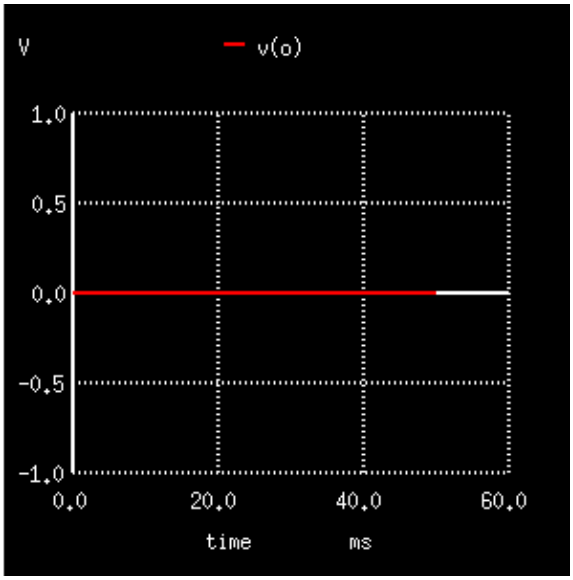

Figure 4.9: Output Plot

4.3 D_SOURCE

d_source is a digital source present in the **esim_digital** library. It has 4 digital sources.The pin diagram of d_source is shown in the Fig. 4.10

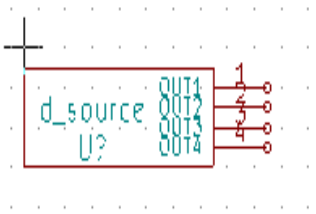

Figure 4.10: pin diagram for d_source

In order to use d_source ,you should create a text file which acts as the input file for d_source.The format of the text file is shown in the table 4.1.Then you should paste the text file in the **project directory** in the **esim-workspace**.

The first column indicates the time ,time should be monotonically increasing down the column.

Second column refers to the outputs of **dout1** for the corresponding times in the time column.

Similarly 3^{rd} column refers to **dout2**, 4^{th} column refers to **dout3**,5^{th} column refers to **dout4**

The values 1s corresponds to binary 1 and 0s corresponds to binary 0

*time	dout1	dout2	dout3	dout4
0.00e-3	1s	1s	0s	1s
1.00e-3	0s	1s	1s	0s
5.00e-3	0s	0s	1s	0s
7.00e-3	1s	0s	1s	1s
8.00e-3	1s	1s	1s	0s
9.00e-3	0s	1s	1s	1s

Table 4.1: text format for d_source

Note :- While converting Kicad to Ngspice , the filename of the text file should be entered in the Ngspice model of the d_source between the double quotation marks. An example is shown in the Fig. 4.11.Here file name is **m_source.txt**

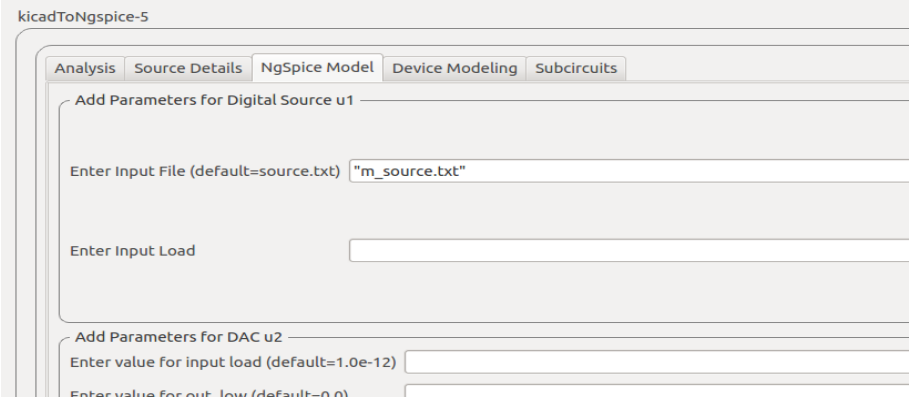

Figure 4.11: Kicad to Ngspice converter

4.3.1 Schematic Diagram

The test circuit schematic for d_source is shown in the Fig. 4.12.

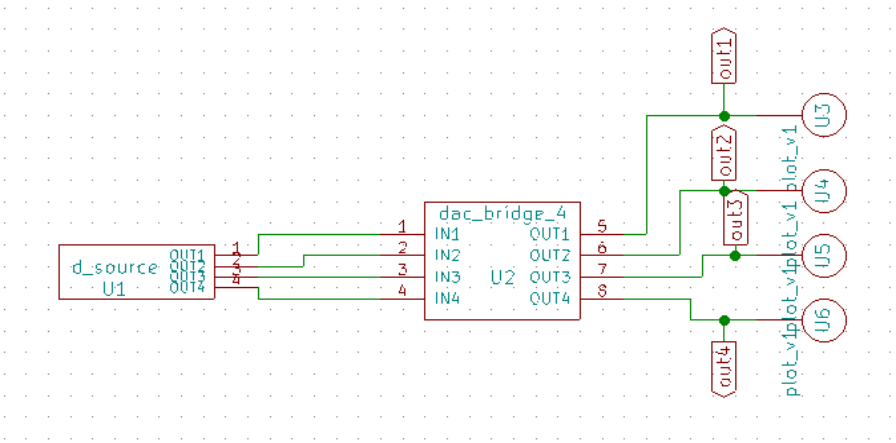

Figure 4.12: Test circuit for d_source

4.3.2 Ngspice Plots

The four Output plots of the d_source is shown in the Fig. 4.13.

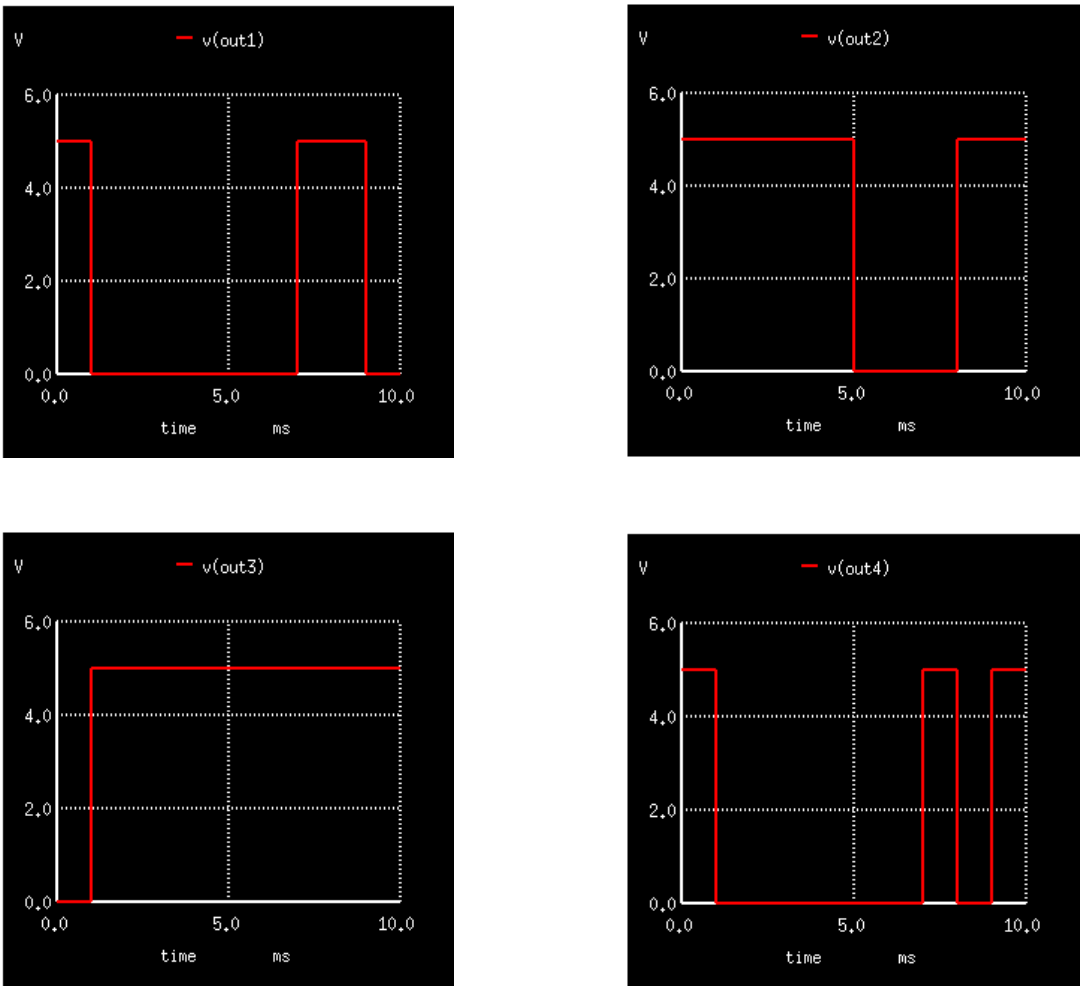

Figure 4.13: Output plots of d_source

Chapter 5

NGHDL Feature

This feature converts VHDL code to Ngspice format.B y using Ngspice Format we can simulate the circuit and can plot the circuits.
We need to run VHDL file in NGHDL which is present in eSim Interface.After succesfull running the component footprint is saved in eSim_Kicad library.We need to add the library file from Component Library Option and need to draw the schematic to simulate.
This feature works only for single output and later with the help of CSE people it was modified and can work upto 64 outputs.
Limitations
Every element(input,outputs and signals) in VHDL code should declare as vector.
We need to define every input or output separately.
We can't use single element in a vector (n downto 0) but we can use the full vector at a same time.
The maximum number of outputs allowed are 64.
We need to close the Xterm Window before simulating other cases otherwise we will face Infinite loop.
The names of inputs and outputs in VHDL code should not be same for different examples.
Can't able to use Structural Style.
Arthematic operations are not possible in this feature.

5.0.1 Working of NGHDL

First we need to write VHDL code and save the file.
We need to compile VHDL code to find the errors.The comand to compile is **ghdl -s filename.vhdl** in the Terminal in working directory.
Now we need to open eSim and click NGHDL option which is present on left side.A window will open and it was shown in Fig. 5.1We need to Browse the file and click Upload.

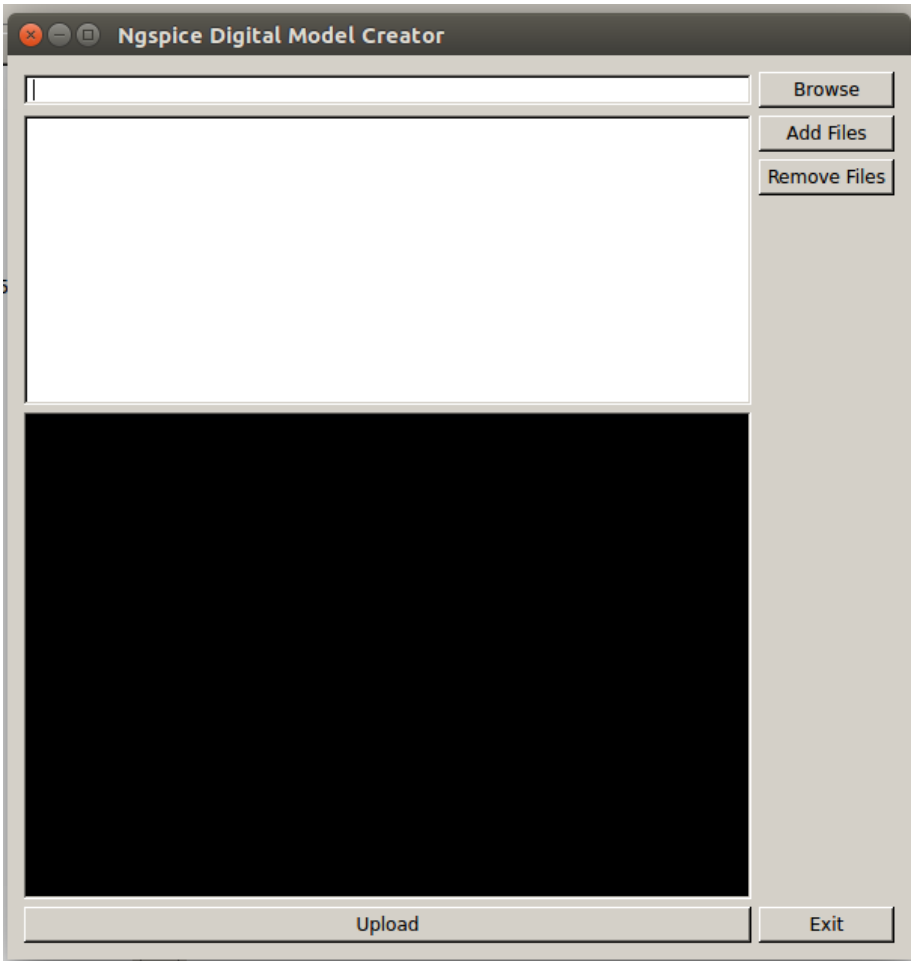

Figure 5.1: NGHDL Interface

After successful conversion We will find a message that model successfully added in eSim_Kicad.lib library and it was shown in Fig. 5.2

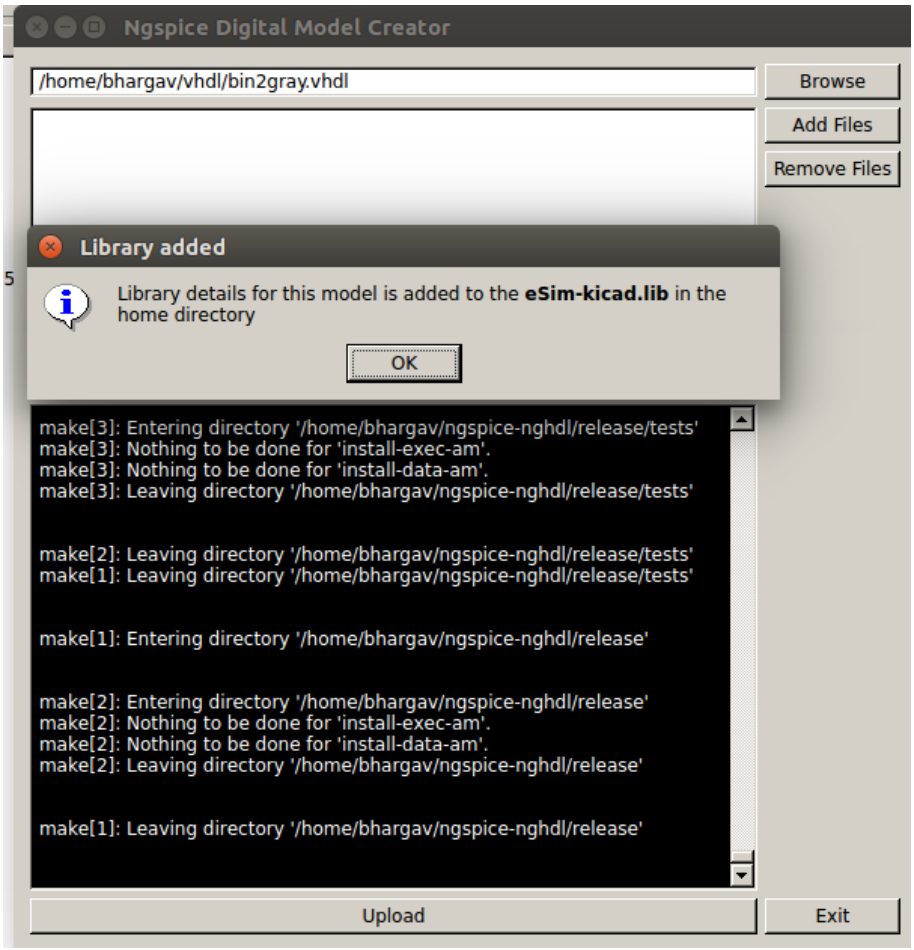

Figure 5.2: Conformation Box

Now we need to create a new project and open EEshema and we need to same process which we did for doing simulation.

5.0.2 Example Circuit

Example for Binary to Gray Code Converter VHDL code:
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

entity bin2gray is
port(bin3 : in std_logic_vector(0 downto 0);
bin2 : in std_logic_vector(0 downto 0);
bin1 : in std_logic_vector(0 downto 0);
bin0 : in std_logic_vector(0 downto 0);
G3 : out std_logic_vector(0 downto 0);
G2 : out std_logic_vector(0 downto 0);
G1 : out std_logic_vector(0 downto 0);

G0 : out std_logic_vector(0 downto 0));
end bin2gray;

architecture gate_level of bin2gray is

begin

G3 ¡= bin3;
G2 ¡= bin3 xor bin2;
G1 ¡= bin2 xor bin1;
G0 ¡= bin1 xor bin0;
end;
The schematic diagram of binary to gray converter is shown in Fig. 5.3

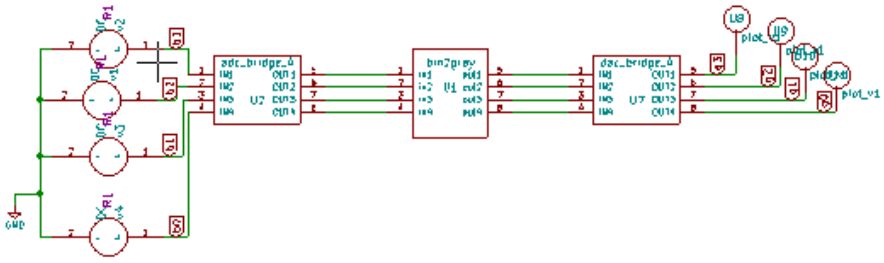

Figure 5.3: Schematic Diagram

5.0.3 Ngspice Plots

Input Plots

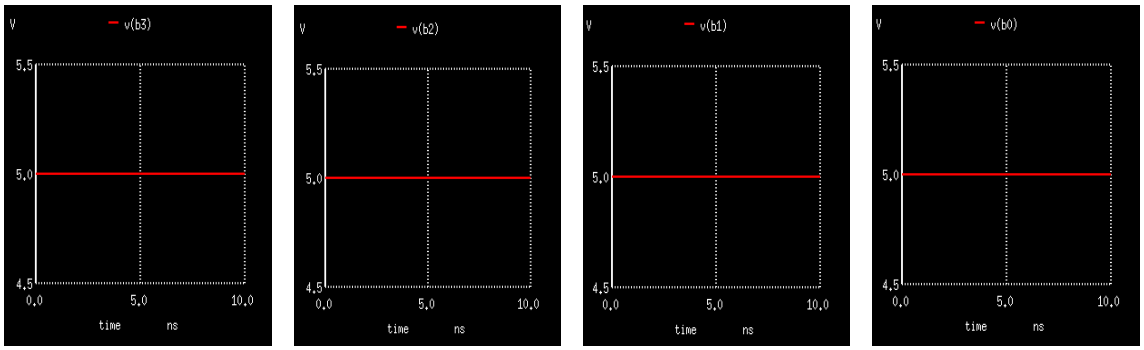

Figure 5.4: Input Values

Output Plots

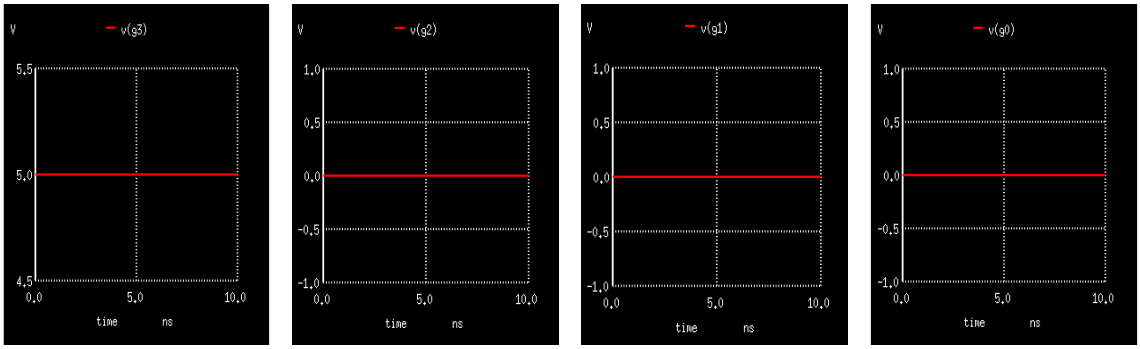

Figure 5.5: Output Values

Reference

- https://github.com/FOSSEE/eSim/pull/115