Summer Fellowship Report

On

Subcircuits in eSim

Submitted by

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Under the guidance of

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October 11, 2022

Acknowledgment

We would like to express our gratefulness to the FOSSEE team for giving us a wonderful and learning experience.

We are extremely thankful to Prof. Kannan M. Moudgalya for guiding and motivating us throughout the FOSSEE fellowship programme.[1]

We would like to thank the eSim [2] team for helping us and providing us all the resources required to work with and guiding us all throughout the project. We are also thankful to our mentors Mr. Sumanto Kar, Mr. Rahul Paknikar, Mr. Nagesh Karmali, Mrs. Madhuri Kadam, Prof. Inderjit Singh Dhanjal, Mrs. Usha Vishwanathan and whole team for the immense support and valuable advices. Their presence and their hard work for us day and night had made our fellowship experience blissful. Moreover, we never forget our fellow friends for assisting us with their fantastic knowledge and superb skills. The work environment is fully energetic and friendly.

We would utilize everything we got from here for our career growth as well as for the betterment of our society.

Contents

Chapter 1

Introduction

FOSSEE [1] (Free/Libre and Open Source Software for Education) project promotes the use of FLOSS tools to improve the quality of education in our country. It aims to reduce dependency on proprietary software in educational institutions. It encourages the use of FLOSS tools through various activities to ensure commercial software is replaced by equivalent FLOSS tools. It also develops new FLOSS tools and upgrade existing tools to meet requirements in academia and research.

The FOSSEE project is part of the National Mission on Education through Information and Communication Technology (ICT), Ministry of Human Resource Development (MHRD), Government of India.

eSim is a free/libre and open source EDA tool for circuit design, simulation, analysis and PCB design developed by FOSSEE, IIT Bombay. It is an integrated tool built using free/libre and open source software such as KiCad, Ngspice, NGHDL and GHDL. eSim is released under GPL.

eSim [2] offers similar capabilities and ease of use as any equivalent proprietary software for schematic creation, simulation and PCB design, without having to pay a huge amount of money to procure licenses. Hence it can be an affordable alternative to educational institutions and SMEs. It can serve as an alternative to commercially available/licensed software tools like OrCAD, Xpedition and HSPICE.

Chapter 2

Problem Statement

To design and develop various Analog and Digital Integrated Circuit Models in the form of sub-circuits using device model files already present in the eSim library. These IC models should be useful in the future for circuit designing purposes by developers & users, once they get successfully integrated into the eSim subcircuit Library.

2.1 Approach

Given below is the flowchart of our used approach as the solution.

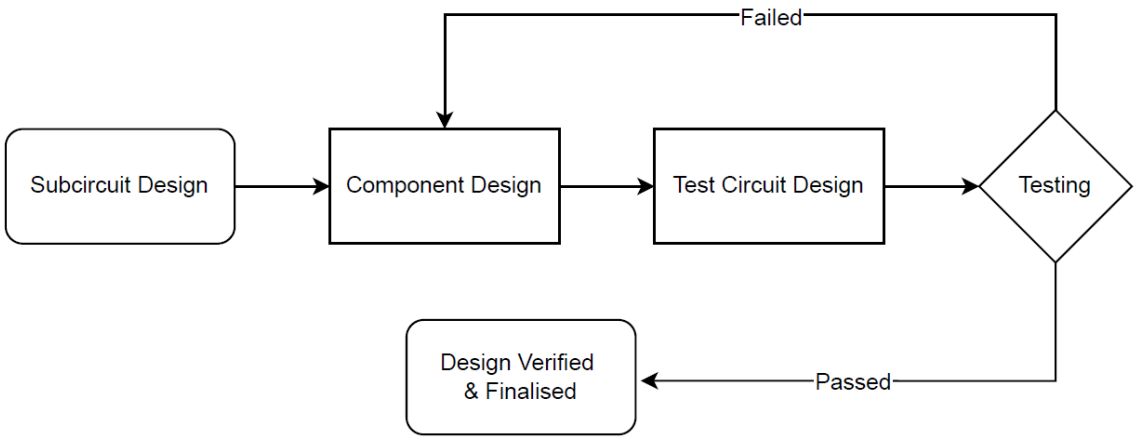

Figure 2.1: Flow chart of the Methodology used

- **Subcircuit Design phase :** This is the first design step in our adopted approach. In this step, we identify the basic ICs which are not yet available in eSim. After deciding the IC, we start modeling it as a sub-circuit in eSim, using the model files present in the eSim device model library only. The design is strictly according to the information given in the official data-sheets of the ICs.

- **Component Design phase :** In this step, we have built the component/ Symbol/Pin diagram of the IC according to the packaging & pin description given in the data-sheets only.
- **Test Circuit Design phase :** Once the component of the IC is ready, now we can build the test circuits, according to the data-sheets. In this step we build the test cases & test circuits using the component IC.
- **Testing phase :** Once the test circuits are ready, now it's time to simulate the test circuits so that the output can be obtained in the form of wave-forms & plots. Here we take help of KiCad to NgSpice conversion & Simulation feature in eSim.

If the output of the test circuit is not as per expectation, this means that the test case has failed. In such case we go back to design phase of the IC or the test circuits, to look for possible errors; and then repeat the testing process again after making required changes.

If the expected output of the test cases are correct and satisfies the expected results, then in that case the IC is declared working & verified. The test case has passed successfully and the designing process is complete.

Chapter 3

Software Requirements

3.1 eSim

As discussed earier, eSim [2] (previously known as Oscad / FreeEDA) is a free/libre and open source EDA tool for circuit design, simulation, analysis and PCB design.This simulation software works fine on both Windows and Linux Operating Systems. There are many installer version of eSim application. eSim is created using open source software packages, such as KiCad, Ngspice and Python. Using eSim, one can create circuit schematics, perform simulations and design PCB layouts. It can create or edit new device models, and create or edit subcircuits for simulation. Because of these reasons, eSim is expected to be useful for students, teachers and another professionals who would want to study and/or design electronic systems.In eSim there are many tools. For subcircuit building there is an icon named subcircuit. With the help of this subcircuit can be made easily. There is also netlist generator button, KiCad to NgSice coverter and Simulation button to check or test the designed IC is working as expected or not.

Chapter 4

Analog ICs

4.1 LM7809 Voltage Regulator IC

In practical circuits voltage sources in a circuit may have fluctuations resulting in not providing fixed voltage outputs. A voltage regulator IC maintains the output voltage at a constant value. 7809 IC [3], a member of 78xx series of fixed linear voltage regulators used to maintain fixed voltage, is a popular voltage regulator integrated circuit (IC). It gives 9 volts constant output voltage.

4.2 Pin Configuration

The TO-220 IC configuration is shown below.

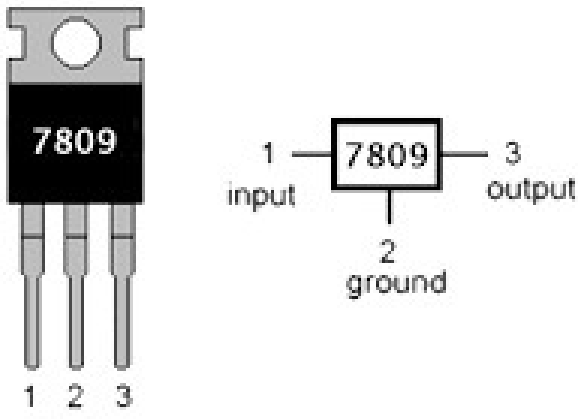

Figure 4.1: CD4001 Pin Configuration

4.3 Subcircuit Schematic Diagram

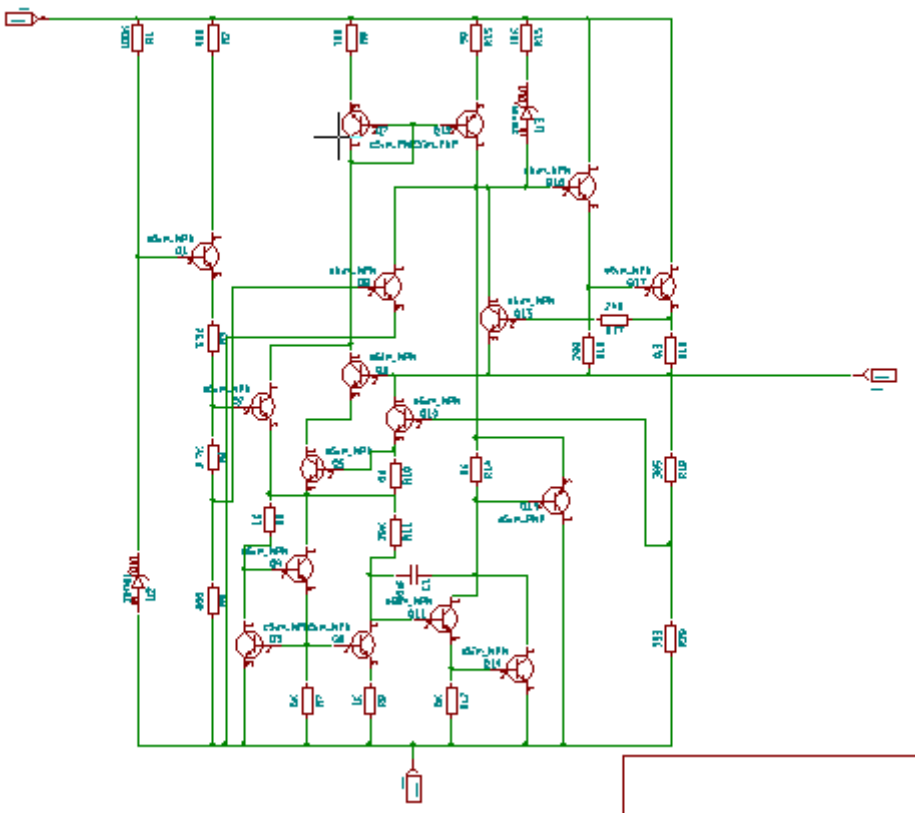

Figure 4.2: LM7809 Subcircuit Schematic Diagram

4.4 Schematic with external circuit

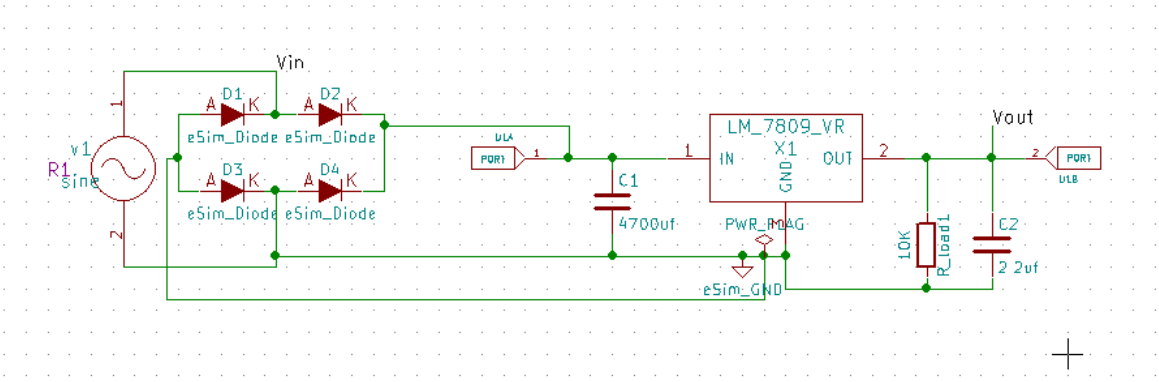

Figure 4.3: Voltage regulator with Bridge Rectifier

4.5 Ngspice Plots

4.5.1 Input plot

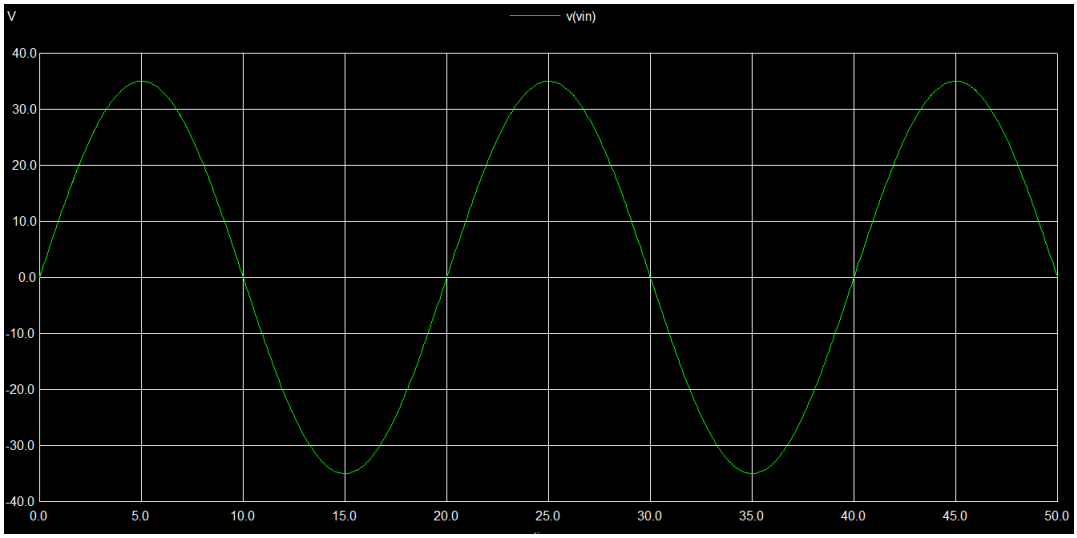

Figure 4.4: Input Sine wave

4.5.2 Output plot

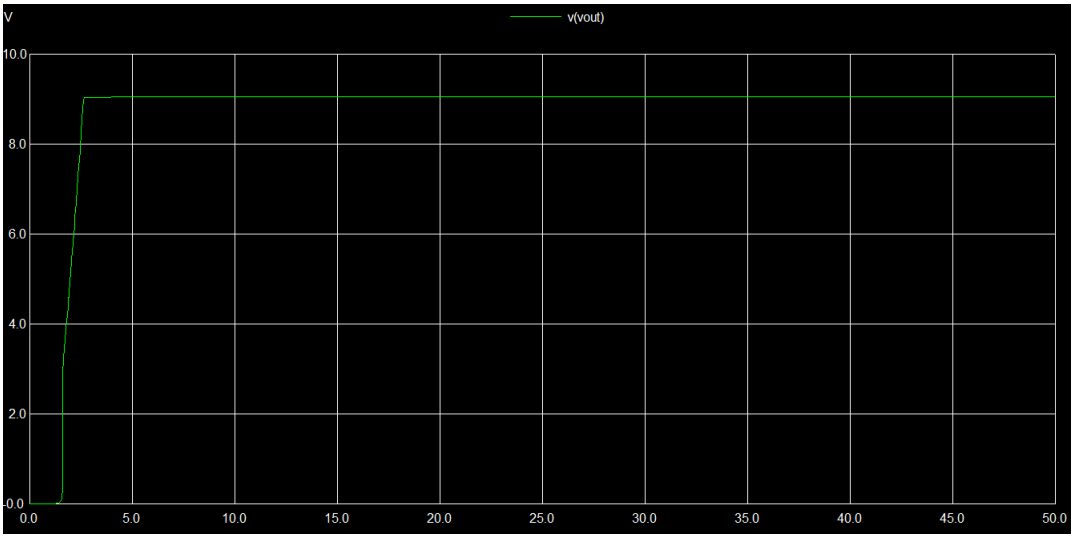

Figure 4.5: DC Output

4.6 LM386 Amplifier IC

It is power amplifier IC [4] designed for use in low voltage consumer applications. It is used in various field of electronics applications like Radio amplifier, TV sound systems, power converter etc. The gain of the IC can be varied from 20 to 200. Though the gain 20 is set internally, using some changes in external circuit the gain would be increased nicely.

4.7 Pin Configuration

The pinout diagram is shown in fig. 4.6.

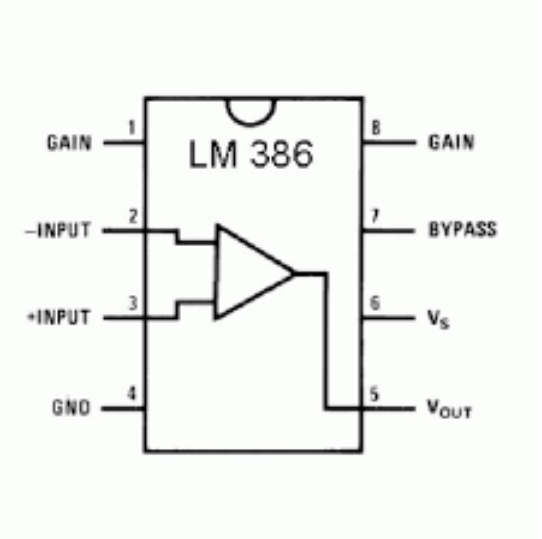

Figure 4.6: INA106 Pin Configuration

4.8 Subcircuit Schematic Diagram

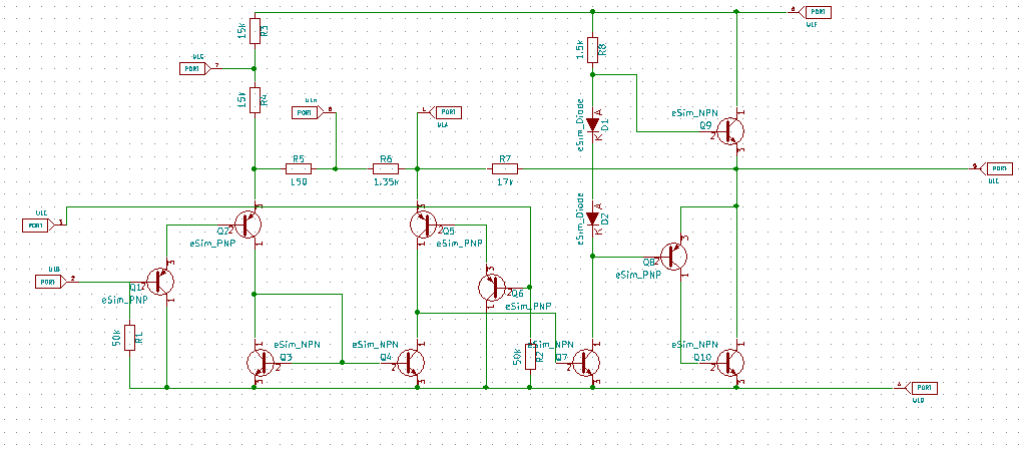

Figure 4.7: INA106 Subcircuit Schematic Diagram

4.9 Schematic with external circuit

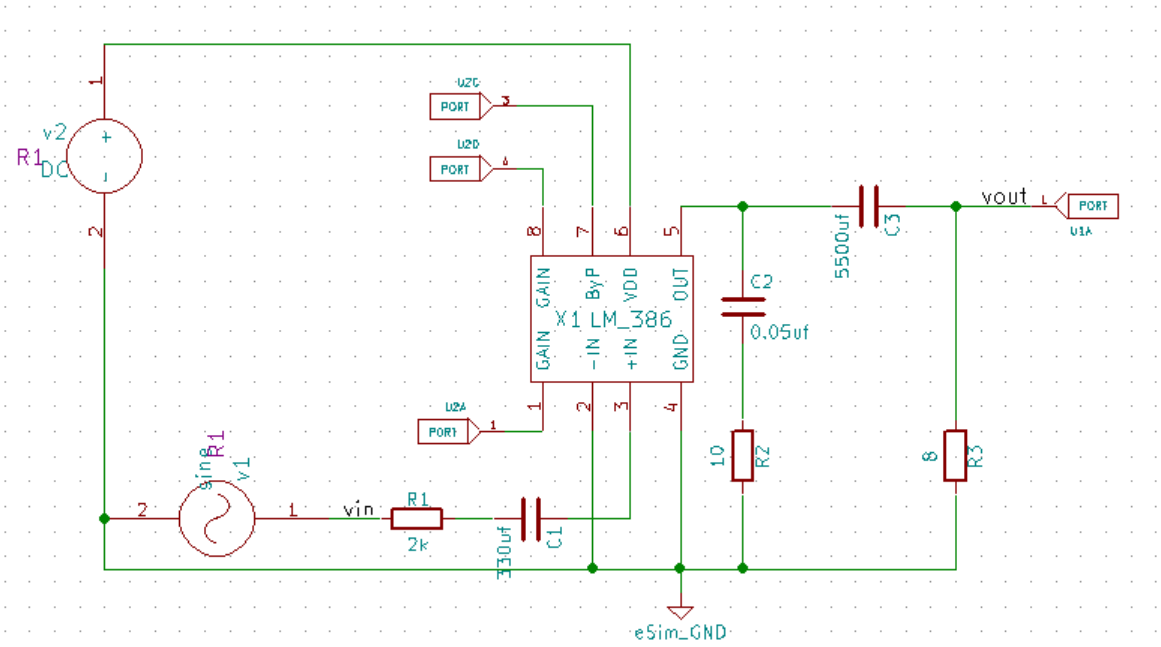

Figure 4.8: Non-Inverting Amplifier with Gain 20

4.10 Ngspice Plots

4.10.1 Input plot

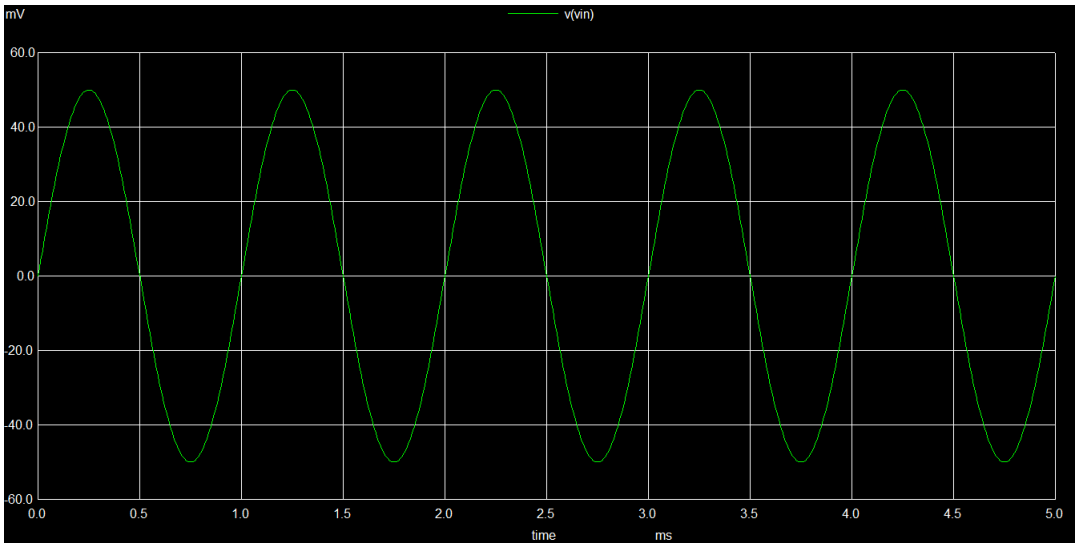

Figure 4.9: Input Sine wave

4.10.2 Output plot

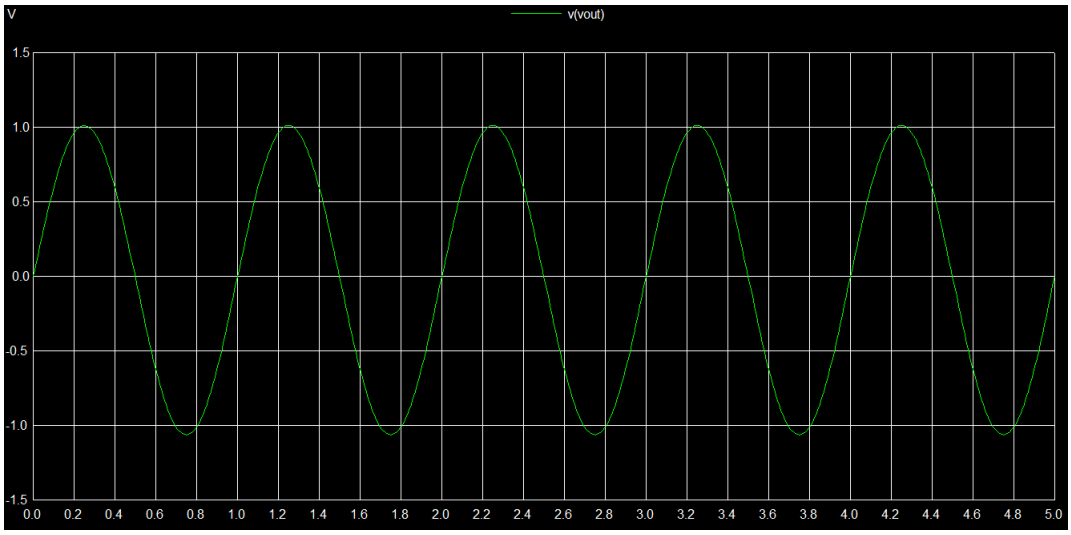

Figure 4.10: Gained output

4.11 AD620 Instrumentation Amplifier IC

AD620 [5] is a low cost and high gain instrumentation amplifier IC has many usage in real life applications like medical in instruments, battery powered devices, ECG machine etc. One can vary the gain from 1 to 1000 by changing only one external resistance value. Gain has an inverse relation with the external resistor.
Note: In our design for high gain as 500,1000 observed reduction in gain due to leakage current of LM741 op-amp IC used in the subcircuit design. But one can get high gain by keeping external resistor too low.

4.12 Pin Configuration

It is available in 8-pin DIP IC.

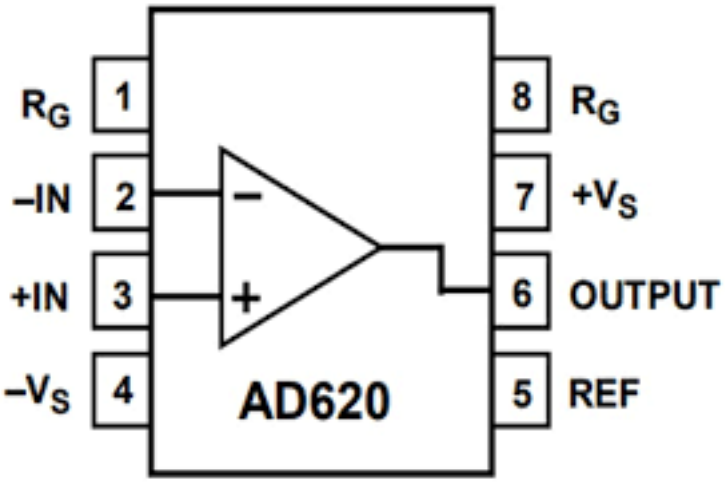

Figure 4.11: AD620 Pin Configuration

4.13 Subcircuit Schematic Diagram

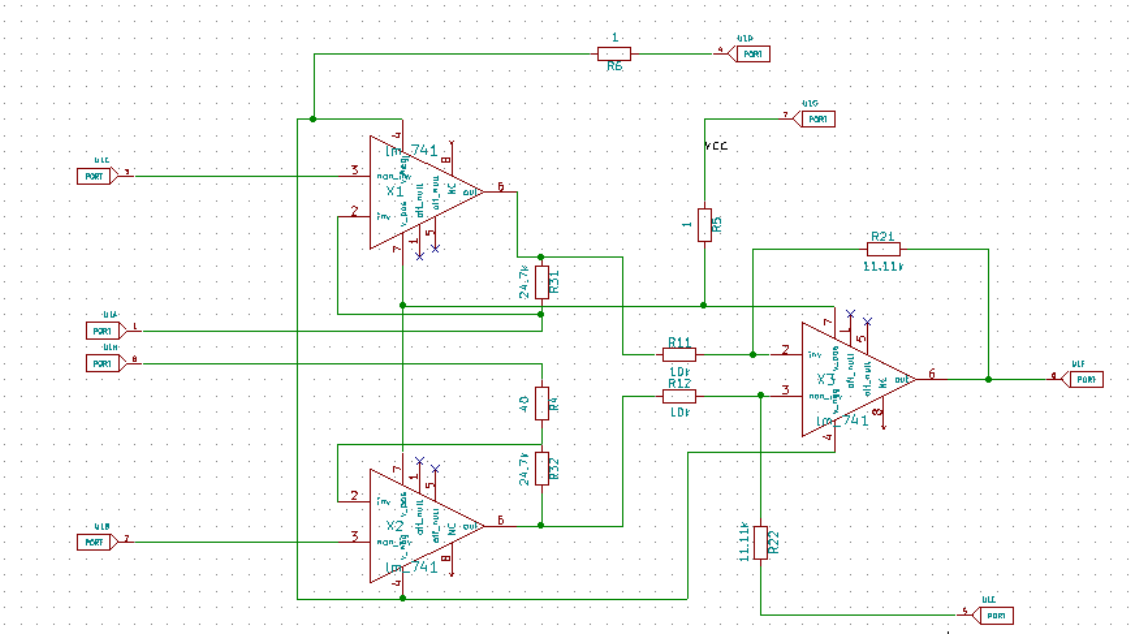

Figure 4.12: AD620 Subcircuit Schematic Diagram

4.14 Schematic with external circuit

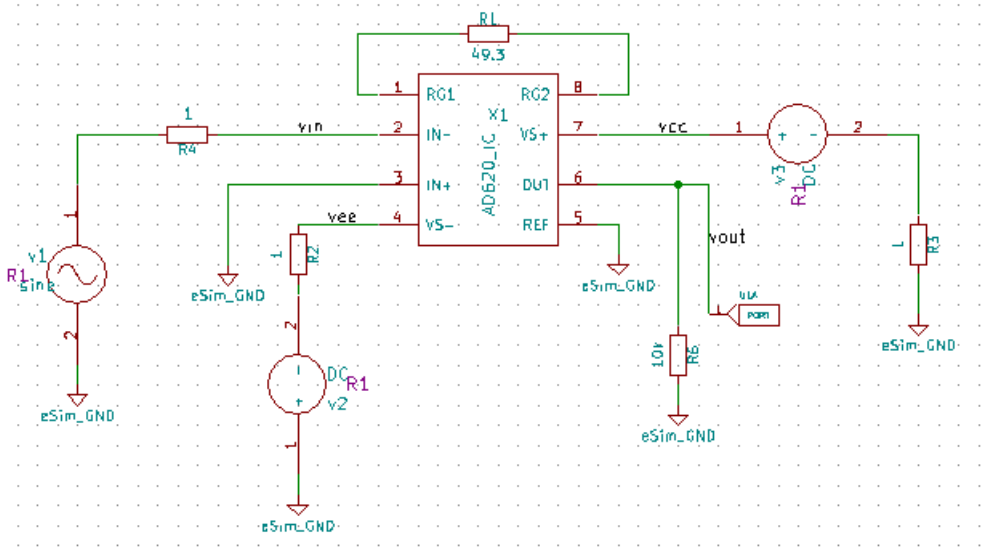

Figure 4.13: Instrumentation Amplifier with Gain 10

4.15 Ngspice Plots

4.15.1 Input plot

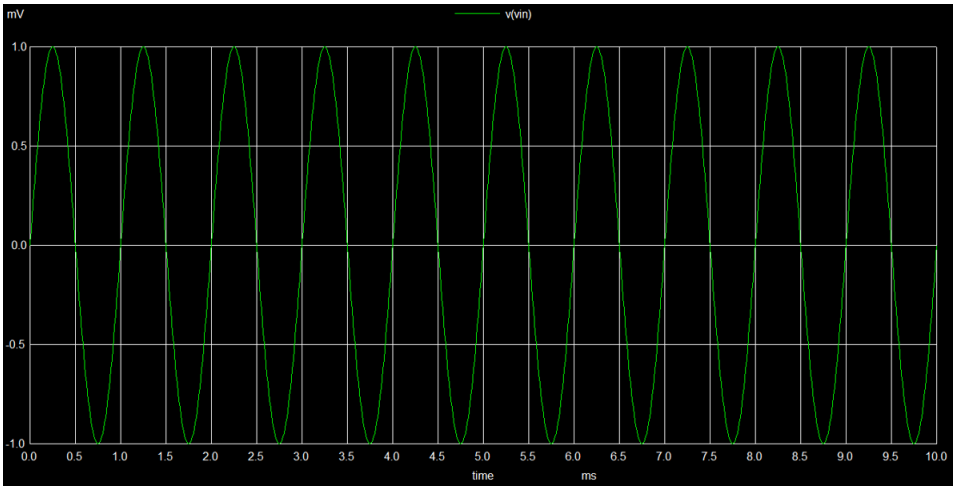

Figure 4.14: Input Sine wave

4.15.2 Output plot

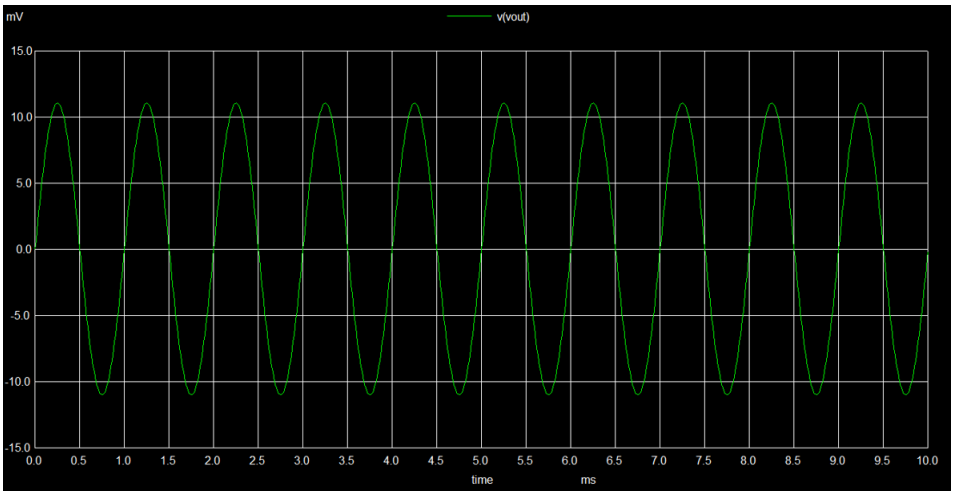

Figure 4.15: Gained output

4.16 INA106 Differential Amplifier IC

Differential Amplifier is a type of amplifier circuit which is used to amplify the difference of input and give the output respectively.

4.17 Pin Configuration

It is an 8 pins IC [6] with pin name REF, -IN, +IN , V- , Sense , Vout , V+ , NC. It is an analog circuit which takes two input and give the difference of both inputs at the output.

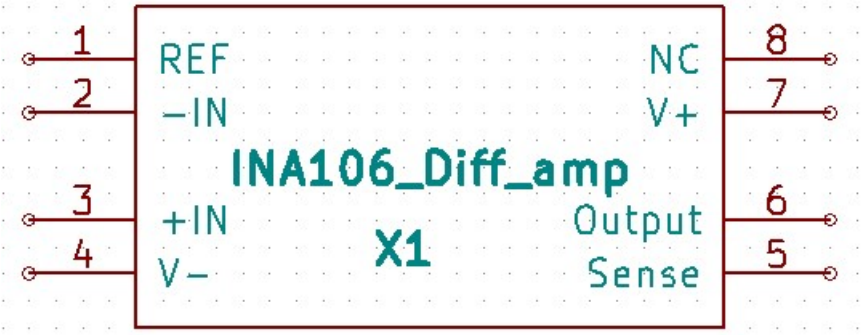

Figure 4.16: INA106 Pin Configuration

The mathematical equation for calculating the output is given as
Vout=Ad(Vin1-Vin2)
Where,
Vin1 = it is the voltage applied at the inverting terminal of op-amp
Vin2= it is the voltage applied at the non-inverting terminal of op-amp
Ad= Differential Gain
Vout= It is the output of the op-amp.

- To calculate the differential amplifier gain we can use :-

Ad=Vout/(Vin1-Vin2)

4.18 Subcircuit Schematic Diagram

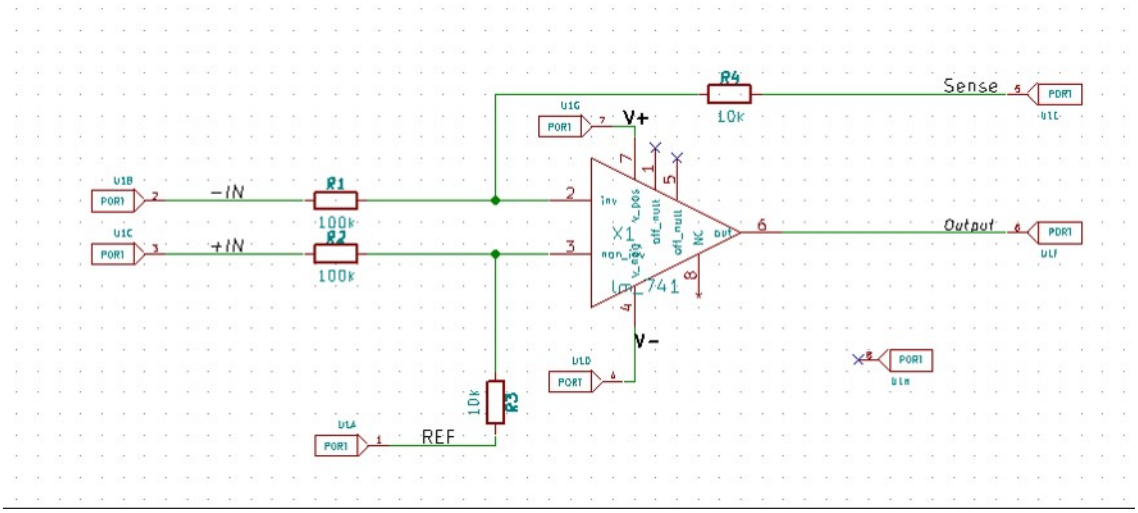

Figure 4.17: Subcircuit Schematic Diagram of INA106 Differential Amplifier using Op-Amp

4.19 Schematic with external circuit

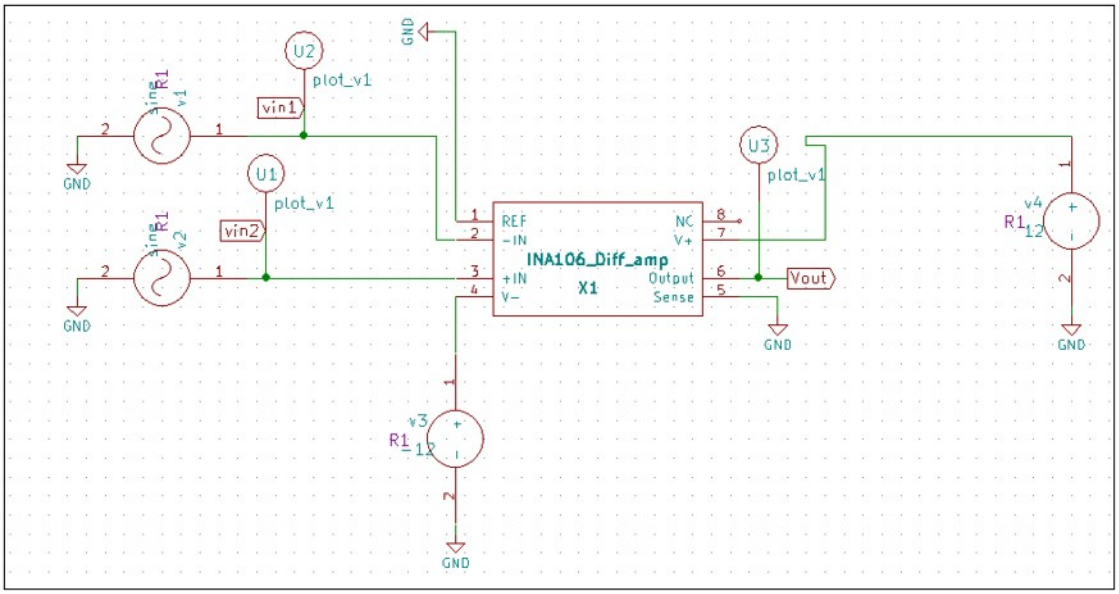

Figure 4.18: Schematic of Differential Amplifier

4.20 Ngspice Plots

4.20.1 Input plot

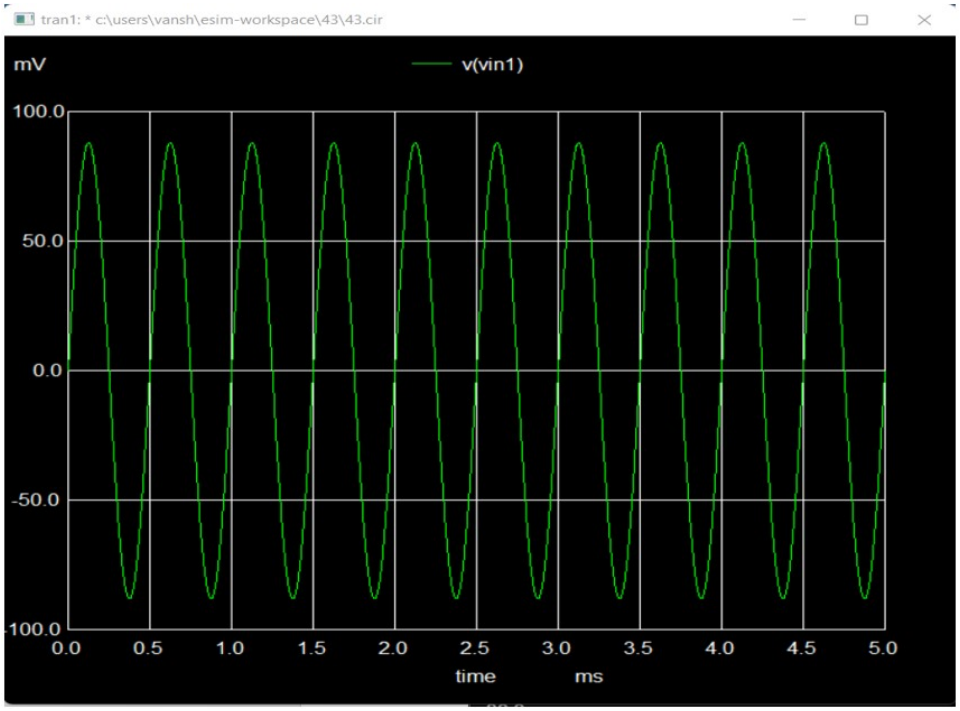

Figure 4.19: Input sine wave Vin1

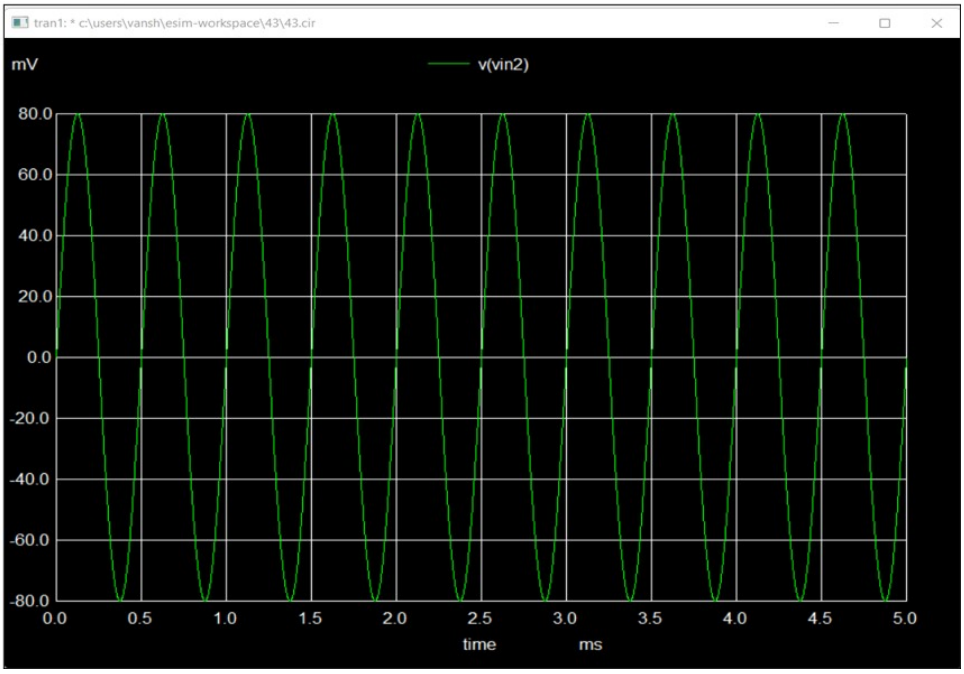

Figure 4.20: Input sine wave Vin2

4.20.2 Output plot

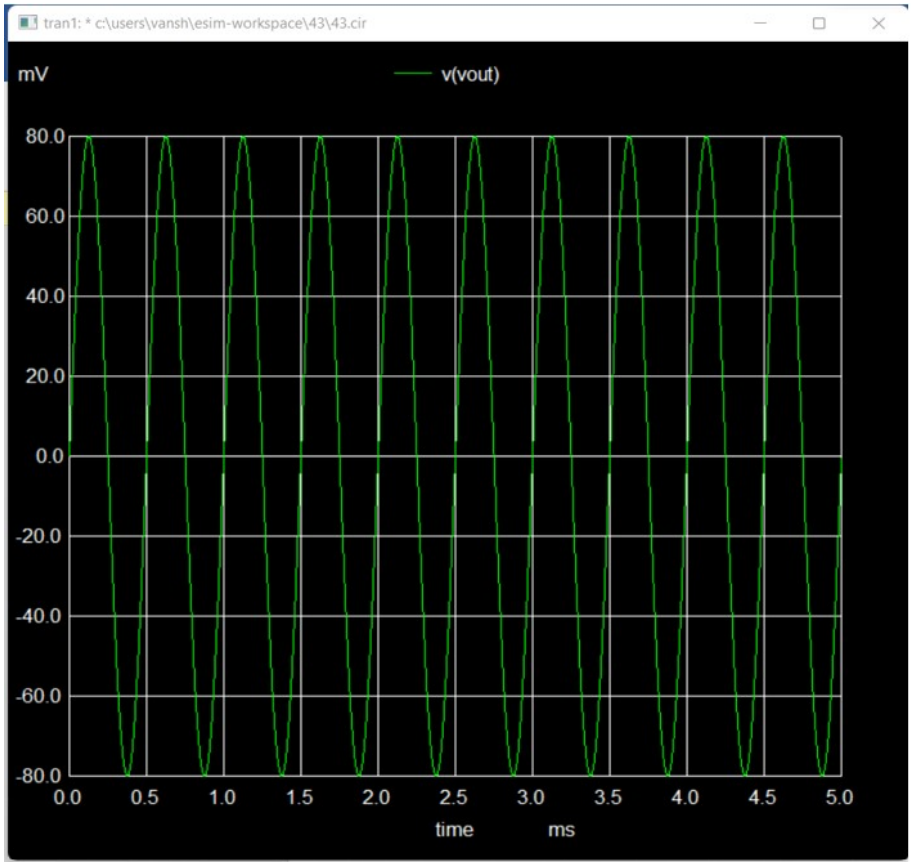

Figure 4.21: Output Waveform

Calculating the differential gain from the waveform (Ad),

$$Vin1 = 88v$$
$$Vin2 = 80v$$
$$Vout = 80v$$
$$Ad = Vout/(Vin1 - Vin2)$$
$$= 80/(88 - 80)$$
$$= 80/(8)$$
$$Ad = 10$$

4.21 74V1G14 Schmitt Trigger IC

Schmitt Trigger is the circuit that is used to convert any type of input signal into a square waveform.

4.22 Pin Configuration

It's a 5 pin IC named 74V1G14 [7] Schmitt Trigger.

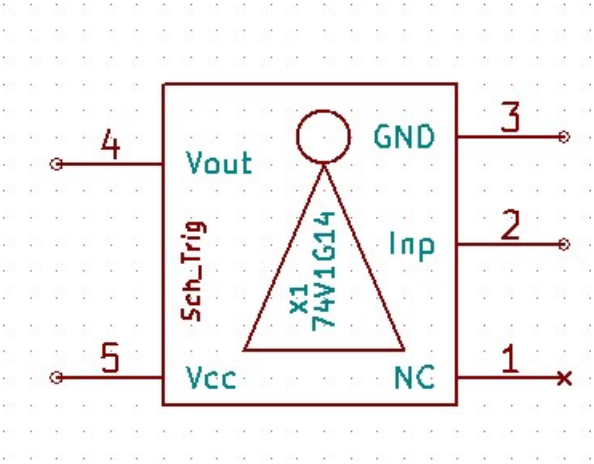

Figure 4.22: 74V1G14 Pin Configuration

The name of all pins are

Pin No.	Pin Name	Pin Description
1	NC	Not Connected Pin.
2	Inp	Input pin of Schmitt trigger.
3	GND	It represents ground.
4	Vout	It represents the Output pin of Schmitt trigger.
5	VCC	Input power supply.

4.23 Subcircuit Schematic Diagram

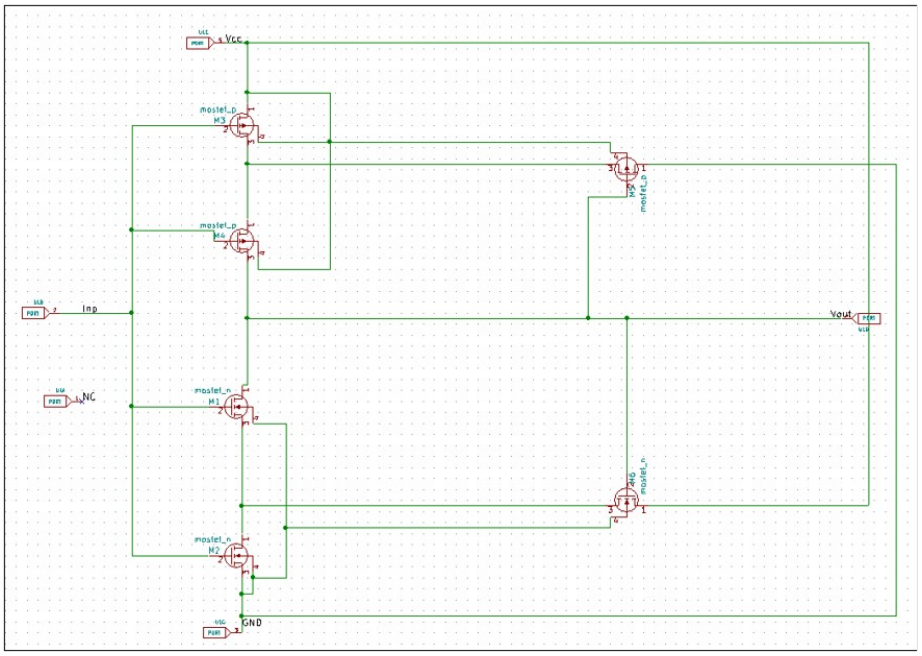

Figure 4.23: Subcircuit Schematic Diagram of 74V1G14 Schmitt Trigger

4.24 Schematic with external circuit

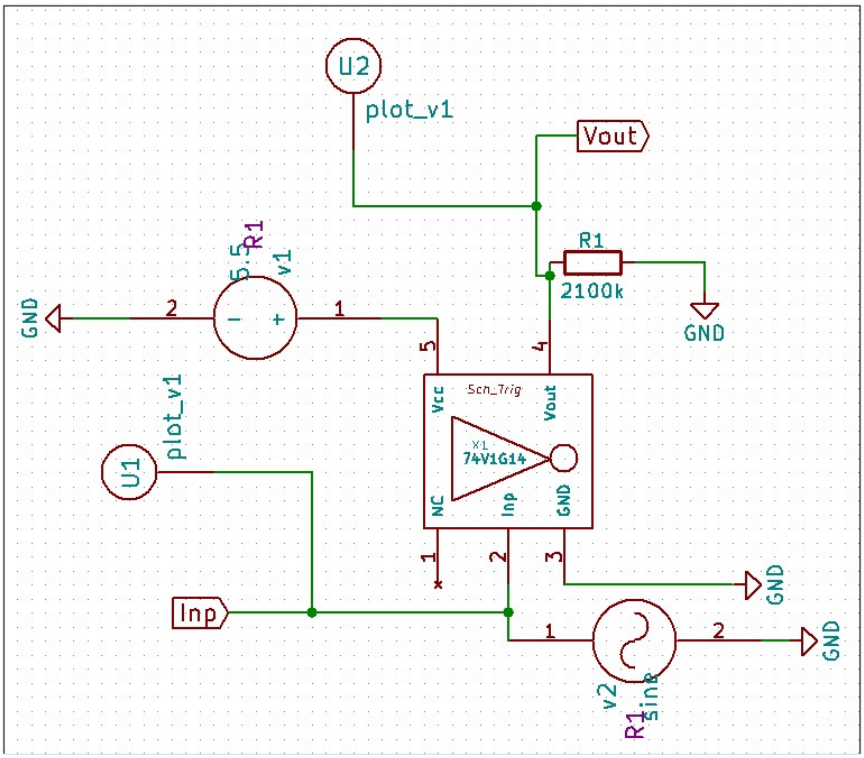

Figure 4.24: Test circuit Schematic of Schmitt Trigger

4.25 Ngspice Plots

4.25.1 Input plot

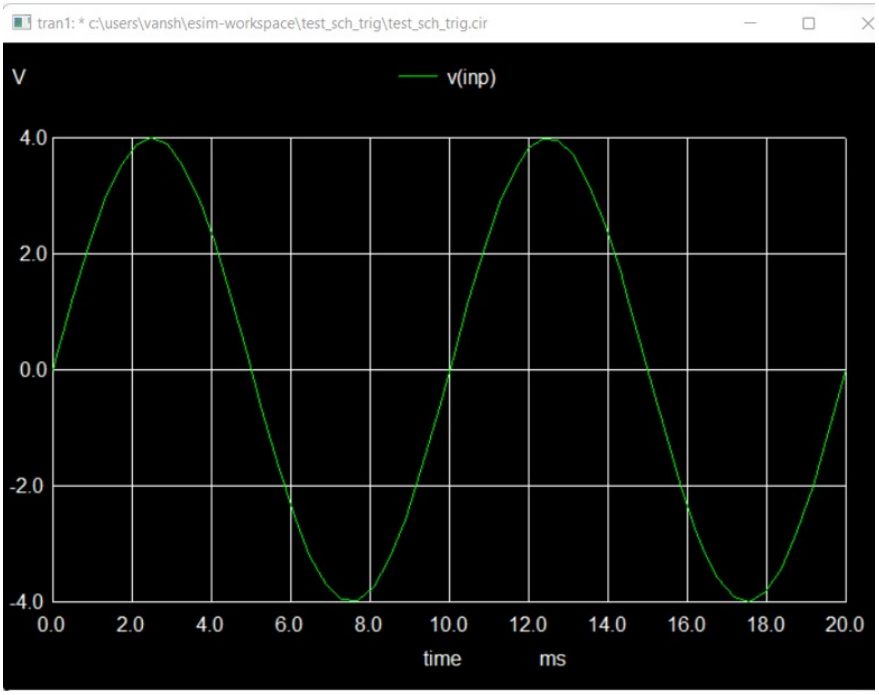

Figure 4.25: Input Sine wave

4.25.2 Output plot

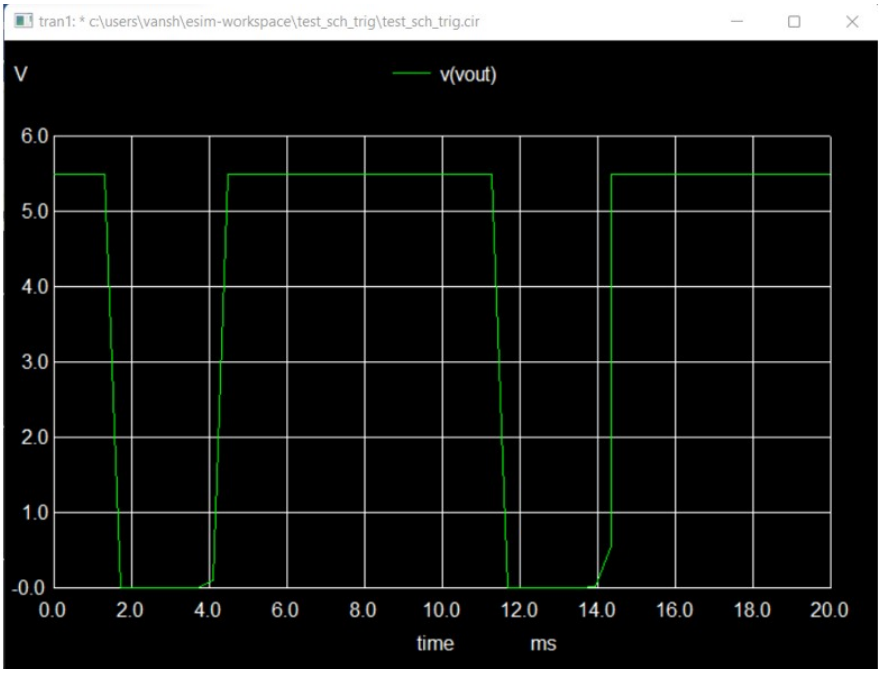

Figure 4.26: Output Waveform

Mathematical Calculation of +Vsat $+Vsat = 0.9Vcc$

+Vsat=0.9 x 5.5 = $4.95v$

Observations from the waveform,
$Vutp = 3.18v$
$Vltp = 1.88v$
$+Vsat = 5.51v$
$-Vsat = 0.01v$

Hystersis Voltage calculation = $Vutp - Vltp = 3.18 - 1.88$
$Vh = 1.3V$

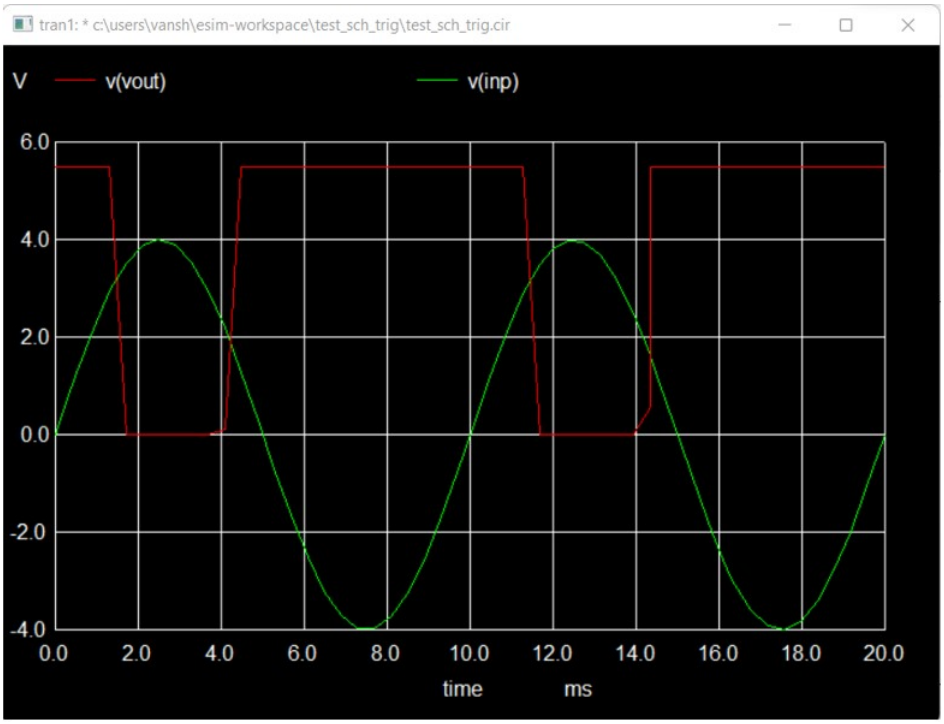

Figure 4.27: Combined Input and Output waveform

4.26 Precision Rectifier IC

The major drawback of the normal diode is that it can not be able to rectify the voltages below (0.6 v) which is the cut-in voltage. So, a special type of diode is used which is a precision diode that is capable of rectifying the input voltage signals in the order of milli volt. So, a circuit that uses this special type of diode(precision diode) is called a precision rectifier.

4.27 Pin Configuration

It's a 4-pin IC named *Precision Rectifier* [8].

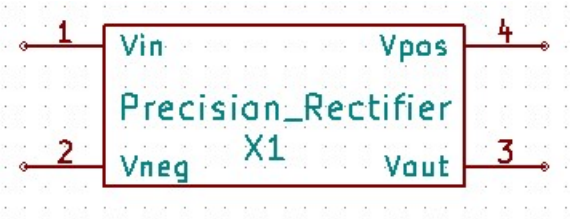

Figure 4.28: Pin Configuration

The description of each pin is given below:-

Pin No.	Pin Name	Pin Description
1	Vin	It represents the input pin where input is given.
2	Vneg	It represents the negative power supply.
3	Vout	It is an output pin where output is measured.
4	Vpos	It represents the positive power supply.

4.28 Subcircuit Schematic Diagram

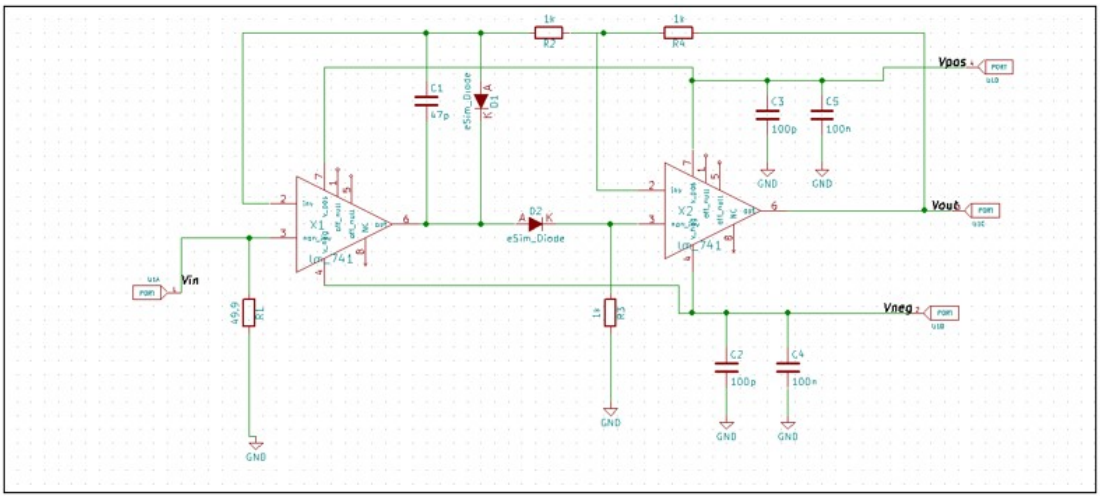

Figure 4.29: Subcircuit Schematic Diagram of Precision Rectifier

4.29 Schematic with external circuit

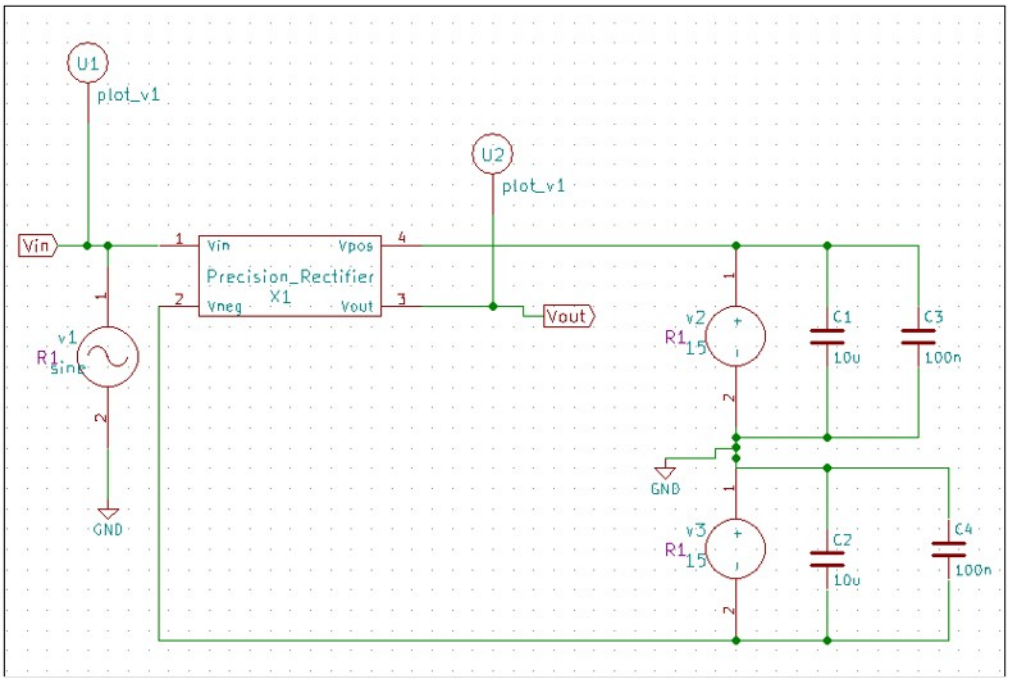

Figure 4.30: Test circuit Schematic of Precision Rectifier

4.30 Ngspice Plots

4.30.1 Input plot

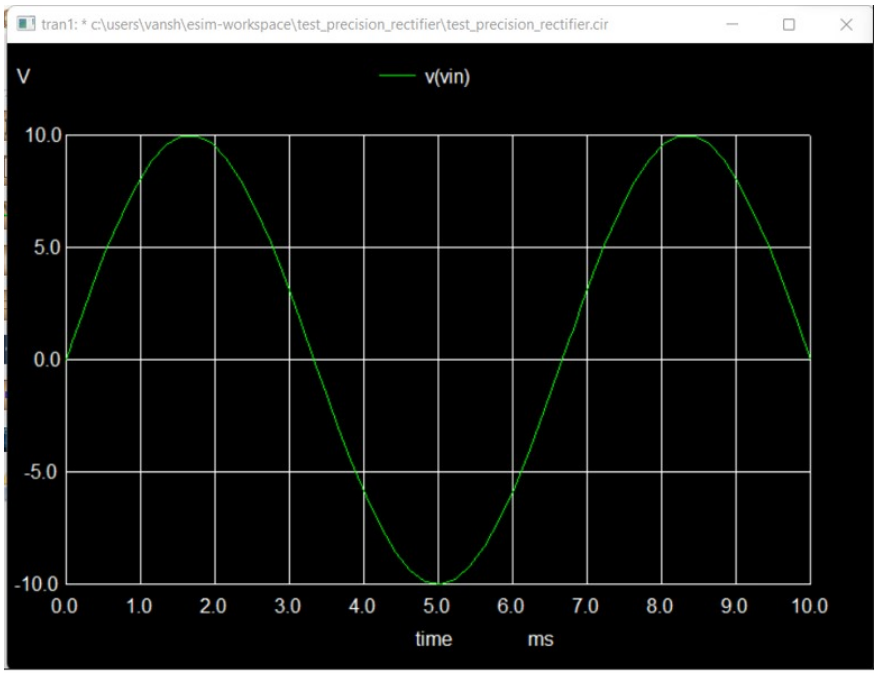

Figure 4.31: Input Sine wave

4.30.2 Output plot

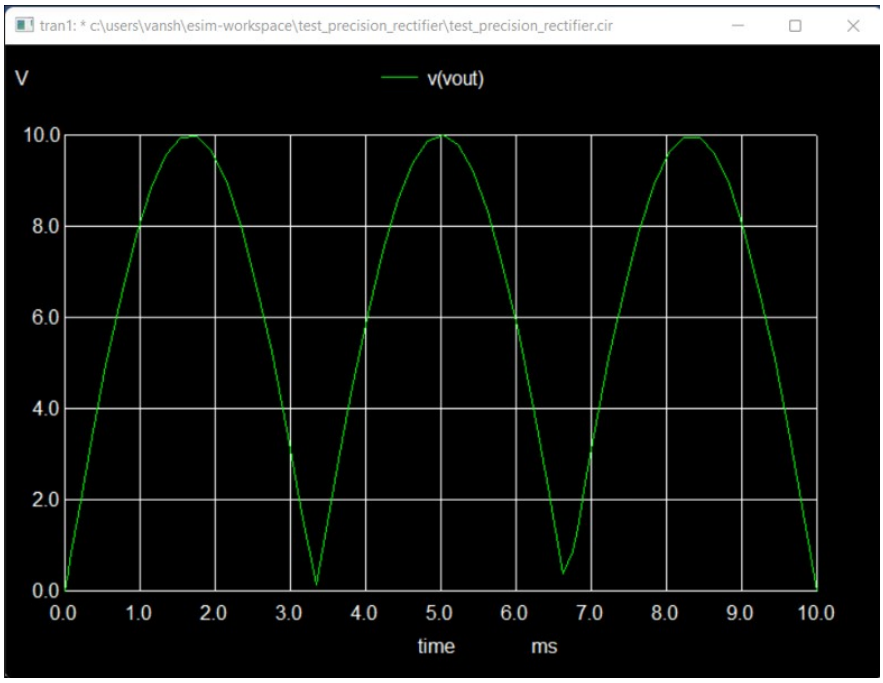

Figure 4.32: Output Waveform

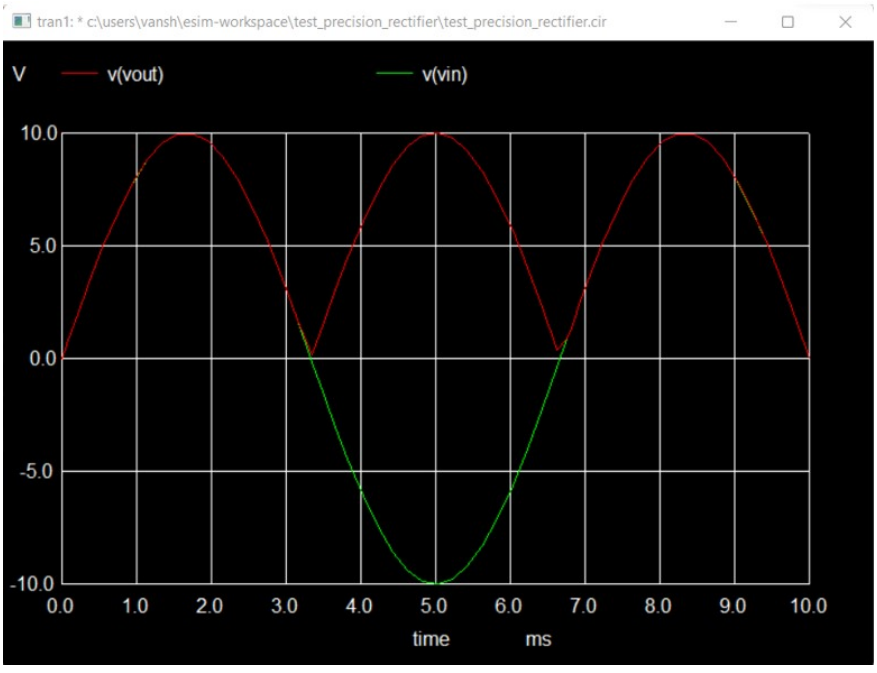

Figure 4.33: Combined Input and Output waveform

4.31 LM723 Adjustable Voltage Regulator IC

LM723 [9] is an adjustable voltage regulator IC. It's regulated output can be determined, by the external circuitry. It's output can range from 2V to 37V. It can be used either as a linear regulator or a switching regulator. The Line Regulation & Load Regulation observed for this IC is 0.089% and 0.351% respectively.

4.32 Pin Configuration

It comes in the form of 14 pin DIP package and a cylindrical packaging as well.

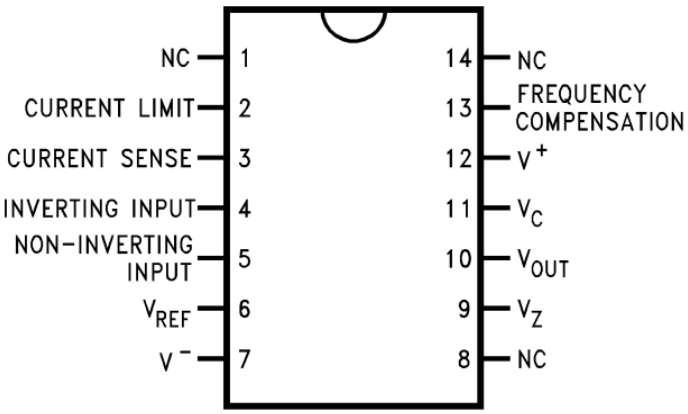

Figure 4.34: LM723 Pin Configuration

4.33 Subcircuit Schematic Diagram

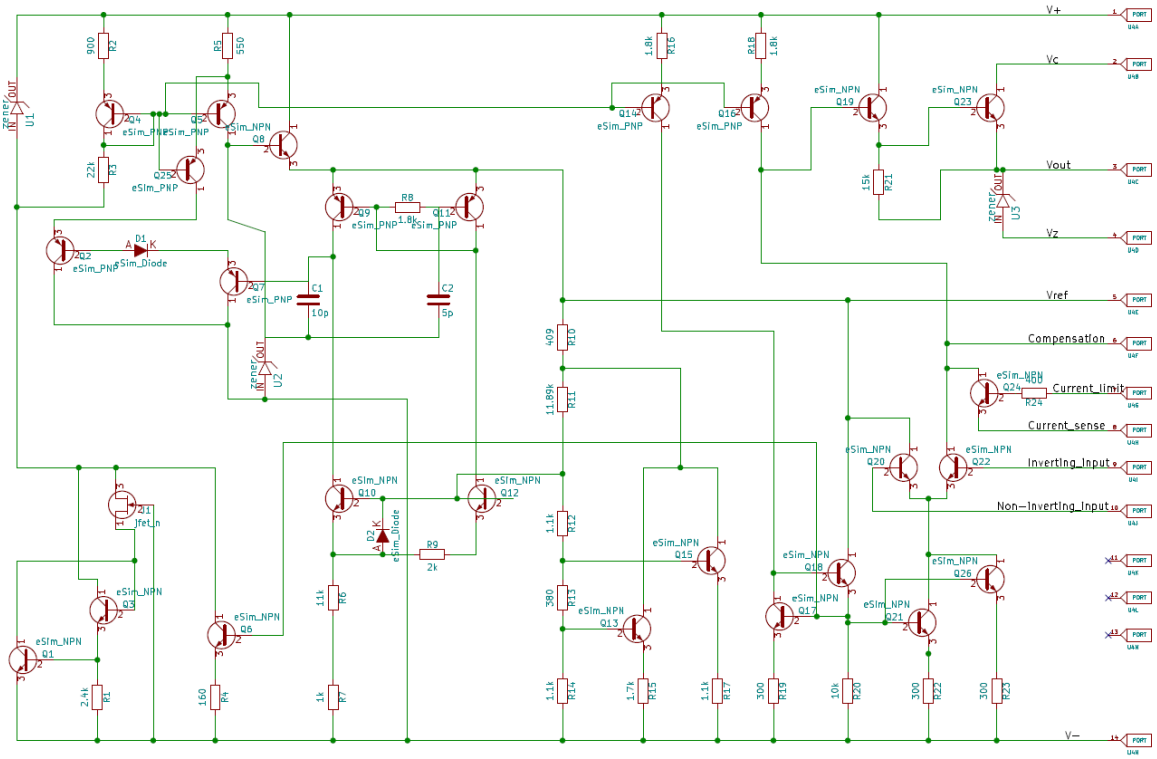

Figure 4.35: LM723 Subcircuit Schematic Diagram

4.34 Schematic with external circuit

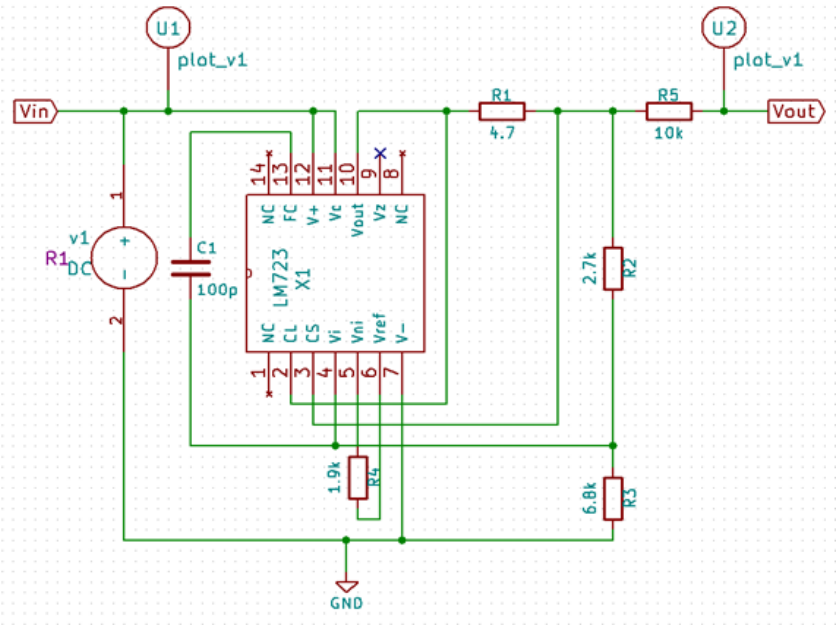

Figure 4.36: 7V Voltage Regulator circuit

4.35 Ngspice Plots

4.35.1 Input plot

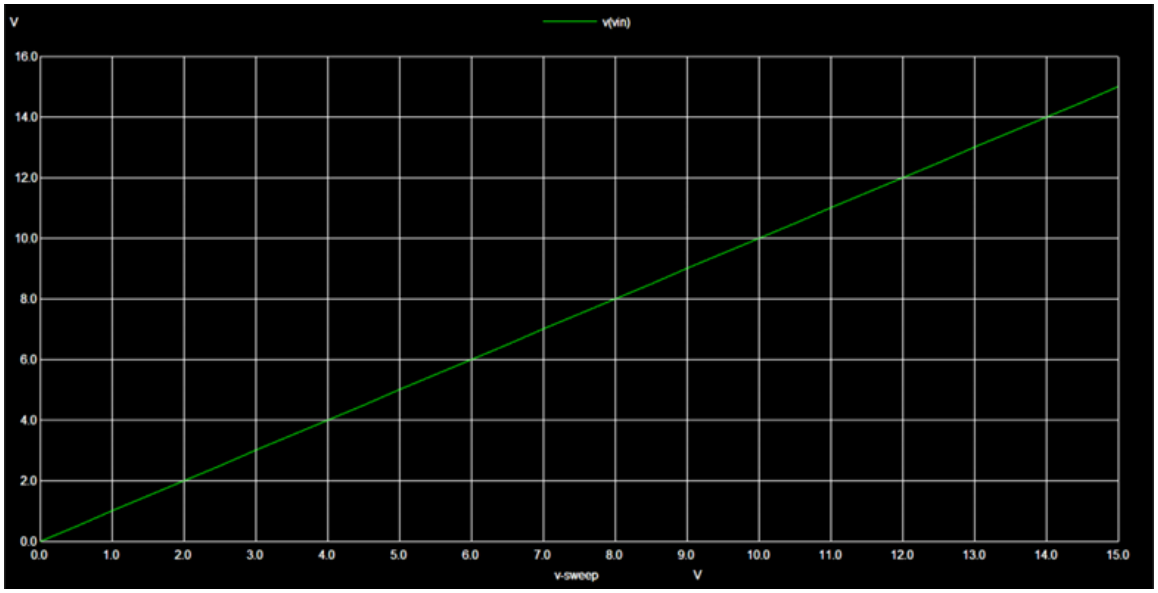

Figure 4.37: Linearly increasing DC input

4.35.2 Output plot

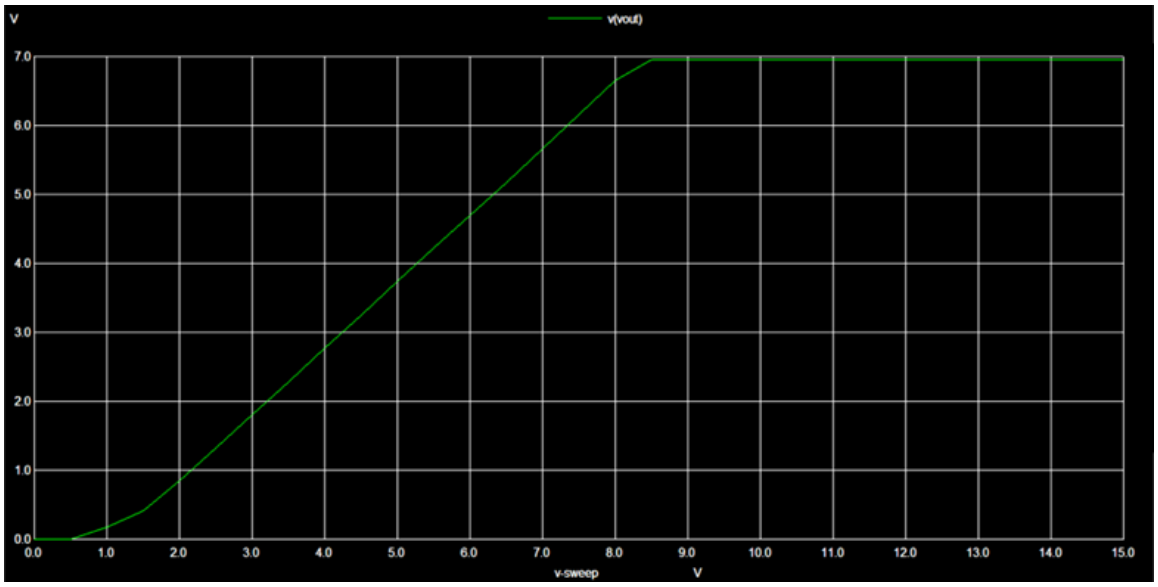

Figure 4.38: 7V Regulated output

4.36 Schematic with external circuit

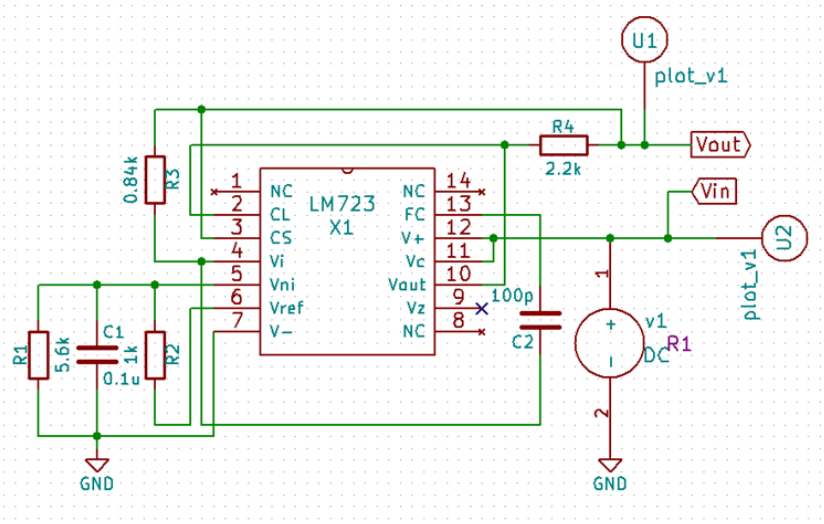

Figure 4.39: 4.25V Voltage Regulator circuit

4.37 Ngspice Plots

4.37.1 Input plot

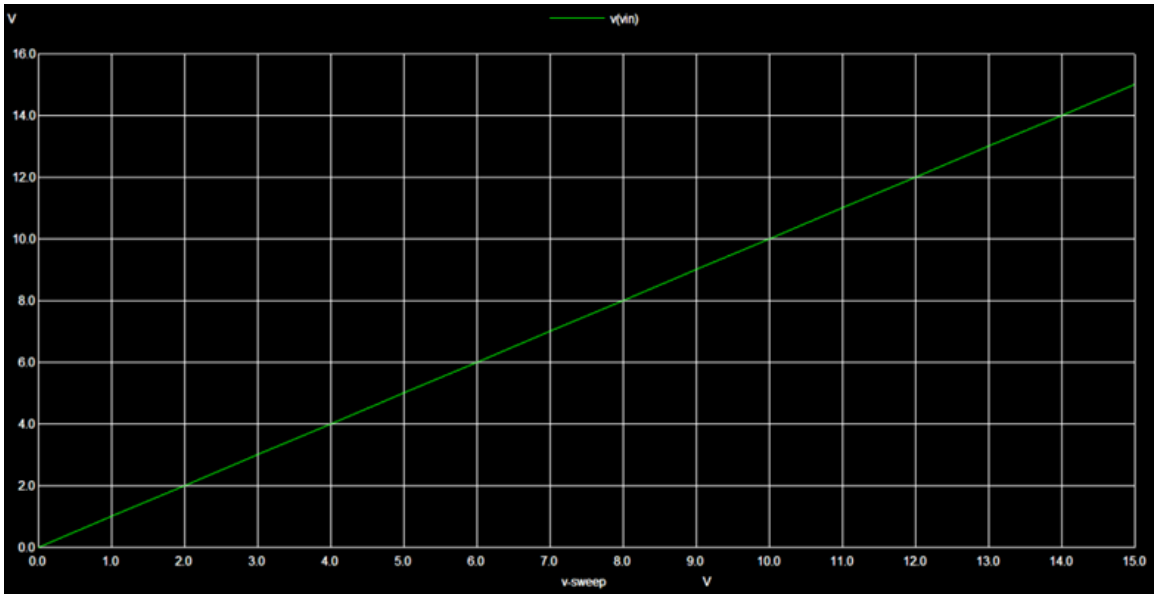

Figure 4.40: Linearly increasing DC input

4.37.2 Output plot

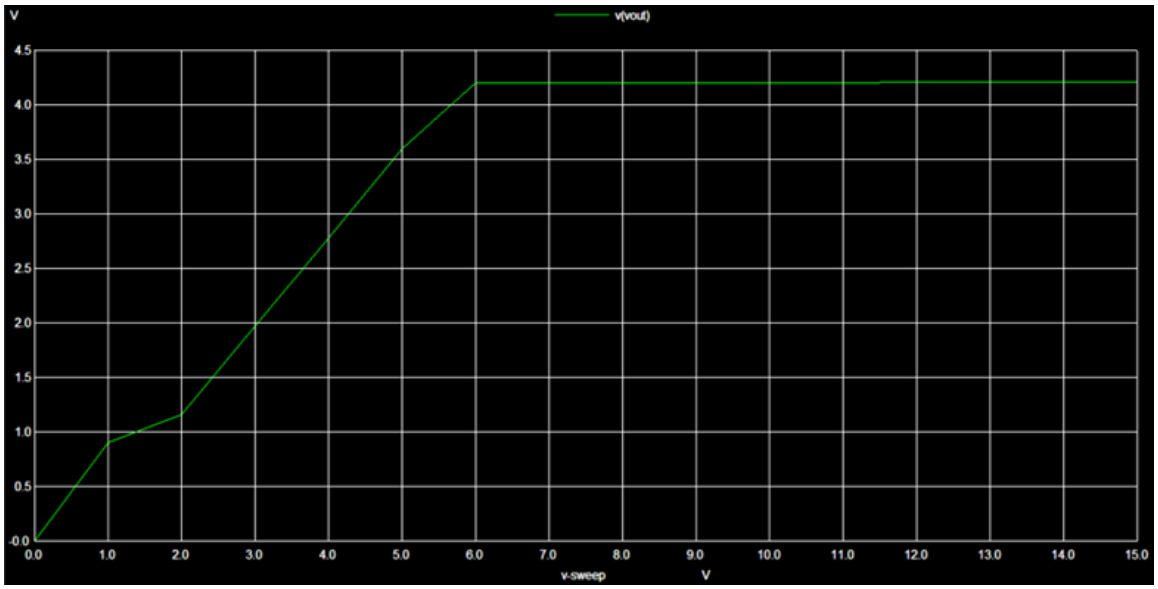

Figure 4.41: 4.25V Regulated output

4.38 LM13700 Operational Transconductance Amplifier IC

The LM13700 [10] is a current controlled, additional output buffer-equipped, differential input, transconductance amplifier with two channels. The two amplifiers operate independently, sharing a common supply. It makes use of linearizing diodes, using which higher input levels are permitted with less distortion. It has improved SNR also.
[**NOTE**] : Due to improper modeling of Darlington pair at the output terminals, this IC is producing improper output (DC Shifted & vertically compressed). Therefore the user is suggested to use this IC only after replacing the subcircuit with a proper working Darlington pair.

4.39 Pin Configuration

LM13700 is available in 16 pin DIP IC packaging shown below.

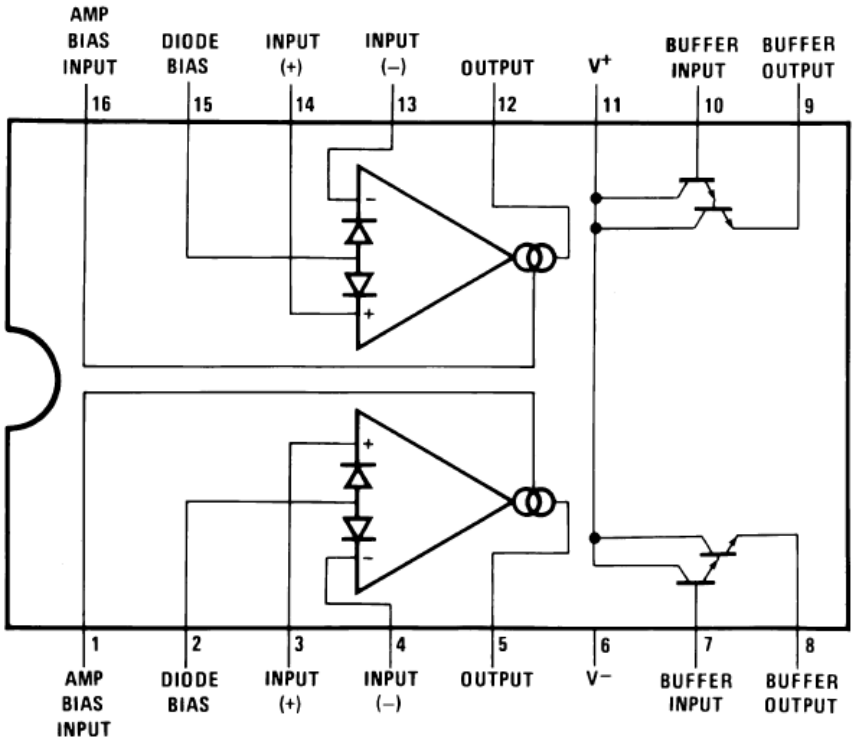

Figure 4.42: LM13700 Pin Configuration

4.40 Subcircuit Schematic Diagram

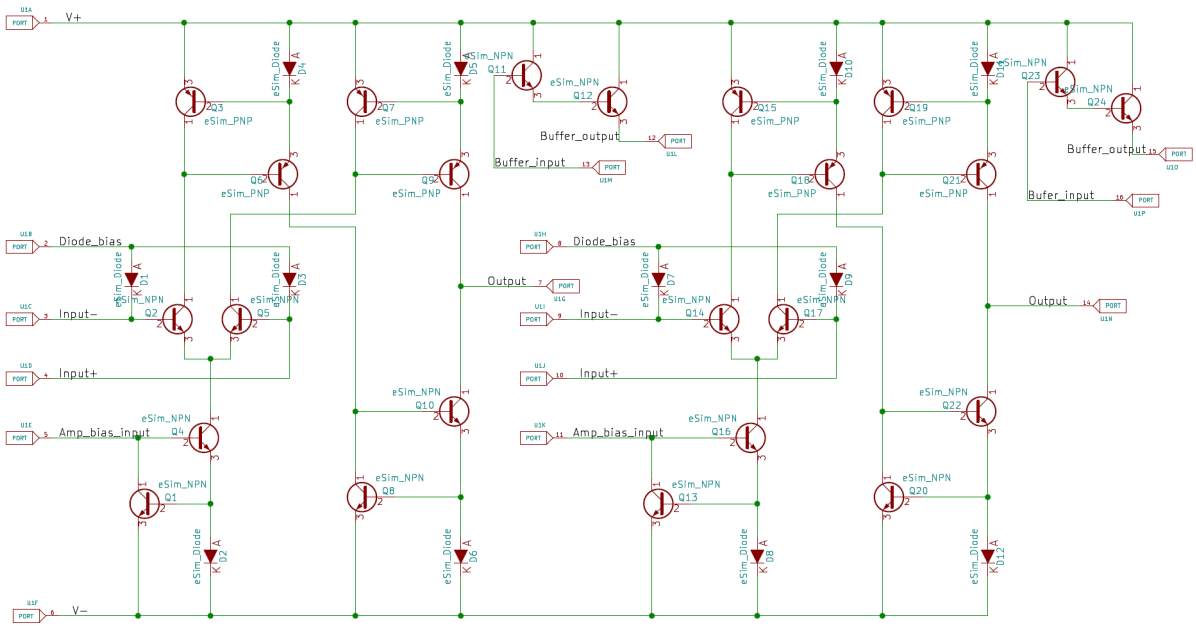

Figure 4.43: LM13700 Subcircuit Schematic Diagram

4.41 Schematic with external circuit

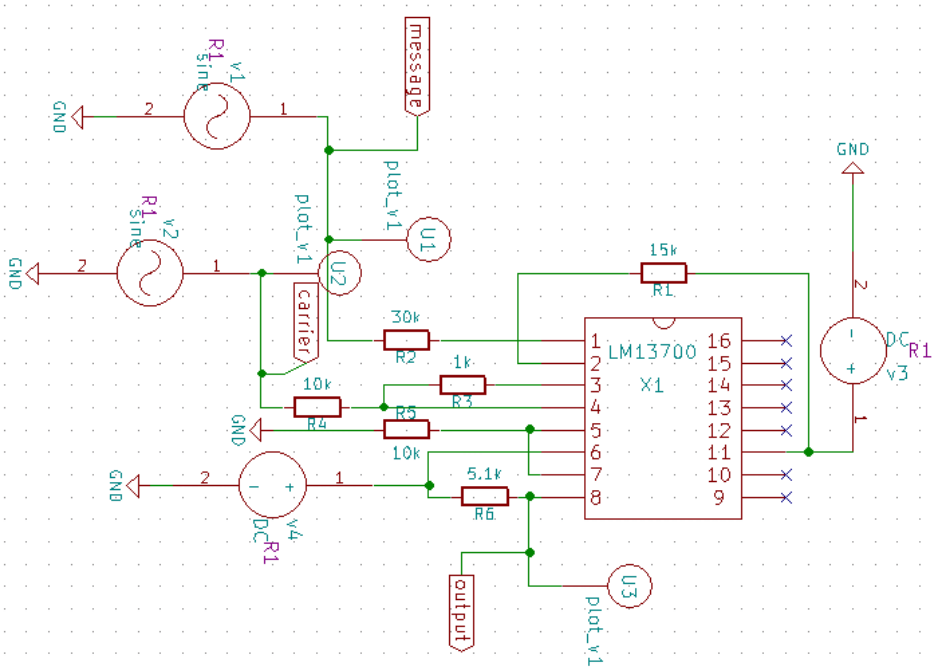

Figure 4.44: Amplitude Modulator circuit

4.42 Ngspice Plots

4.42.1 Input plot

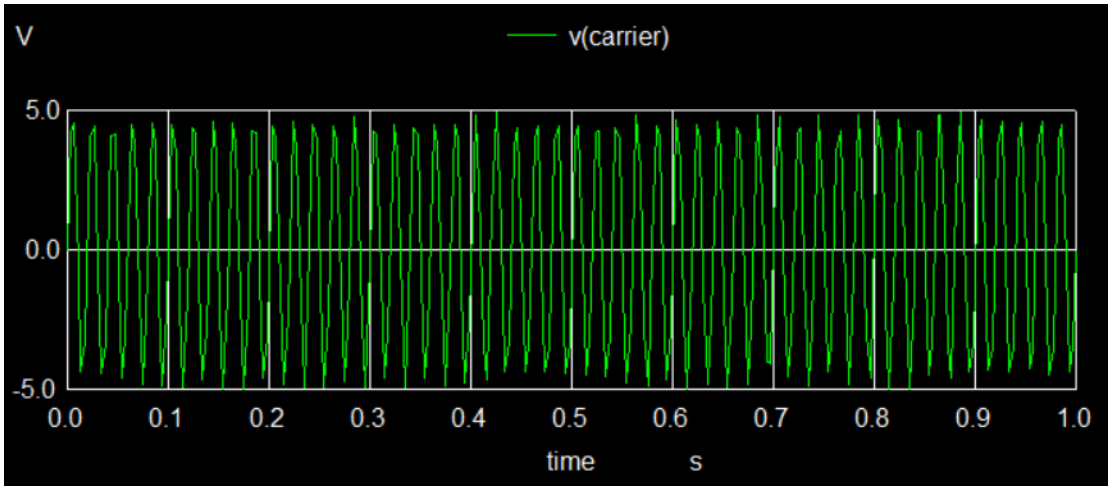

Figure 4.45: High frequency Carrier wave

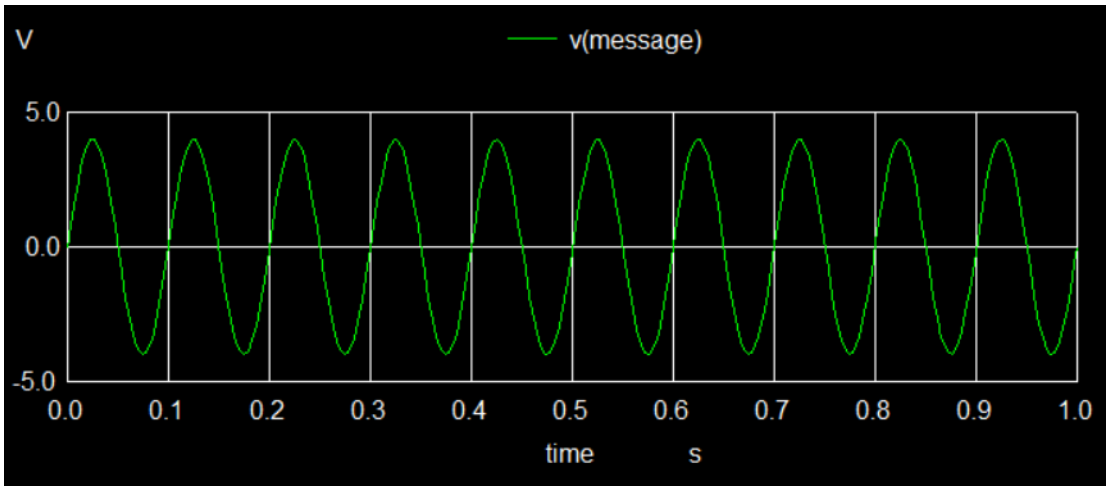

Figure 4.46: Baseband signal

4.42.2 Output plot

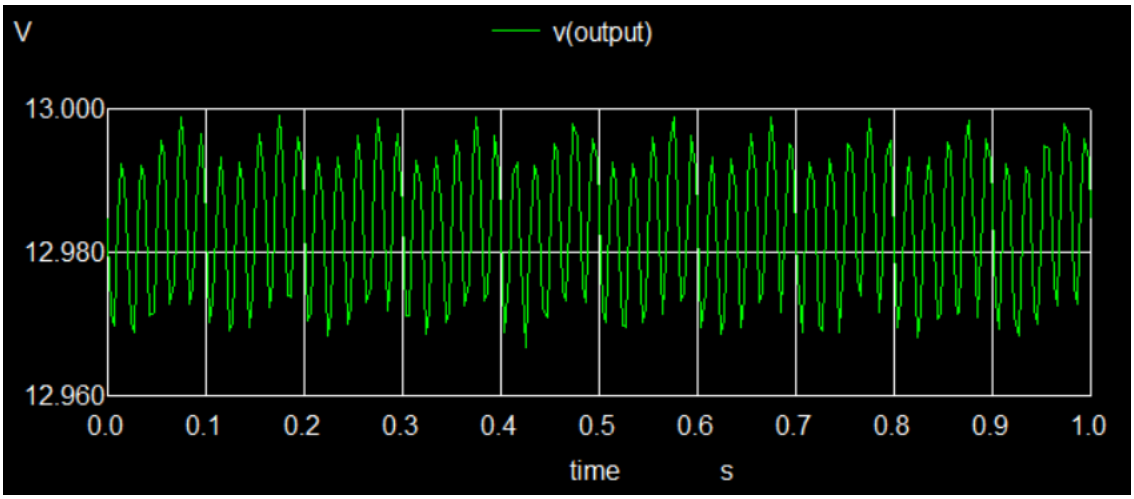

Figure 4.47: Amplitude Modulated signal

4.43 Schematic with external circuit

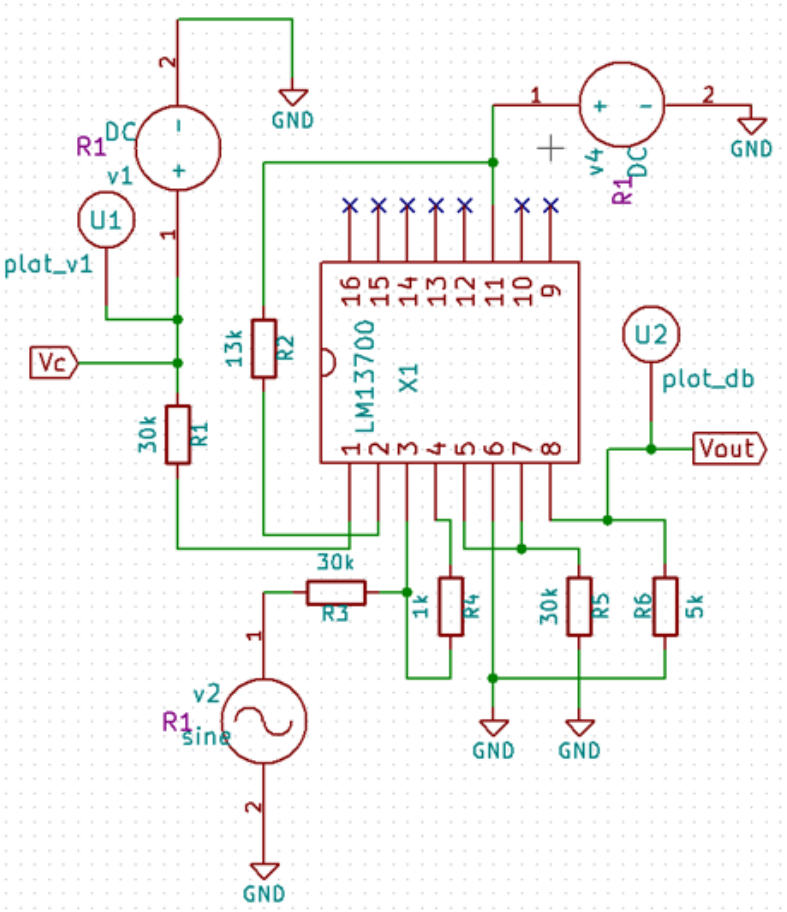

Figure 4.48: Voltage Controlled Amplifier circuit

4.44 Ngspice Plots

4.44.1 Input plot

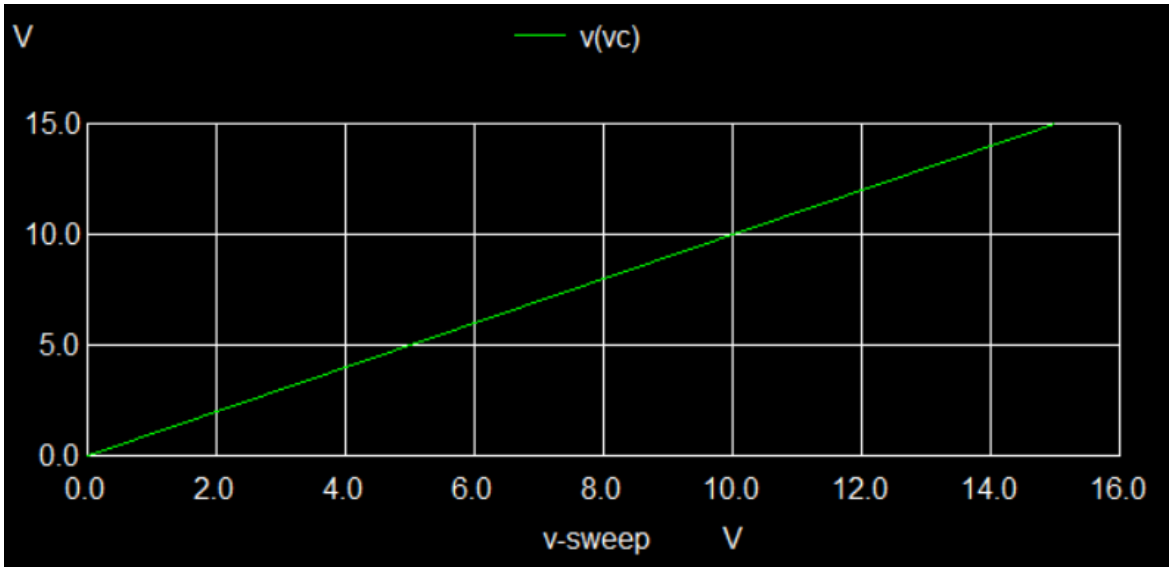

Figure 4.49: Linearly increasing Control voltage, sweep from 0 V to 15 V

4.44.2 Output plot

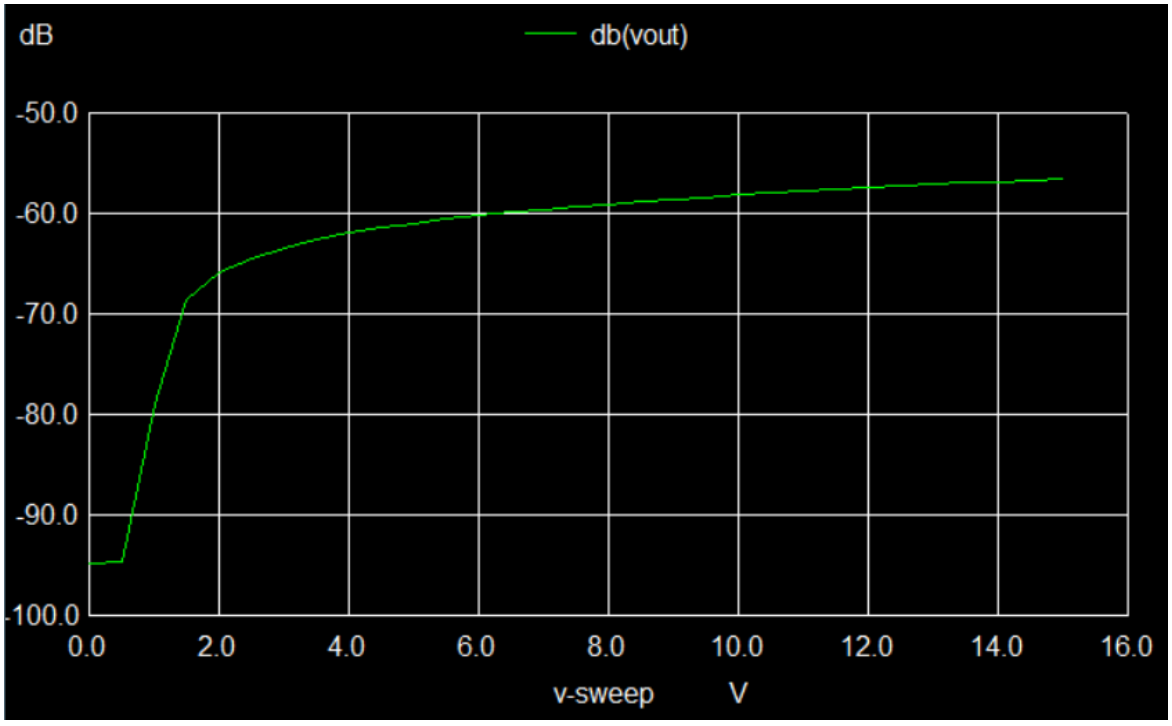

Figure 4.50: Output Response

4.45 LM393 Comparator IC

LM393 [11] is a Low power, low offset voltage comparator IC. It has two channels sharing common biasing. It is a high precision comparator with a low offset voltage of 2 mV. It has various applications such as in limit comparators, A/D convertors, wave shaping circuits etc.

4.46 Pin Configuration

LM393 is available in 8 pin DIP IC packaging shown below.

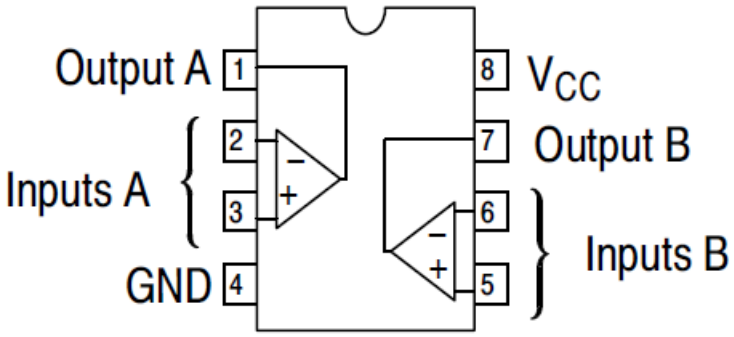

Figure 4.51: LM393 Pin Configuration

4.47 Subcircuit Schematic Diagram

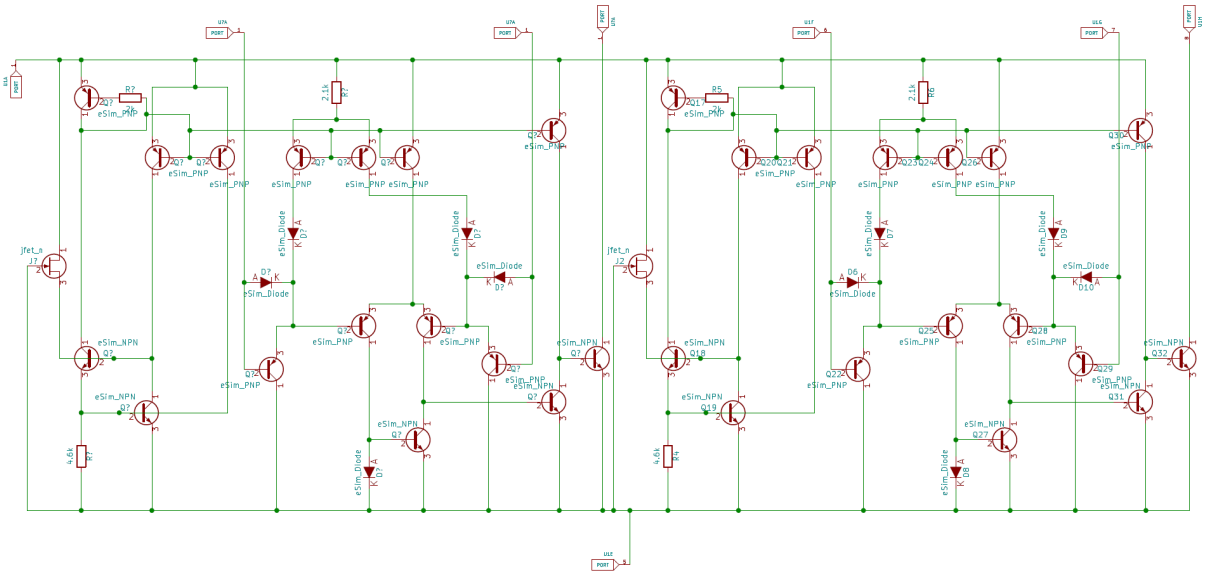

Figure 4.52: LM393 Subcircuit Schematic Diagram

4.48 Schematic with external circuit

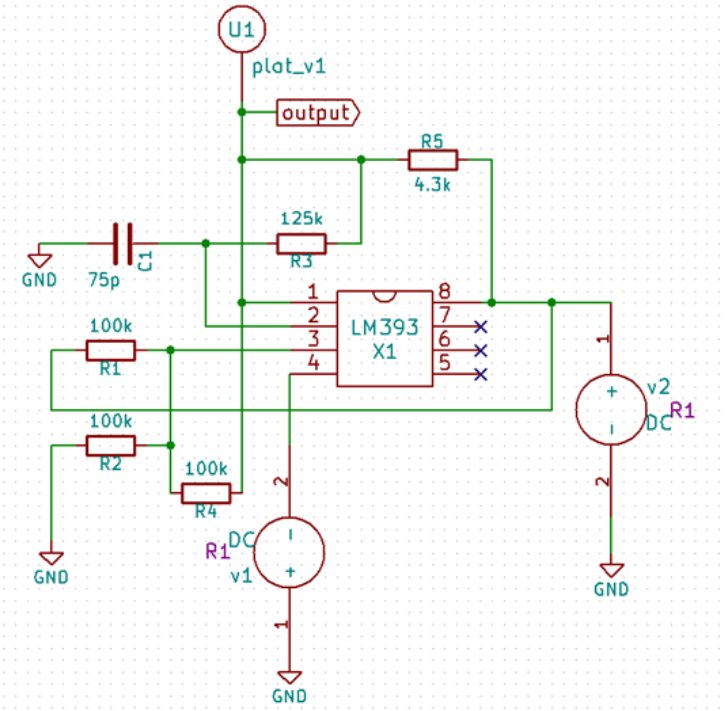

Figure 4.53: Free running Pulse Train Generator

4.49 Ngspice Plots

4.49.1 Output plot

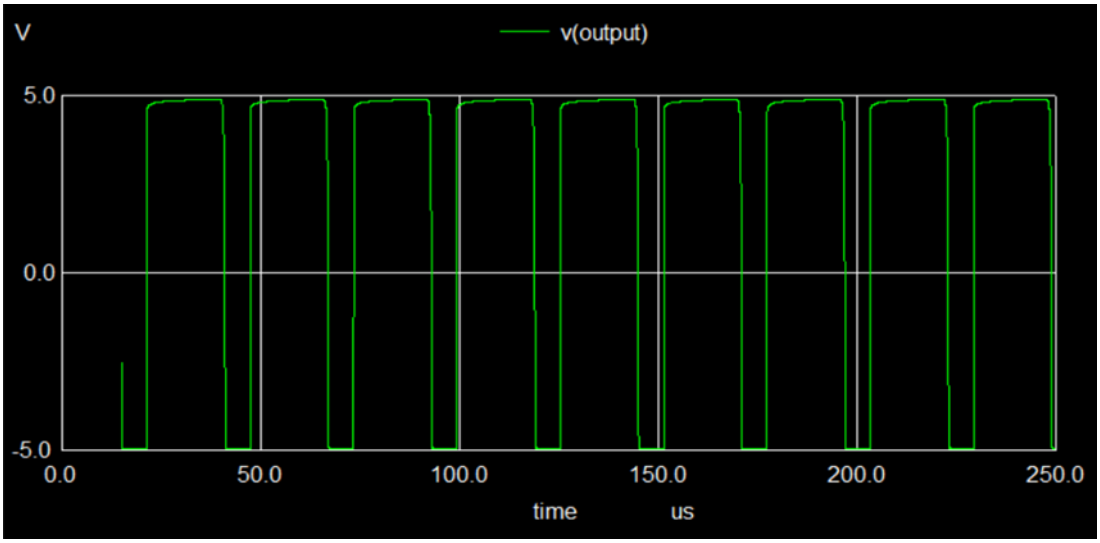

Figure 4.54: Output waveform

4.50 Schematic with external circuit

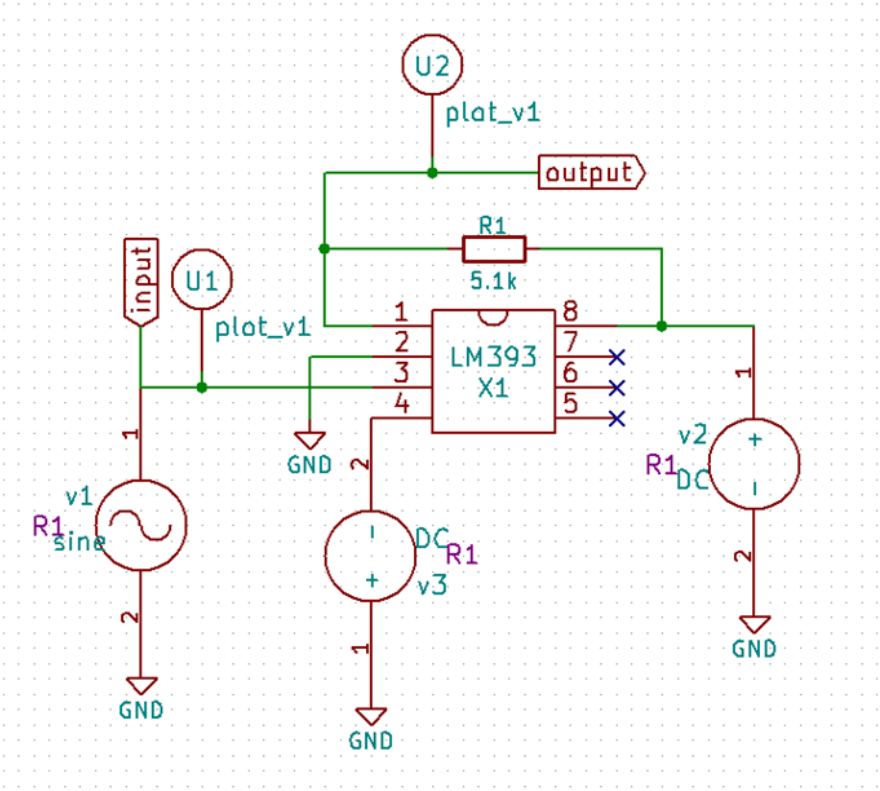

Figure 4.55: Zero crossing detector circuit

4.51 Ngspice Plots

4.51.1 Input plot

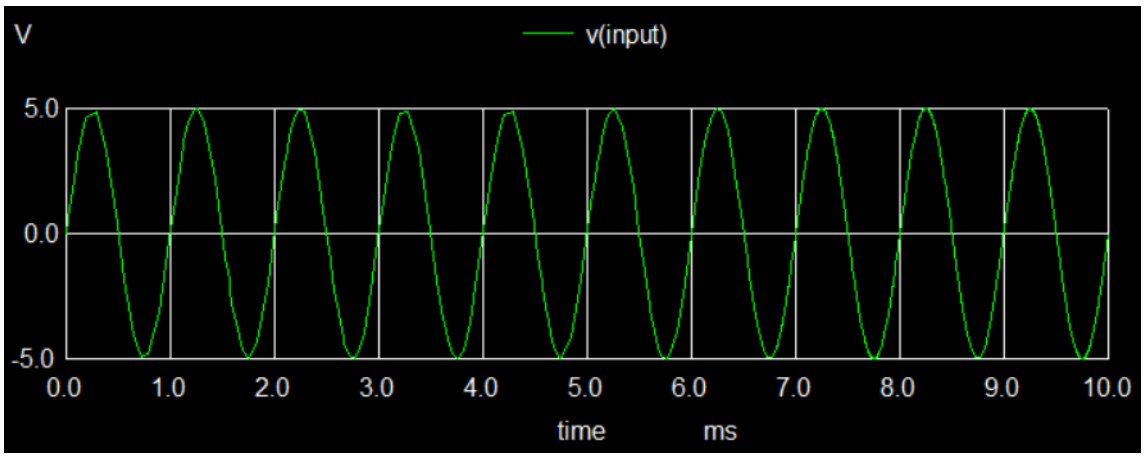

Figure 4.56: Sine wave input

4.51.2 Output plot

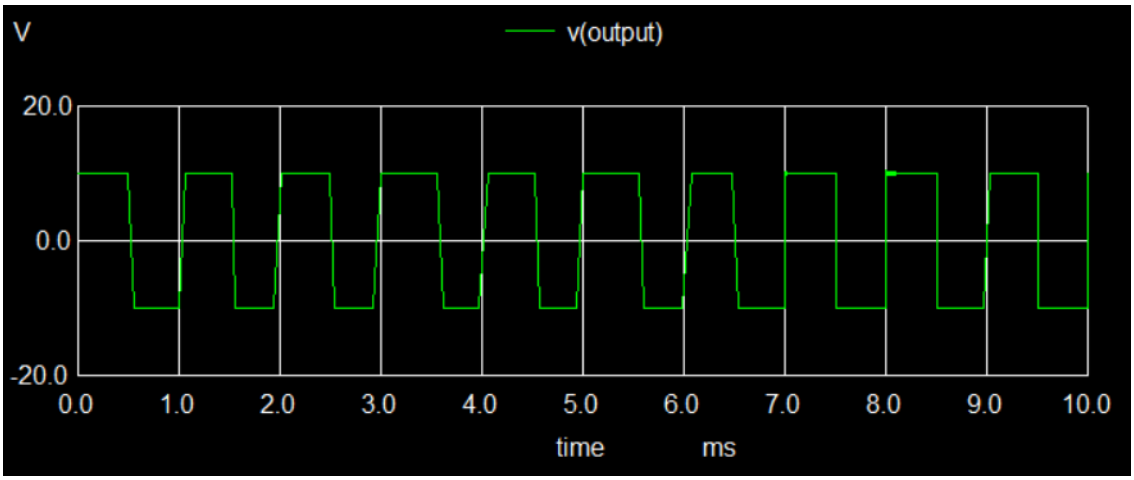

Figure 4.57: Square wave output

4.52 LM321 Operational Amplifier IC

LM321 [12] is a 5 pin Op-Amp IC. It has differential input, is internally compensated. Supply voltage ranges from 3V to 32V. Output is short circuit protected. Its output stage is class B, comprising of push-pull transistors. Hence output contains cross-over distortion near mid-rail where neither push or pull transistor is conducting.

4.53 Pin Configuration

LM321 is available in 5 pin surface mount IC packaging, shown below.

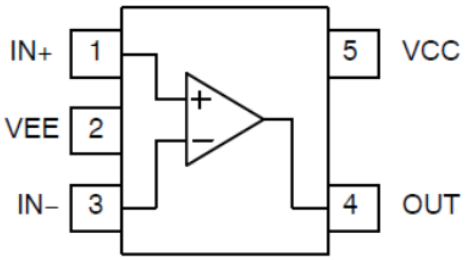

Figure 4.58: LM321 Pin Configuration

4.54 Subcircuit Schematic Diagram

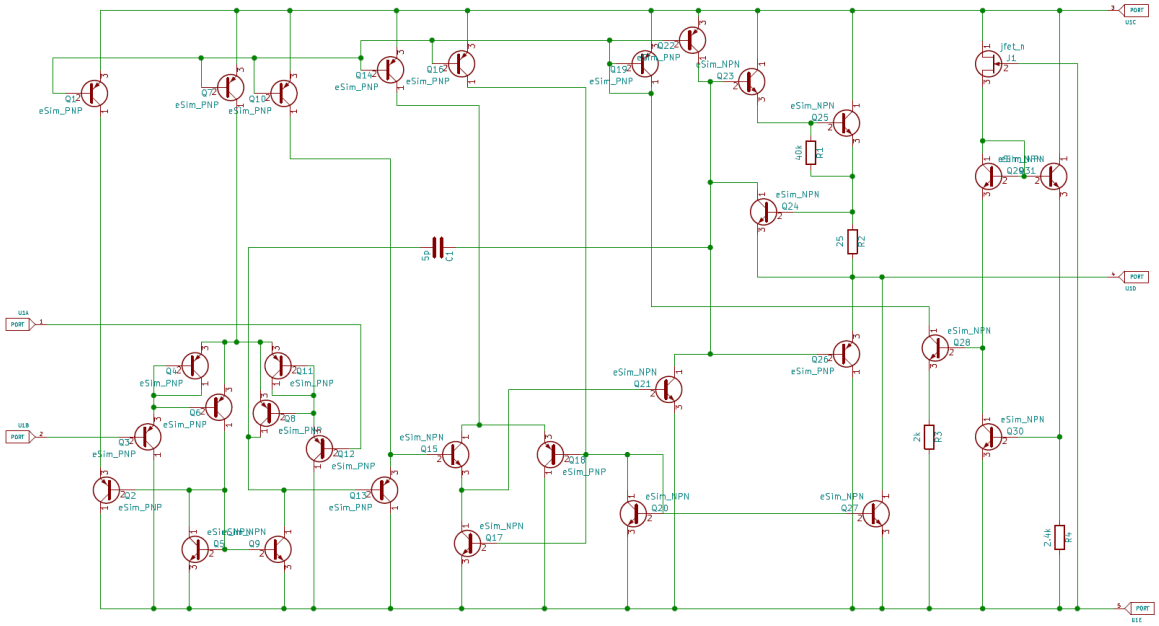

Figure 4.59: LM321 Subcircuit Schematic Diagram

4.55 Schematic with external circuit

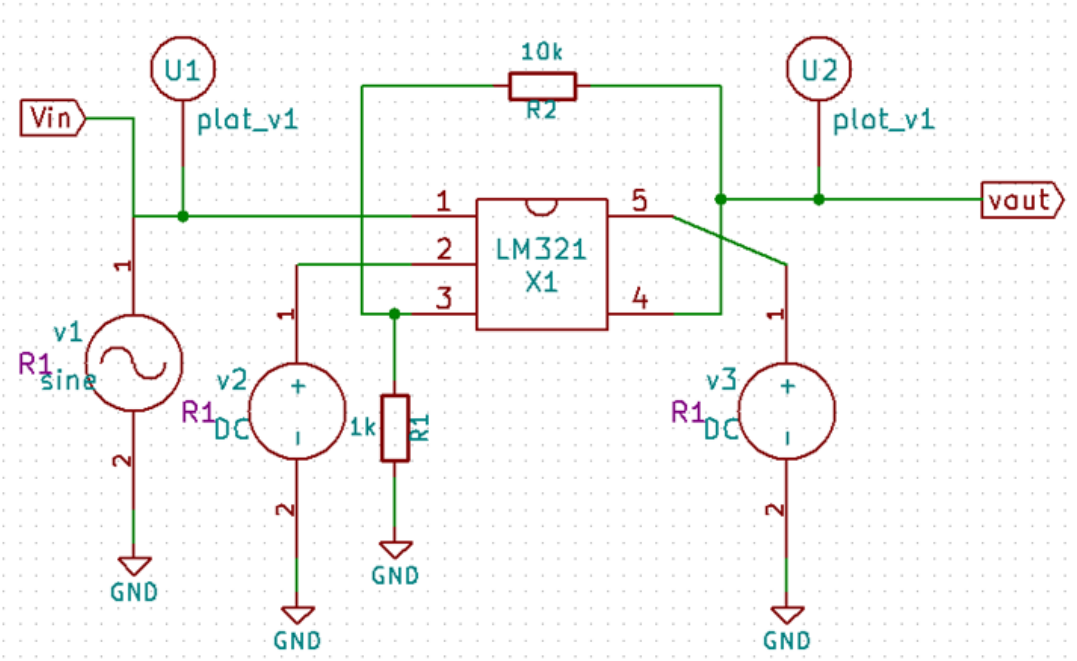

Figure 4.60: Non Inverting Amplifier

4.56 Ngspice Plots

4.56.1 Input plot

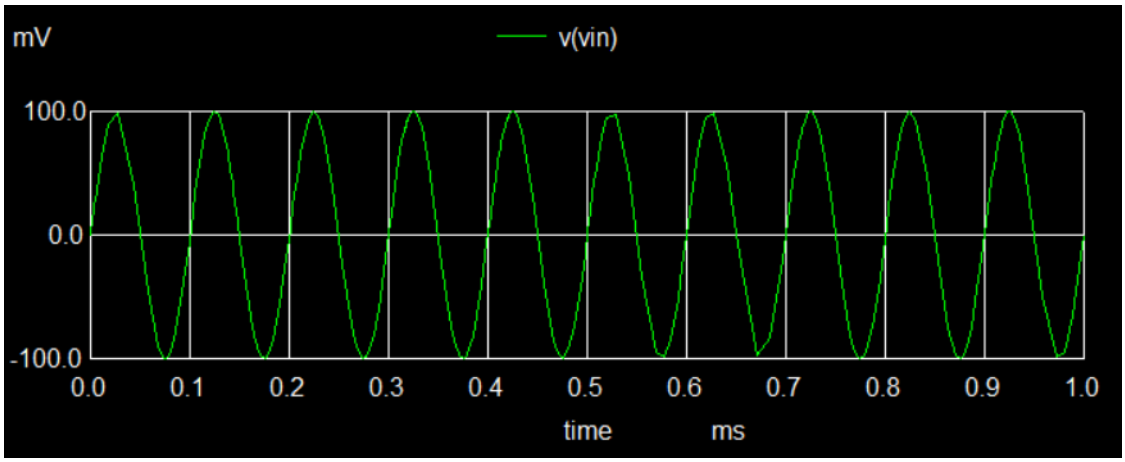

Figure 4.61: 0.1V Amplitude Sine wave input

4.56.2 Output plot

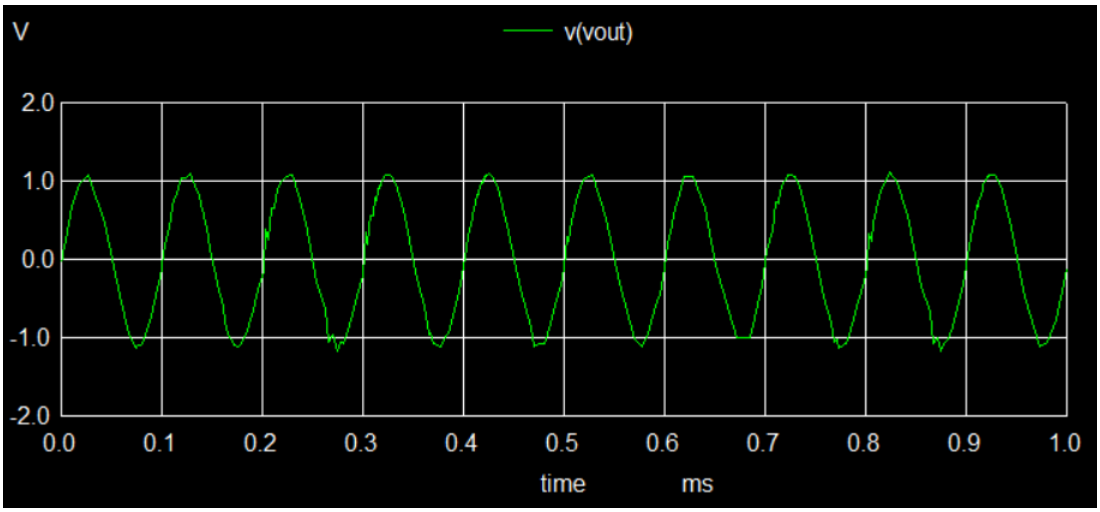

Figure 4.62: 1.1V Amplified wave output

4.57 Schematic with external circuit

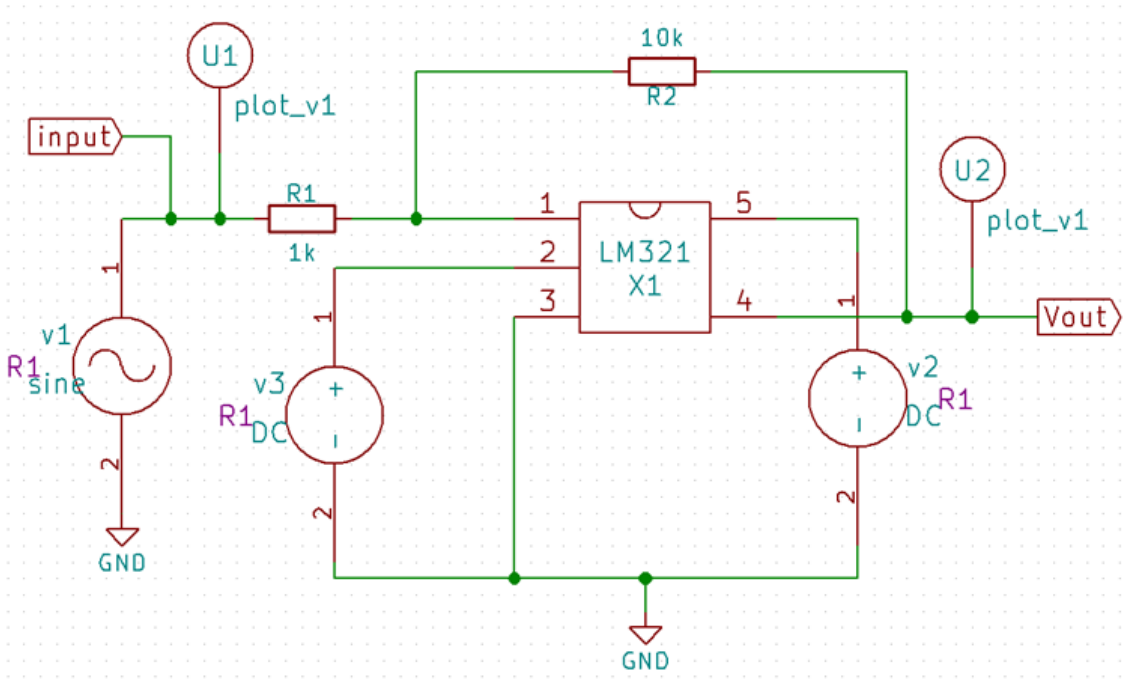

Figure 4.63: Non Inverting Schmitt Trigger

4.58 Ngspice Plots

4.58.1 Transient Analysis

Input plot

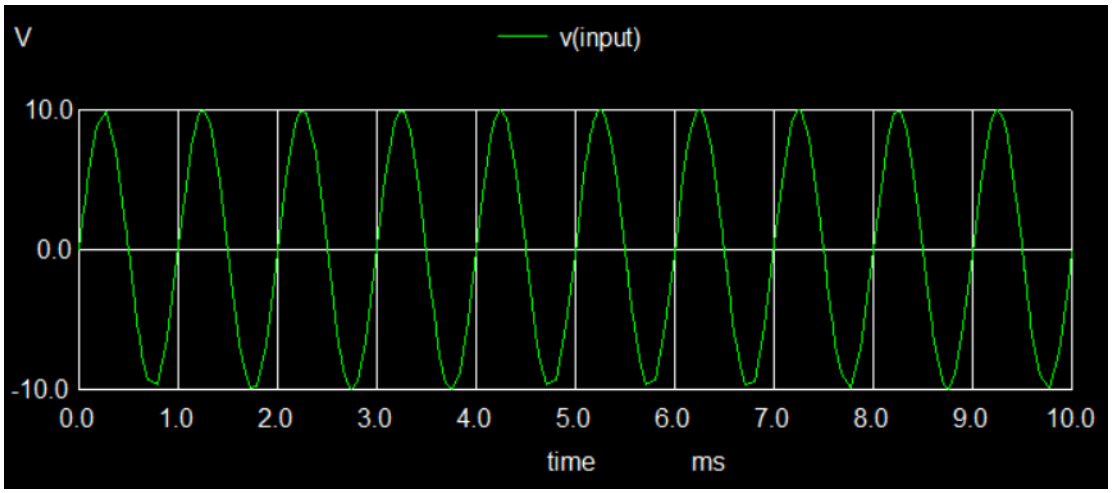

Figure 4.64: Sine wave input

Output plot

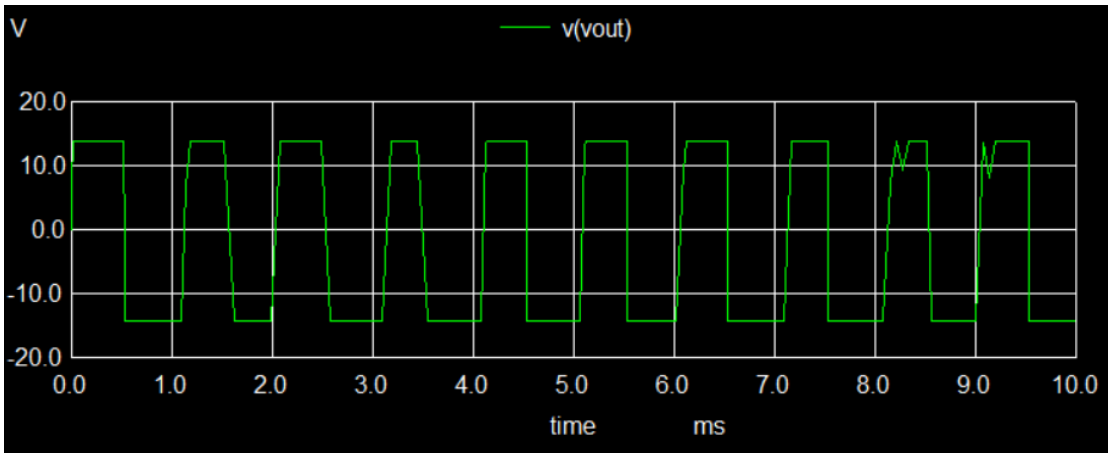

Figure 4.65: Square wave output

4.58.2 DC Analysis (Increasing Input Sweep)

Input plot

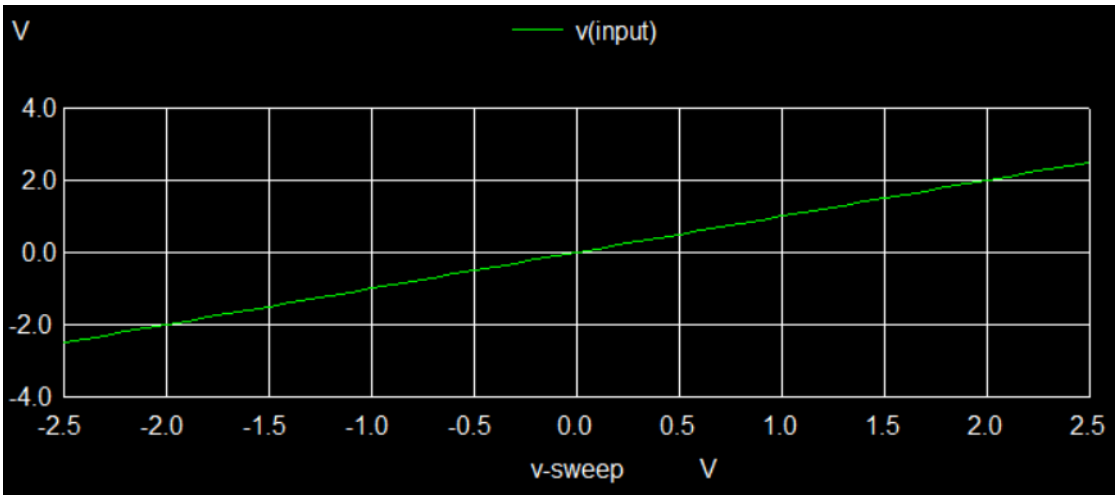

Figure 4.66: DC input sweep from -2.5V to +2.5V

Output plot

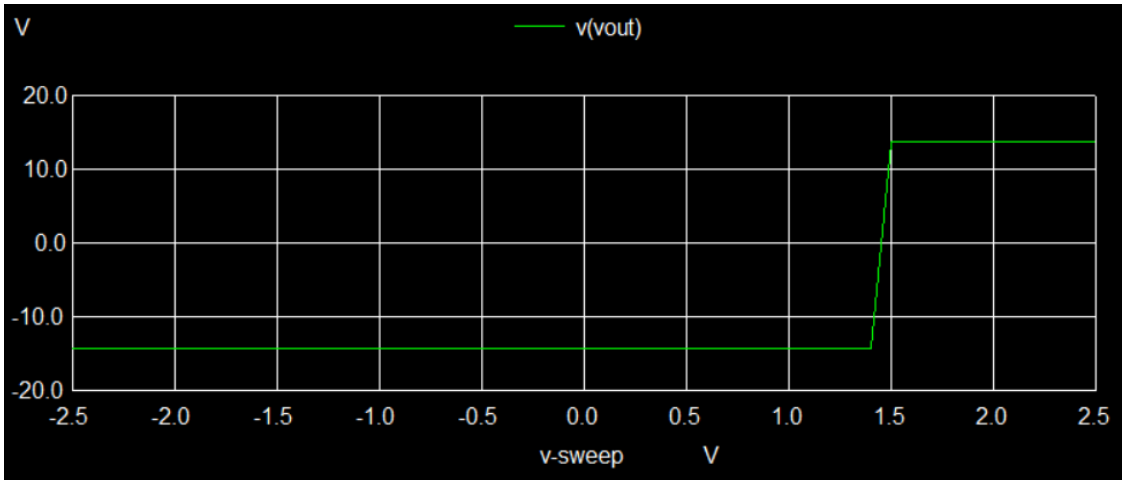

Figure 4.67: Output Transition at Vin=+1.4V

4.58.3 DC Analysis (Decreasing Input Sweep)

Input plot

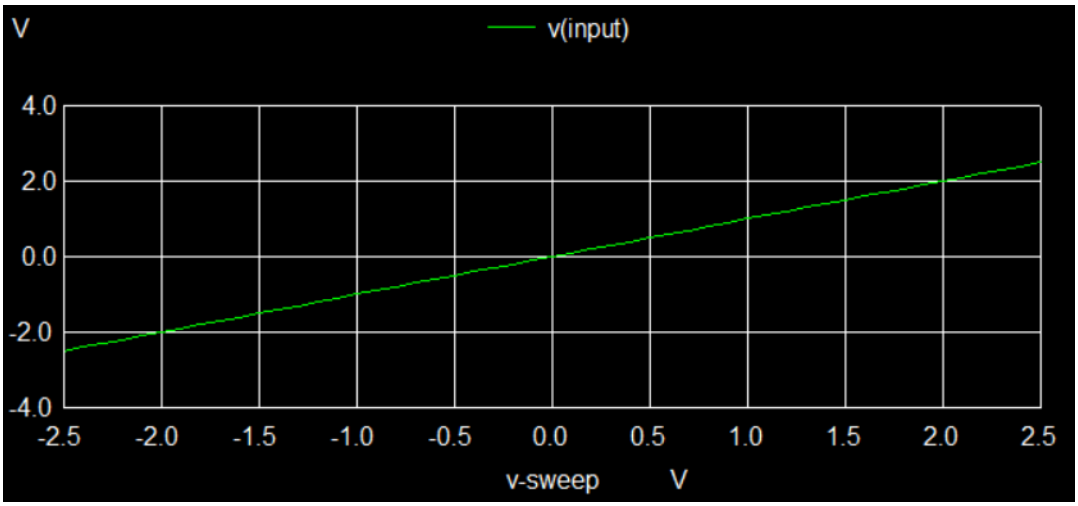

Figure 4.68: DC input sweep from +2.5V to -2.5V

Output plot

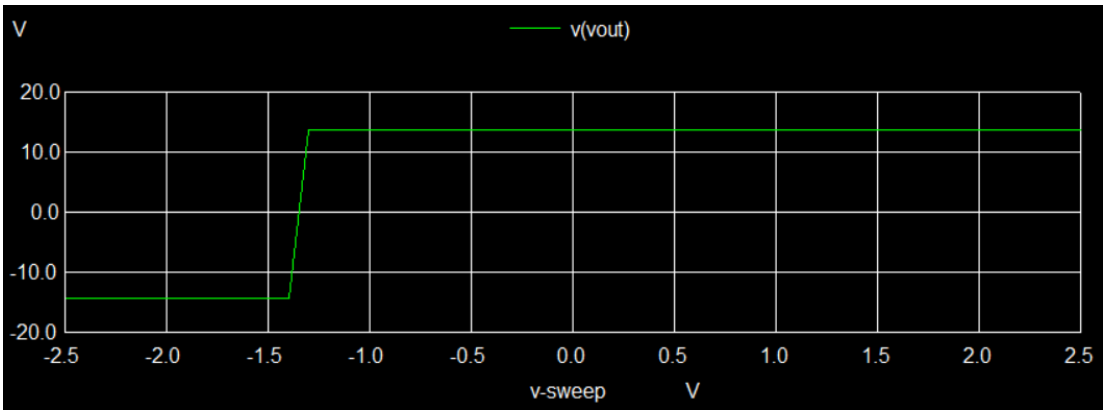

Figure 4.69: Output Transition at Vin = -1.4V

Observing the output for increasing sweep & Decreasing sweep, the transitions happen only at $\pm 1.4V$ hence the DC transfer/Hysteresis characteristics of Schmitt trigger is verified.

4.59 LM1458 Dual Operational Amplifier IC

LM1458 [13] is a general purpose, Dual Channel Operational Amplifier IC. Both the Amplifiers operate independently but they share common supply. It has inbuilt short circuit protection & offers low power consumption. No frequency compensation is needed.

4.60 Pin Configuration

LM1458 is available in 8 pin DIP IC packaging, shown below.

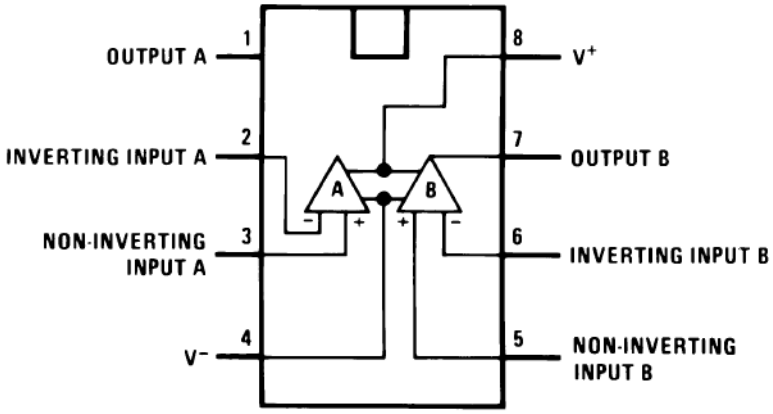

Figure 4.70: LM1458 Pin Configuration

4.61 Subcircuit Schematic Diagram

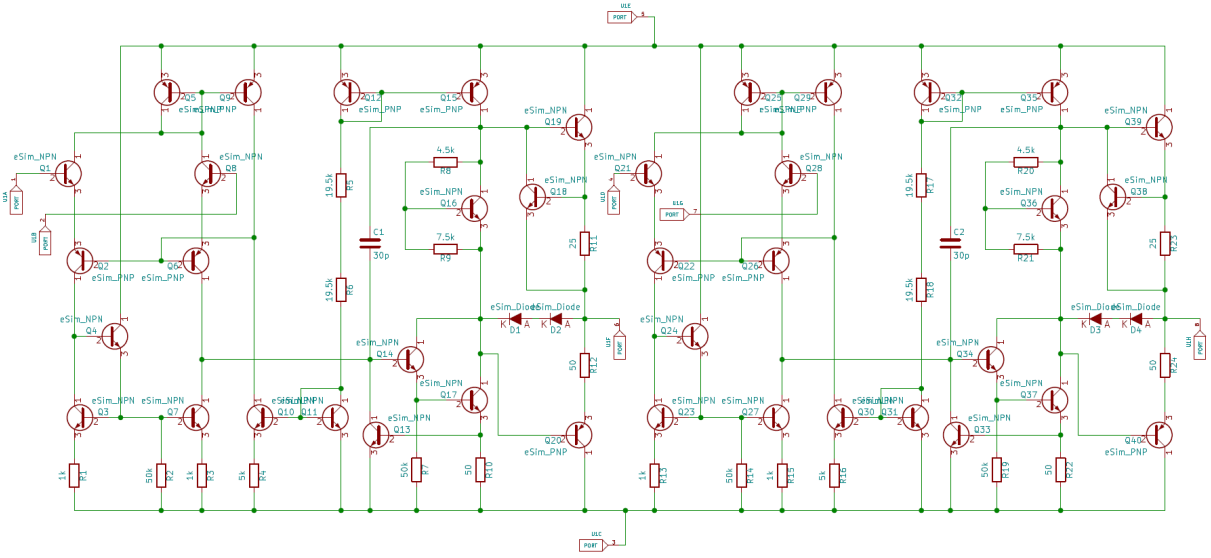

Figure 4.71: LM1458 Subcircuit Schematic Diagram

4.62 Schematic with external circuit

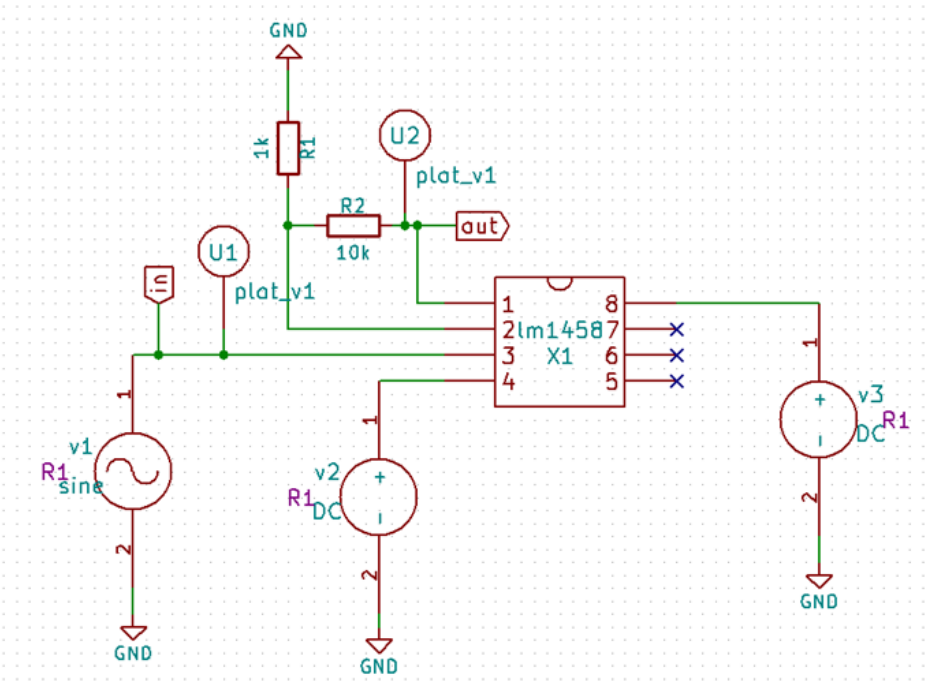

Figure 4.72: Non Inverting Amplifier

4.63 Ngspice Plots

4.63.1 Input plot

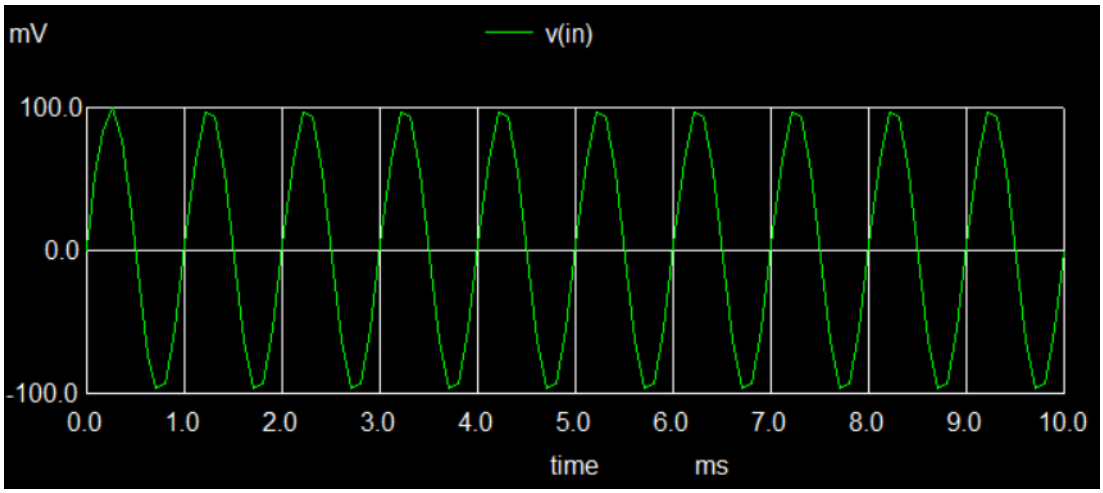

Figure 4.73: 0.1V Amplitude Sine wave input

4.63.2 Output plot

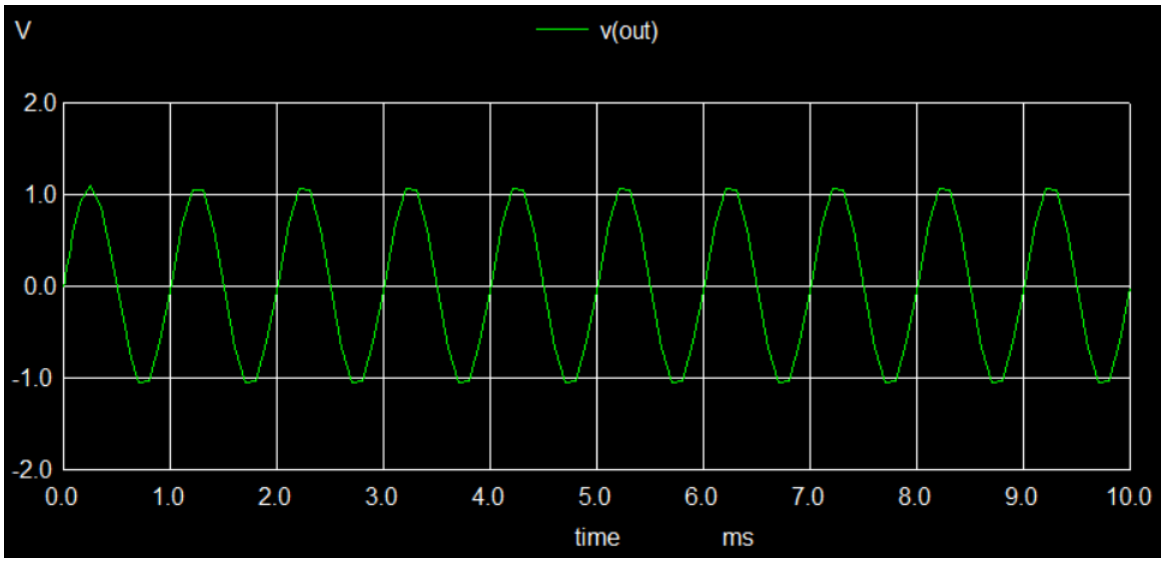

Figure 4.74: 1.1V Amplitude Amplified wave output

4.64 Schematic with external circuit

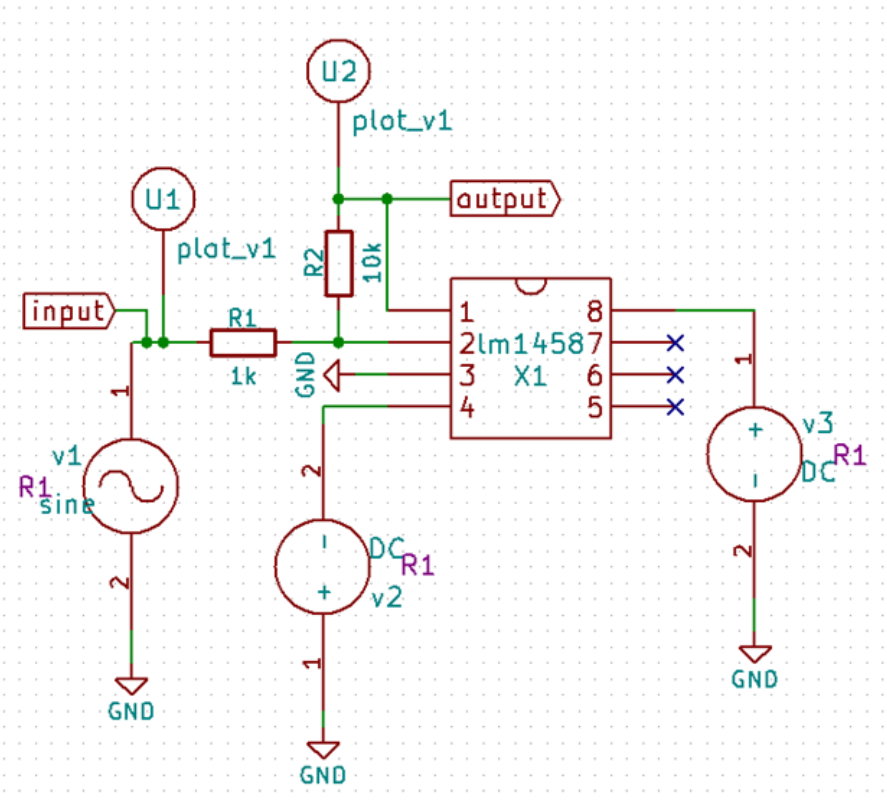

Figure 4.75: Inverting Amplifier

4.65 Ngspice Plots

4.65.1 Input plot

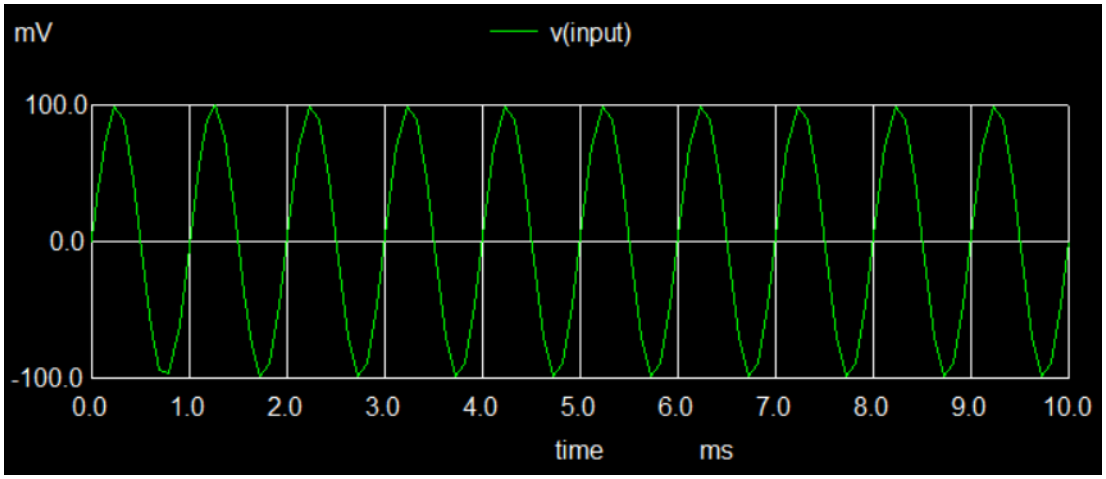

Figure 4.76: 0.1V Amplitude Sine wave input

4.65.2 Output plot

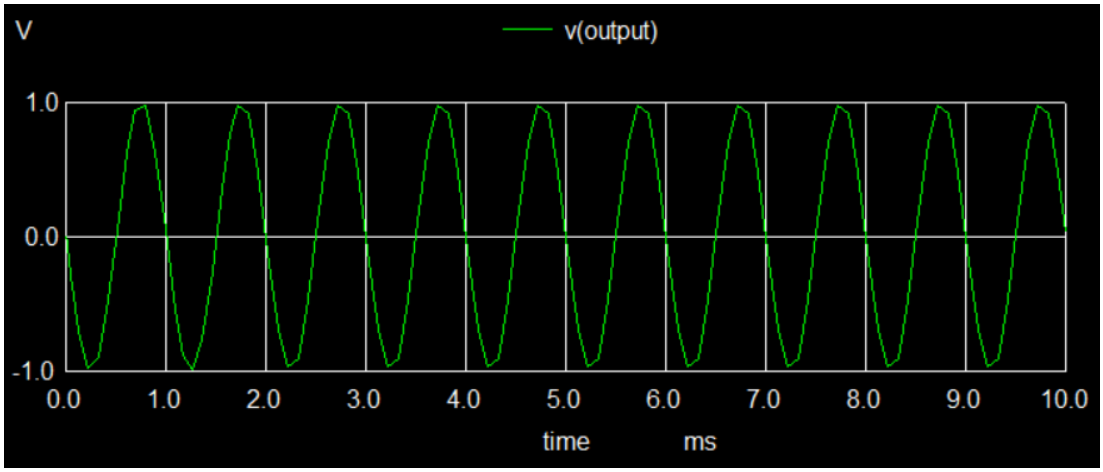

Figure 4.77: 1.1V Amplitude Amplified wave output

Chapter 5

Digital ICs

5.1 CD4081 IC

It is 2-input AND Gate IC. CD4081 [14] IC is designed with 180nm CMOS technology in eSim consisting four AND Gates. When both the inputs are HIGH then only output is HIGH, otherwise LOW.

5.2 Pin Configuration

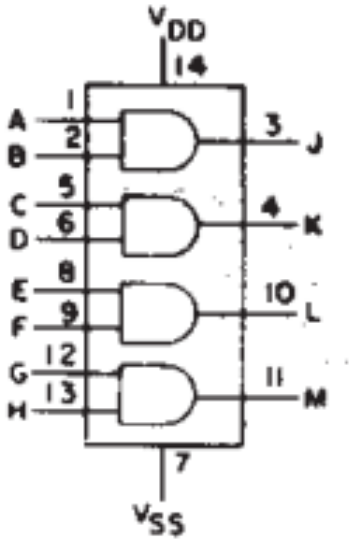

Figure 5.1: CD4081 Pin Configuration

5.3 CD4081 Subcircuit Schematic Diagram

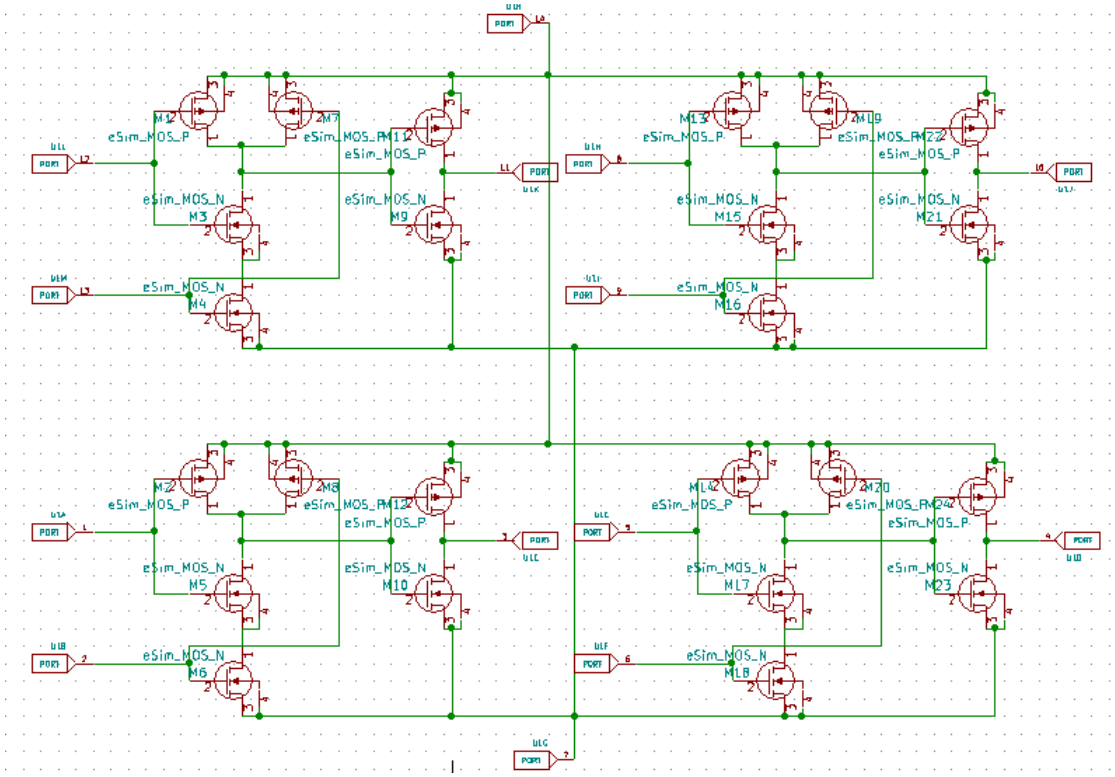

Figure 5.2: Subcircuit Schematic Diagram

5.4 Schematic with external circuit

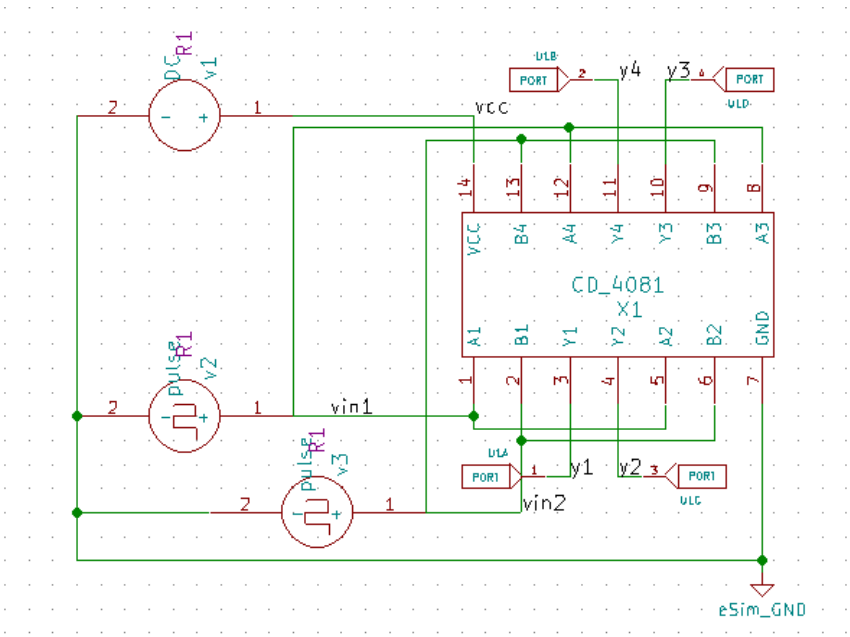

Figure 5.3: Schematic with external circuit

5.5 Ngspice Plots

5.5.1 Input Output plot

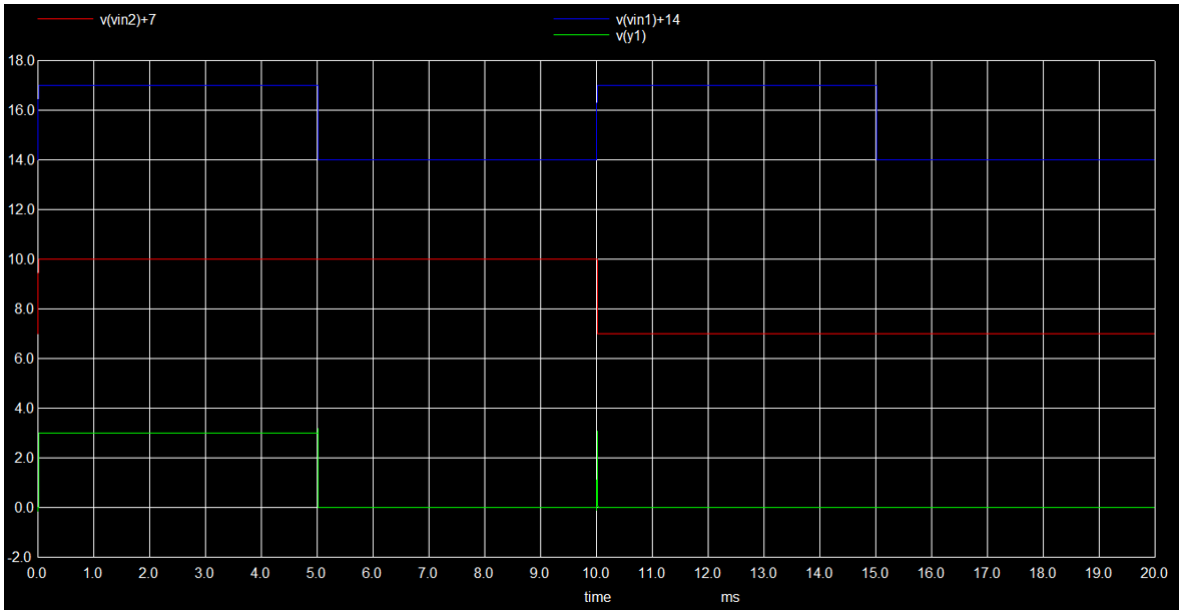

Figure 5.4: Input and Output

5.6 CD4071 IC

It is 2-input OR Gate IC. CD4071 [15] IC is designed with 180nm CMOS technology in eSim consisting four OR Gates. When both the inputs are LOW then only output is LOW, otherwise HIGH.

5.7 Pin Configuration

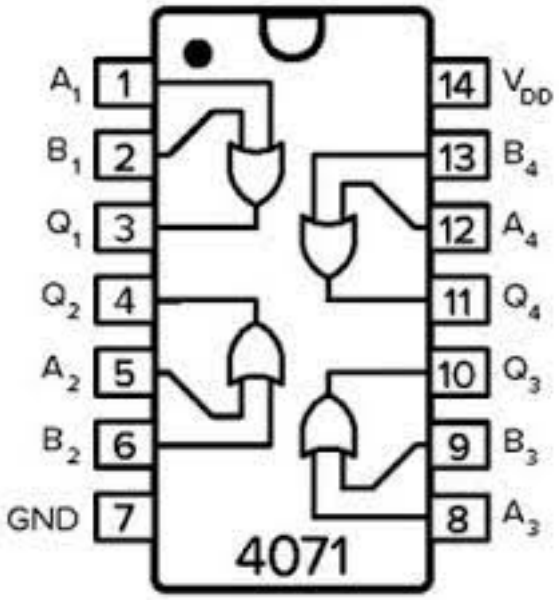

Figure 5.5: CD4071 Pin Configuration

5.8 Subcircuit Schematic Diagram

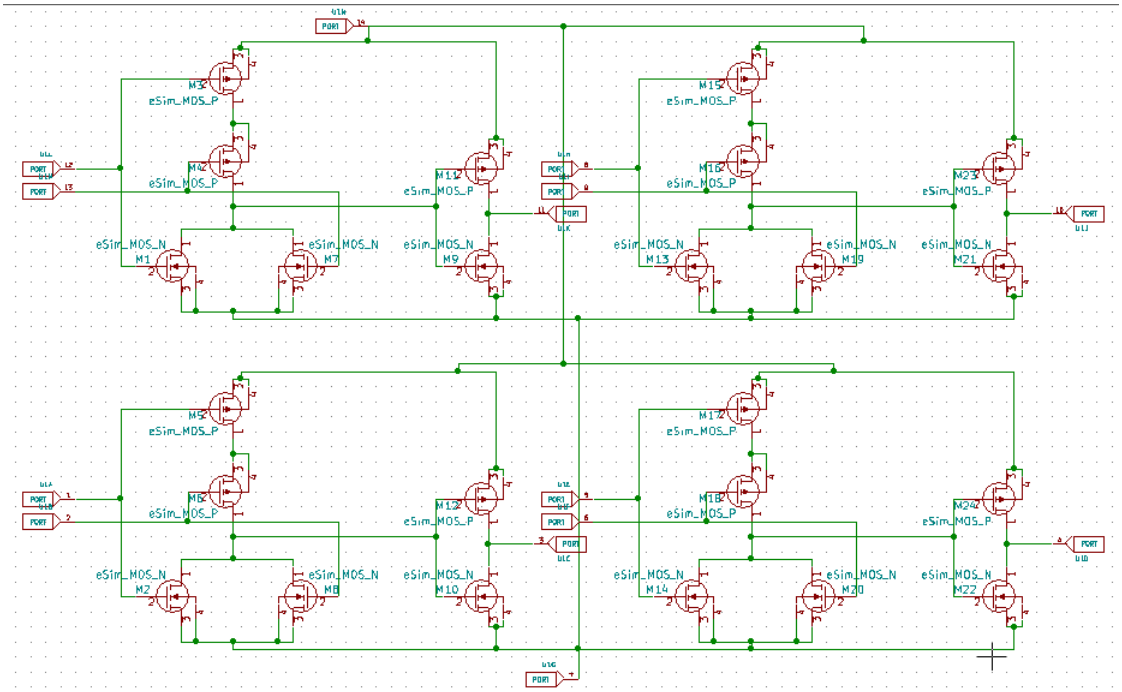

Figure 5.6: CD4071 Subcircuit Schematic Diagram

5.9 Schematic with external circuit

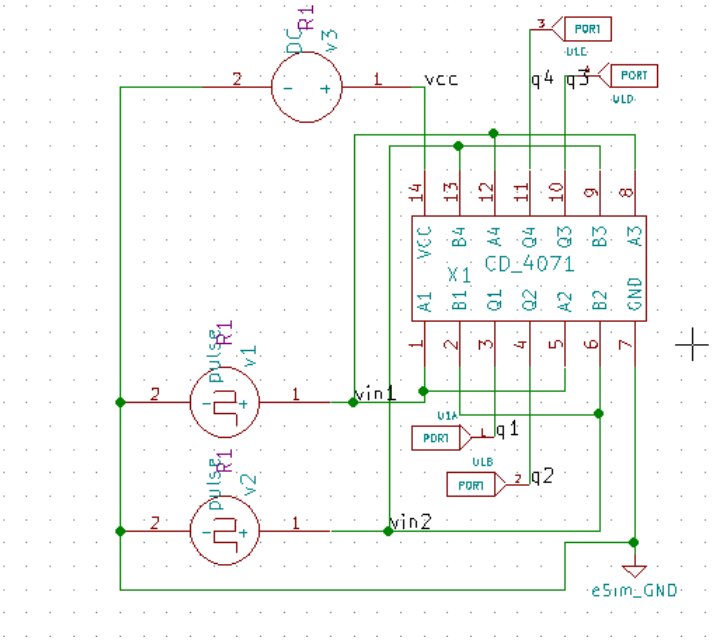

Figure 5.7: Schematic with external circuit

5.10 Ngspice Plots

5.10.1 Input Output plot

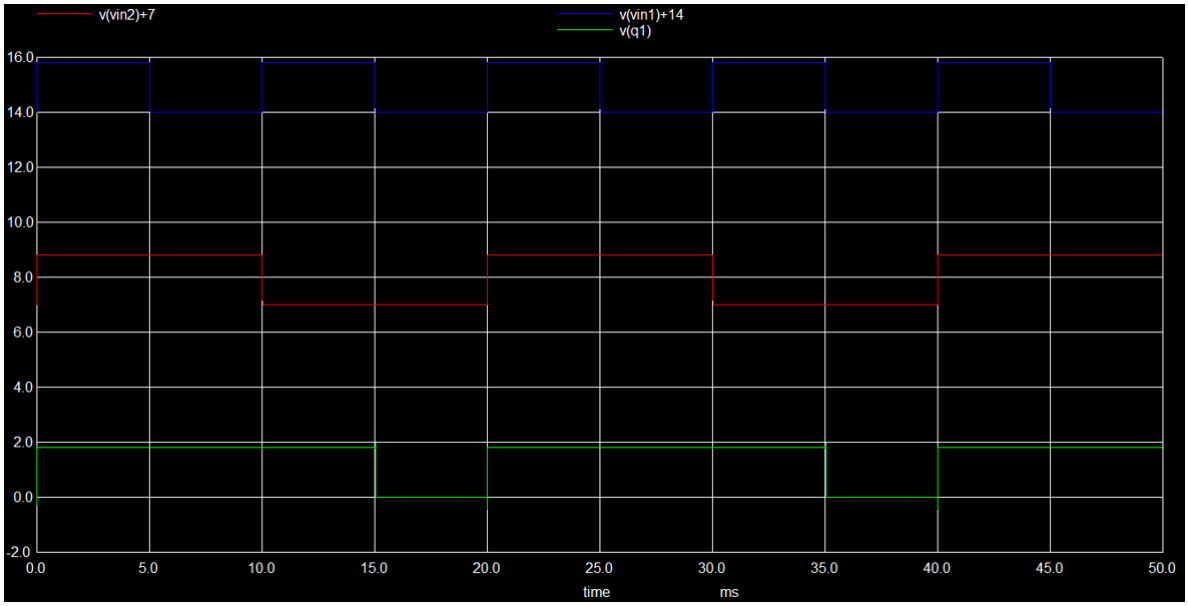

Figure 5.8: Input and Output

5.11 CD4011 IC

It is 2-input NAND Gate IC. CD4011 IC [16] is designed with 180nm CMOS technology in eSim consisting four NAND Gates. When both the inputs are HIGH then only output is LOW, otherwise HIGH. It is also called inverted AND Gate, a type of Universal Gate.

5.12 Pin Configuration

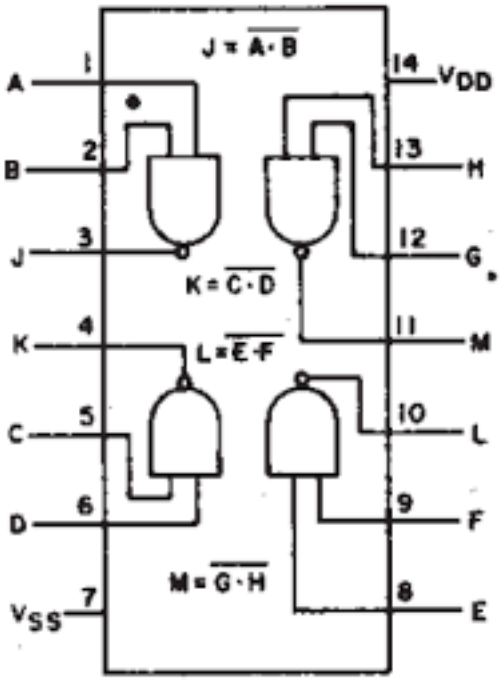

Figure 5.9: CD4011 Pin Configuration

5.13 Subcircuit Schematic Diagram

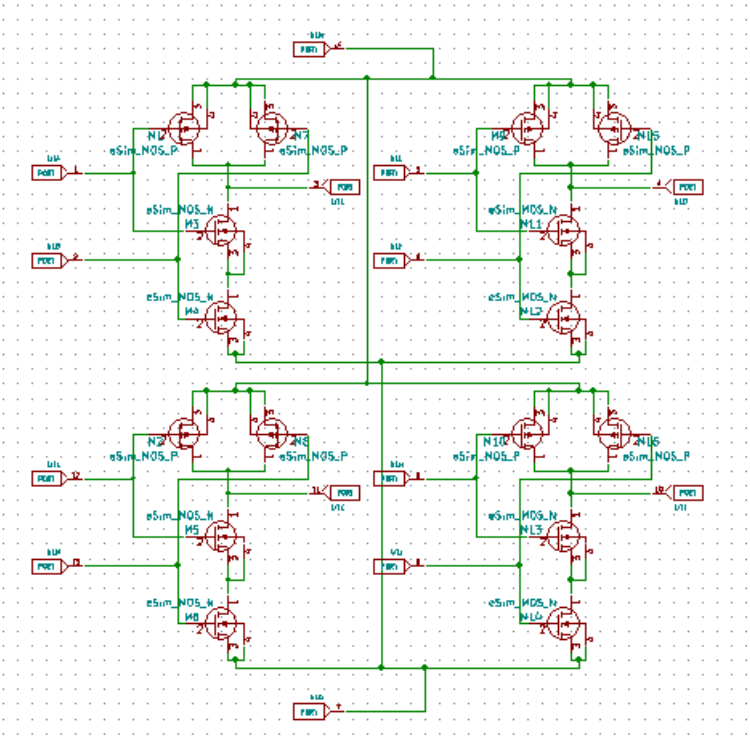

Figure 5.10: CD4011 Subcircuit Schematic Diagram

5.14 Schematic with external circuit

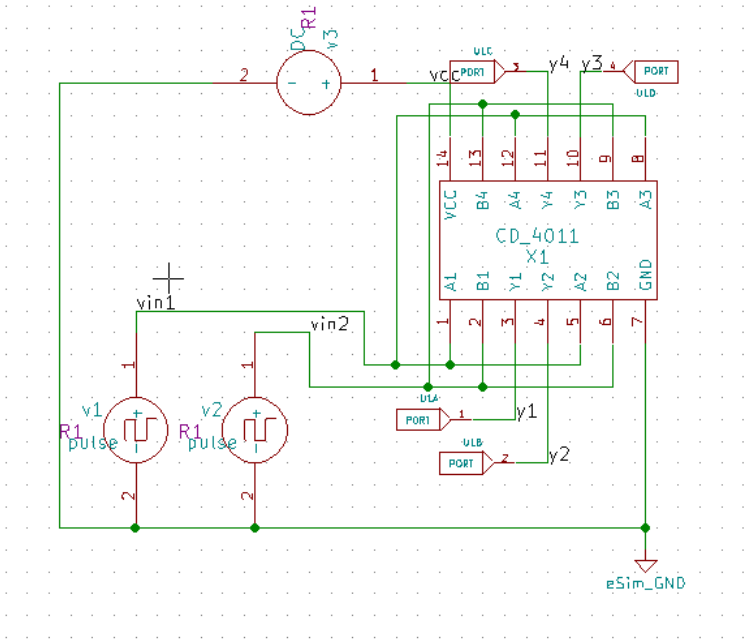

Figure 5.11: Schematic with external circuit

5.15 Ngspice Plots

5.15.1 Input Output plot

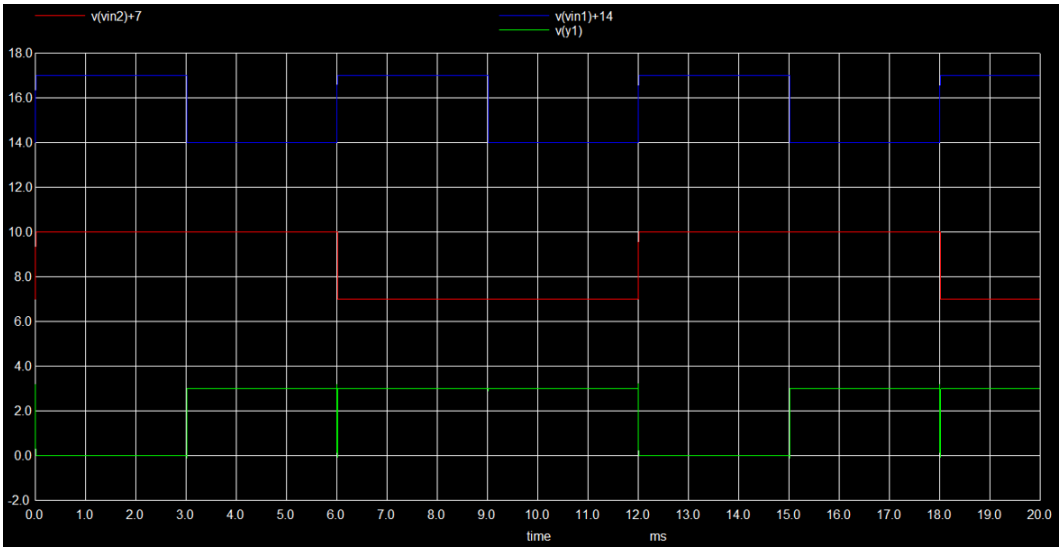

Figure 5.12: Input and Output

5.16 CD4001 IC

It is 2-input NOR Gate IC. CD4001 IC [17] is designed with 180nm CMOS technology in eSim consisting four NOT Gates. When both the inputs are LOW then only output is HIGH, otherwise LOW. It is also called inverted OR Gate, a type of Universal Gate.

5.17 Pin Configuration

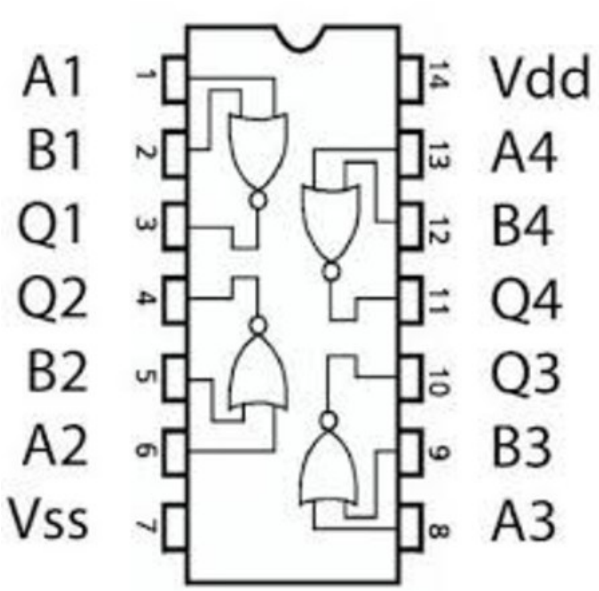

Figure 5.13: CD4001 Pin Configuration

5.18 CD4001 Subcircuit Schematic Diagram

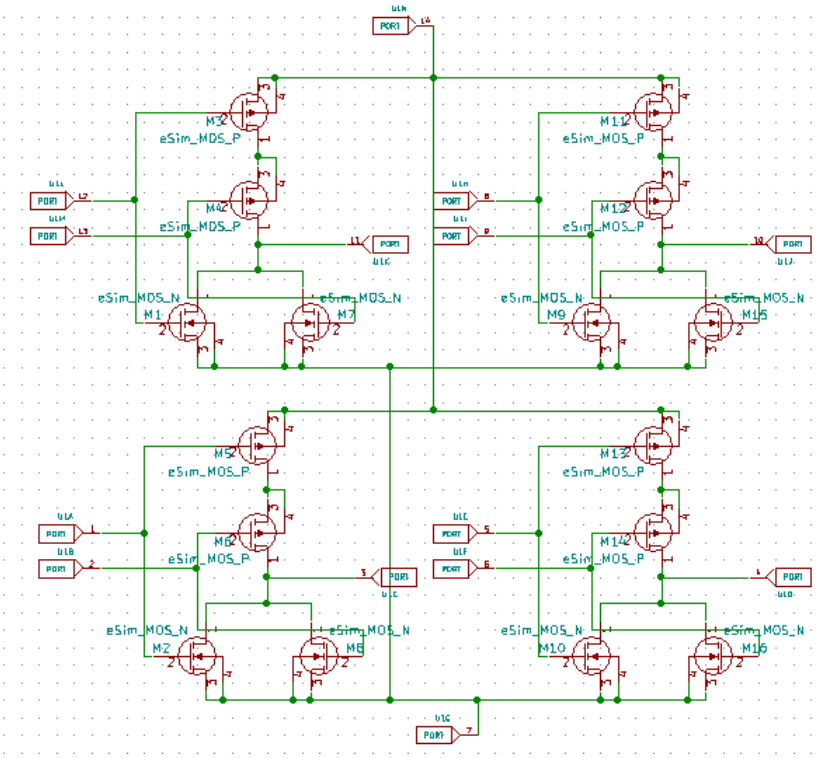

Figure 5.14: CD4001 Subcircuit Schematic Diagram

5.19 Schematic with external circuit

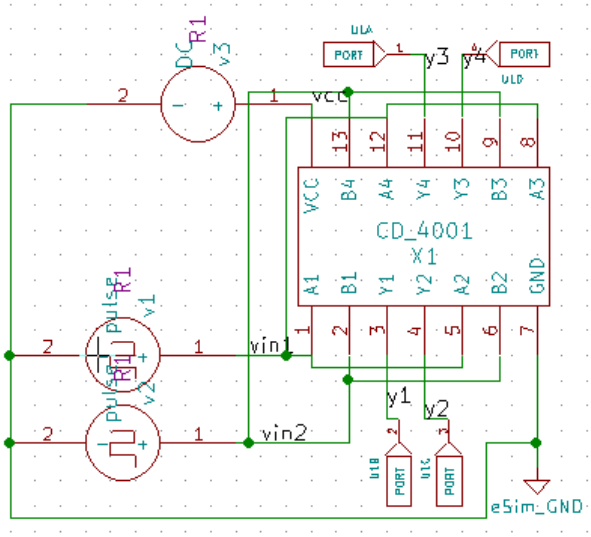

Figure 5.15: Schematic with external circuit

5.20 Ngspice Plots

5.20.1 Input Output plot

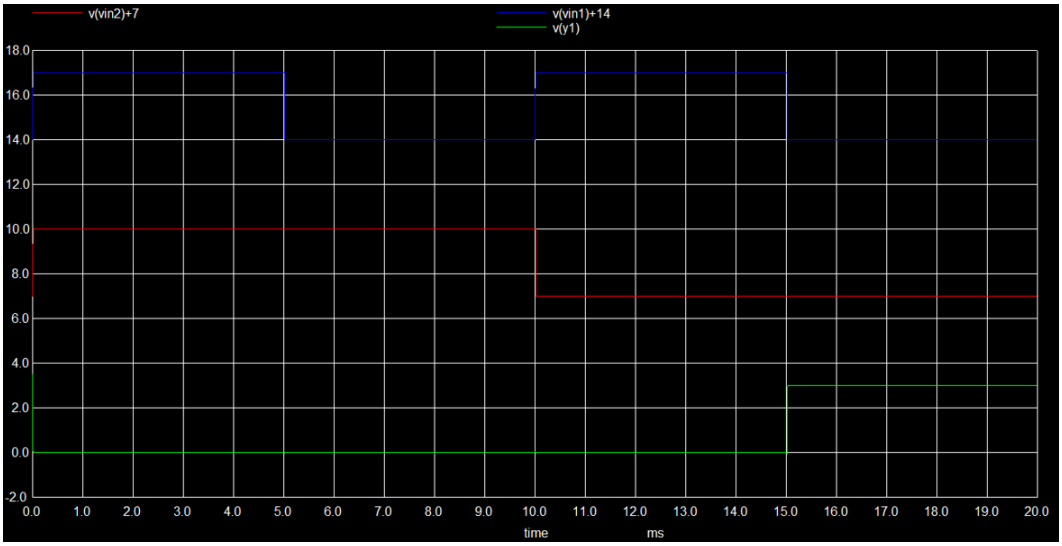

Figure 5.16: Input and Output

5.21 CD4023 IC

It is 3-input NAND Gate IC. CD4023 IC [18] is designed with 180nm CMOS technology in eSim consisting three NAND Gates. When both the inputs are HIGH then only output is LOW, otherwise HIGH. It is also called inverted AND Gate, a type of Universal logic Gate.

5.22 Pin Configuration

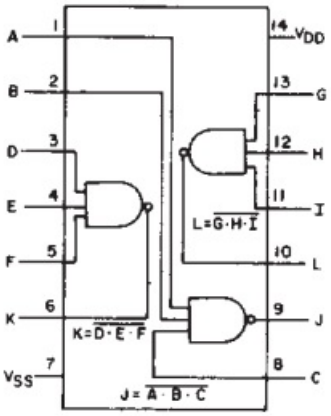

Figure 5.17: CD4023 Pin Configuration

5.23 Subcircuit Schematic Diagram

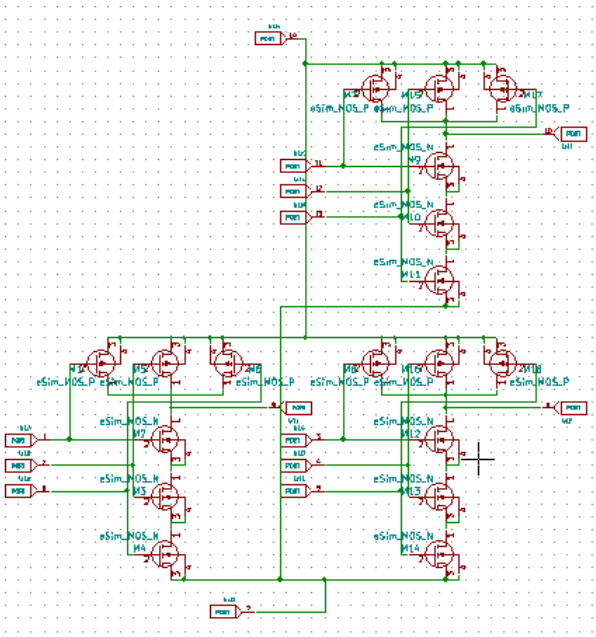

Figure 5.18: CD4023 Subcircuit Schematic Diagram

5.24 Schematic with external circuit

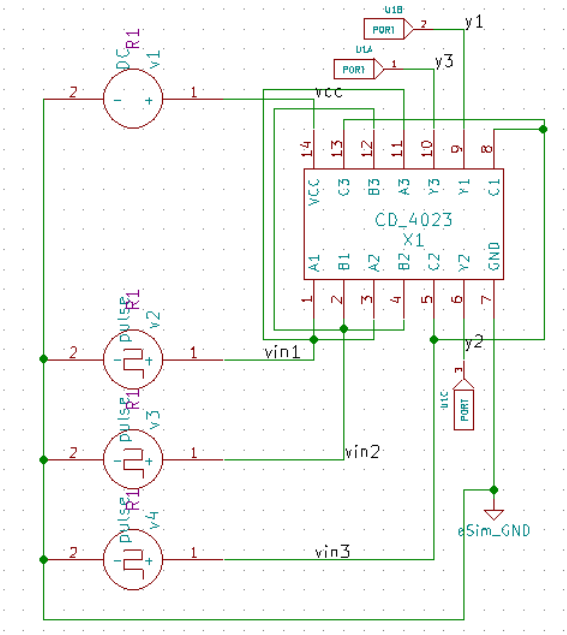

Figure 5.19: Schematic with external circuit

5.25 Ngspice Plots

5.25.1 Input Output plot

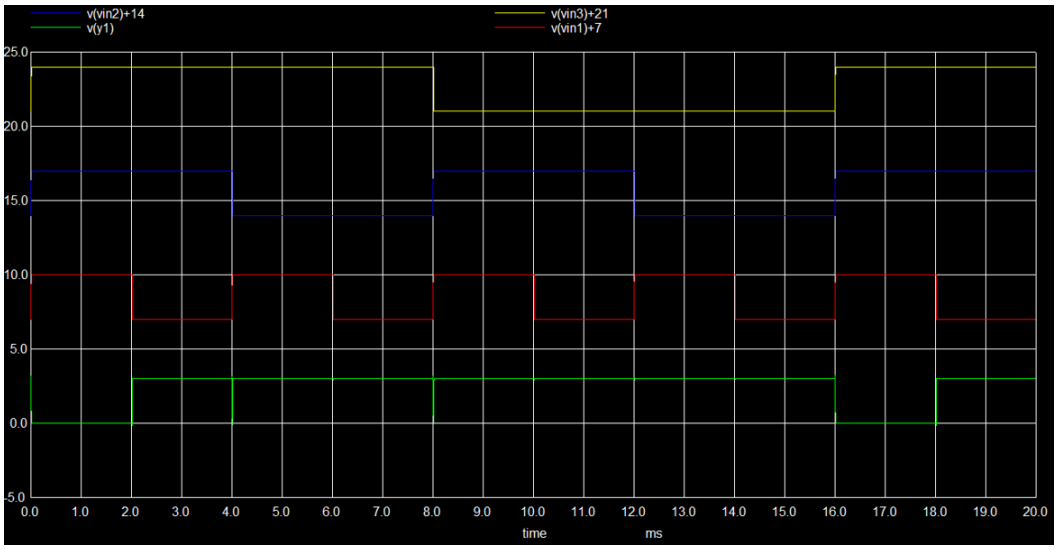

Figure 5.20: Input and Output

5.26 CD4070 IC

It is 2-input XOR Gate IC. CD4070 IC [19] is designed with 180nm CMOS technology in eSim consisting four XOR Gates. It plays the role of odd 1's detector. When both inputs are same, then output is LOW. It is also known as Special logic Gate.

5.27 Pin Configuration

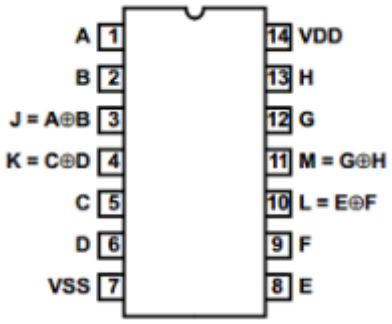

Figure 5.21: Pin Configuration

5.28 Subcircuit Schematic Diagram

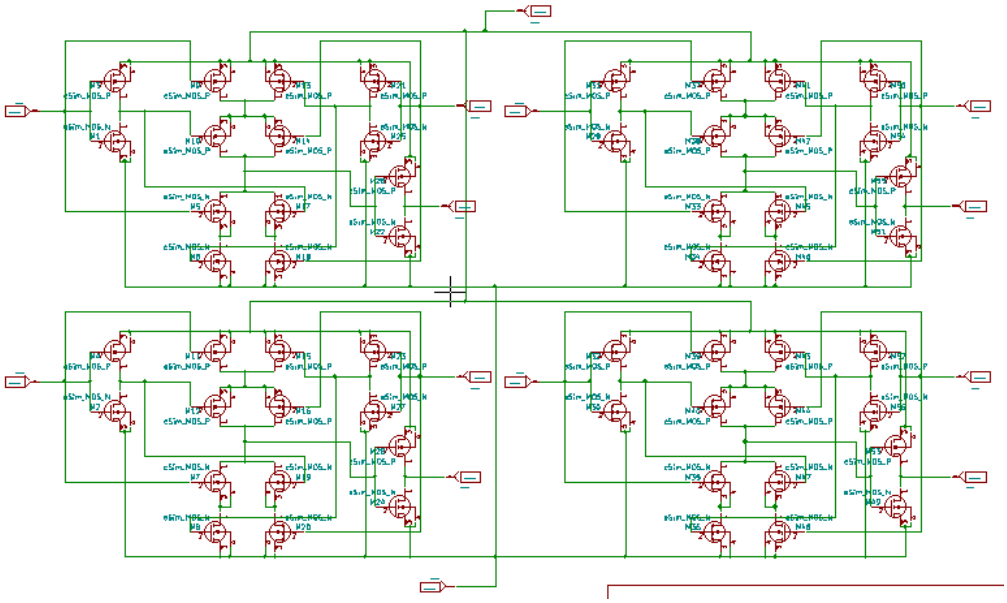

Figure 5.22: CD4070 Subcircuit Schematic Diagram

5.29 Schematic with external circuit

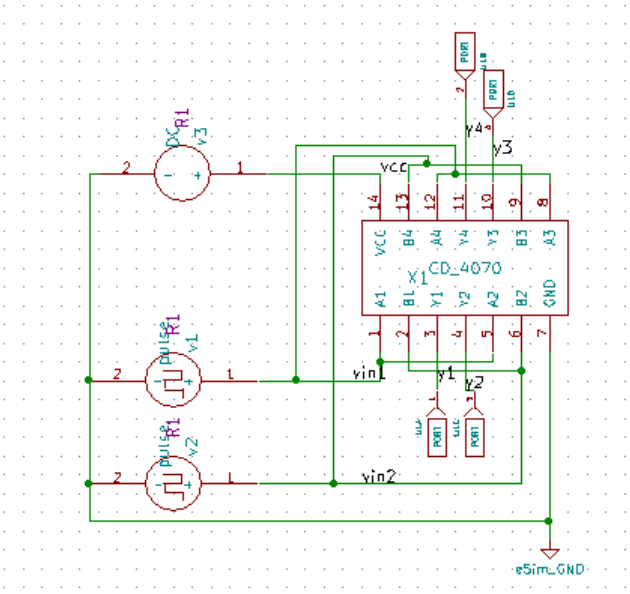

Figure 5.23: Schematic with external circuit

5.30 Ngspice Plots

5.30.1 Input Output plot

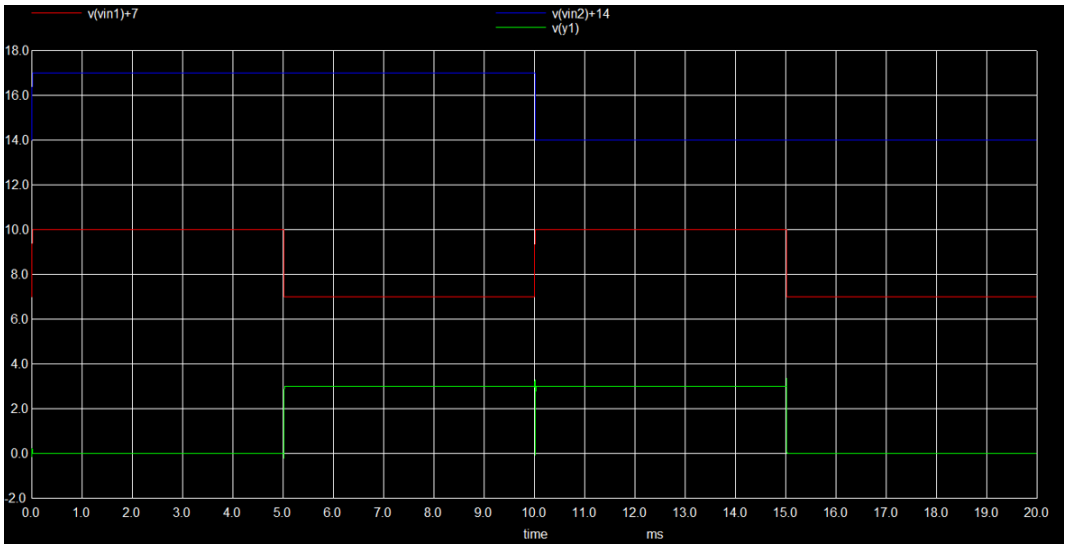

Figure 5.24: Input and Output

5.31 CD4077 IC

It is 2-input XNOR Gate IC. CD4077 IC [20] is designed with 180nm CMOS technology in eSim consisting four XNOR Gates. It plays the role of even 1's detector. When both inputs are same, then output is HIGH, else LOW. It is also known as Special logic Gate.

5.32 Pin Configuration

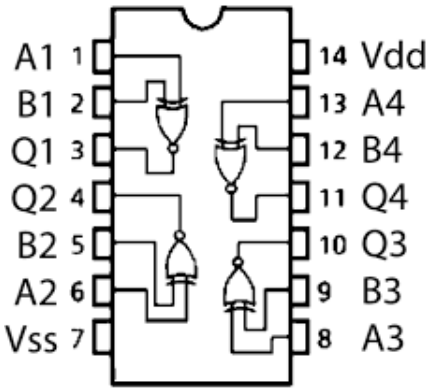

Figure 5.25: Pin Configuration

5.33 Subcircuit Schematic Diagram

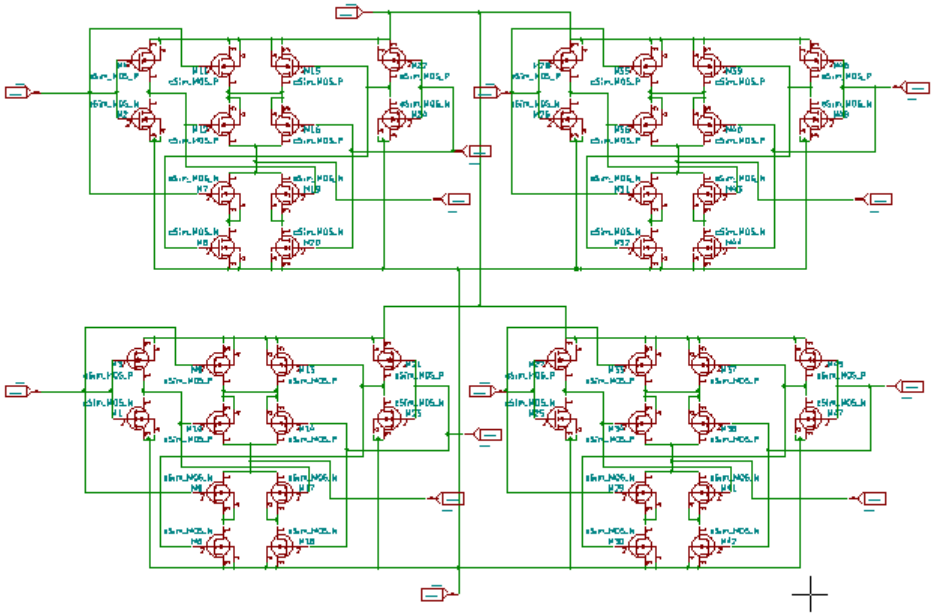

Figure 5.26: CD4077 Subcircuit Schematic Diagram

5.34 Schematic with external circuit

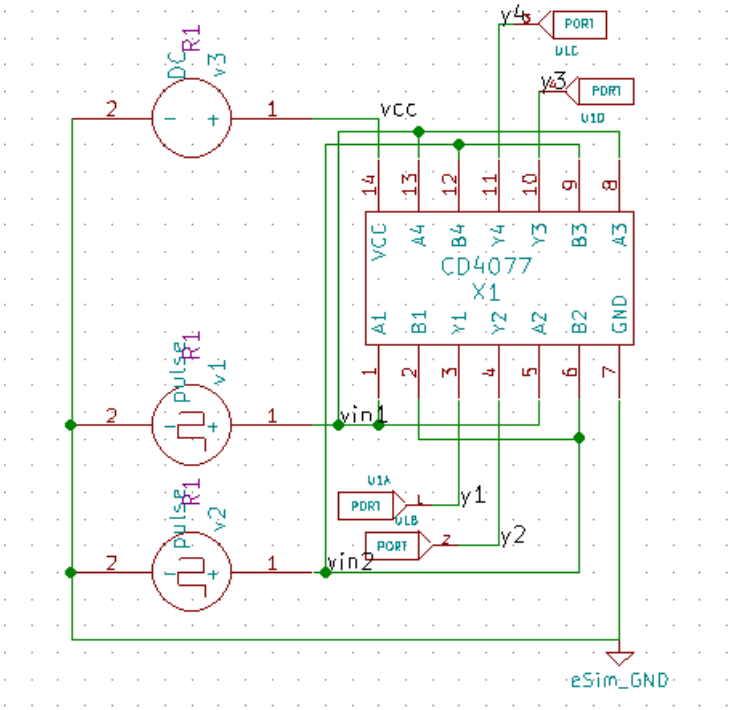

Figure 5.27: Schematic with external circuit

5.35 Ngspice Plots

5.35.1 Input Output plot

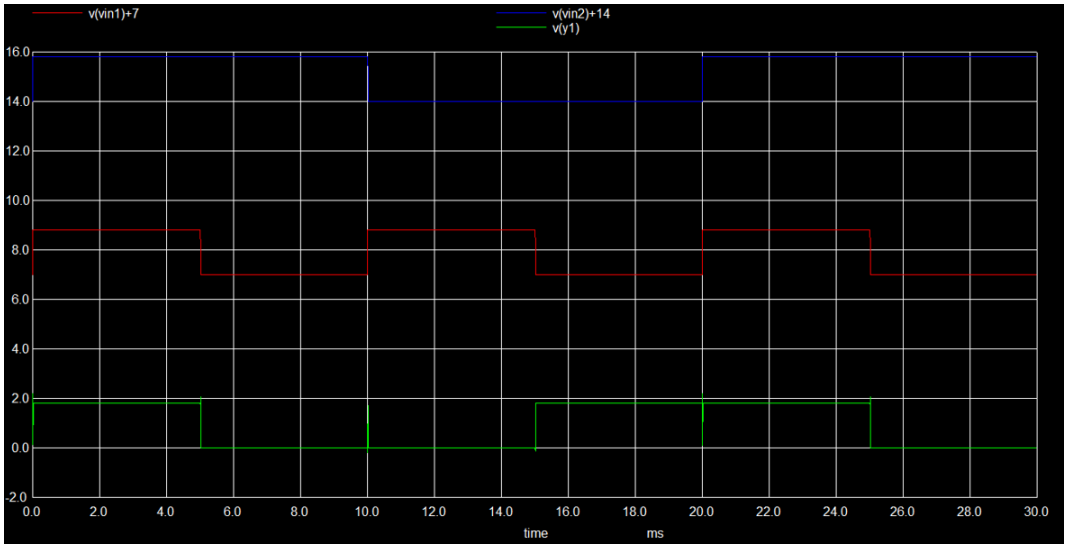

Figure 5.28: Input and Output

5.36 CD4000 IC

It is dual 3-input NOR Gate IC. CD4000 IC [21] is designed with 180nm CMOS technology in eSim consisting two NOR Gates and one NOT Gate. When all the inputs are LOW, then only output is HIGH, else LOW for NOR gate and NOT gate inverts the input as output.

5.37 Pin Configuration

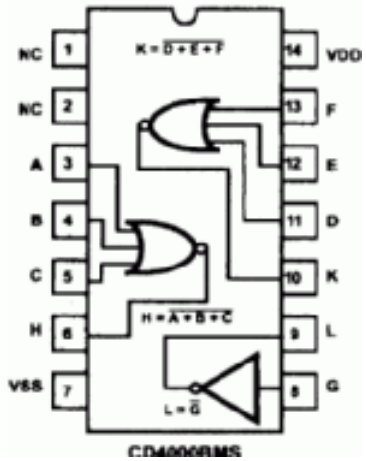

Figure 5.29: CD4000 Pin Configuration

5.38 Subcircuit Schematic Diagram

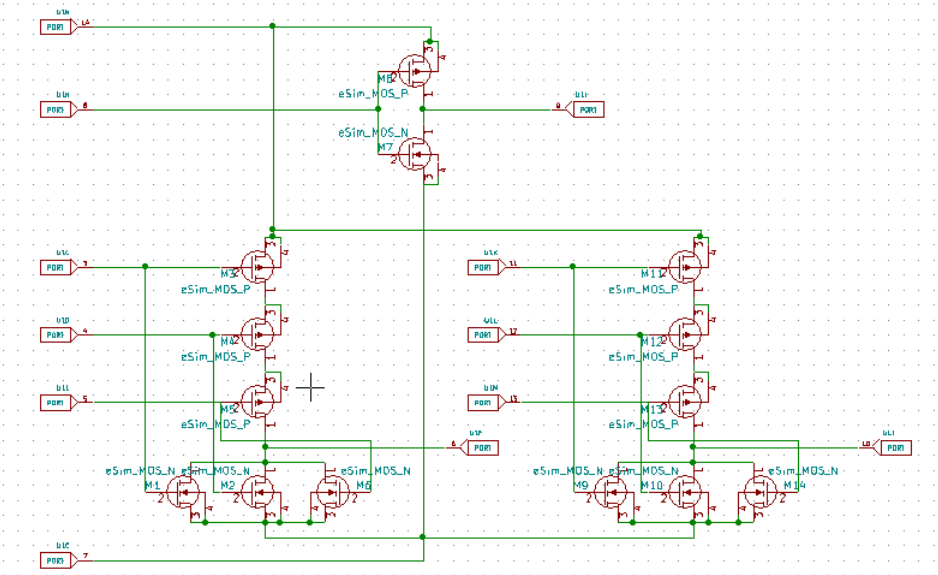

Figure 5.30: CD4000 Subcircuit Schematic Diagram

5.39 Schematic with external circuit

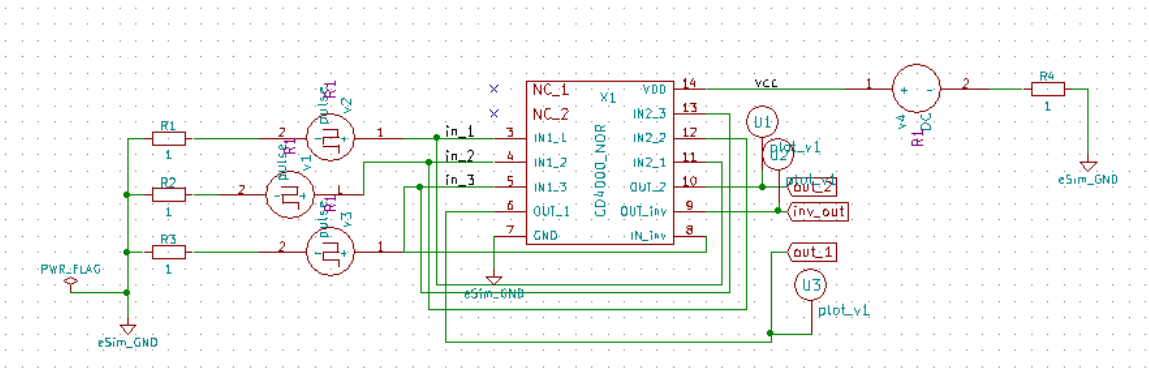

Figure 5.31: Schematic with external circuit

5.40 Ngspice Plots

5.40.1 Input Output plot

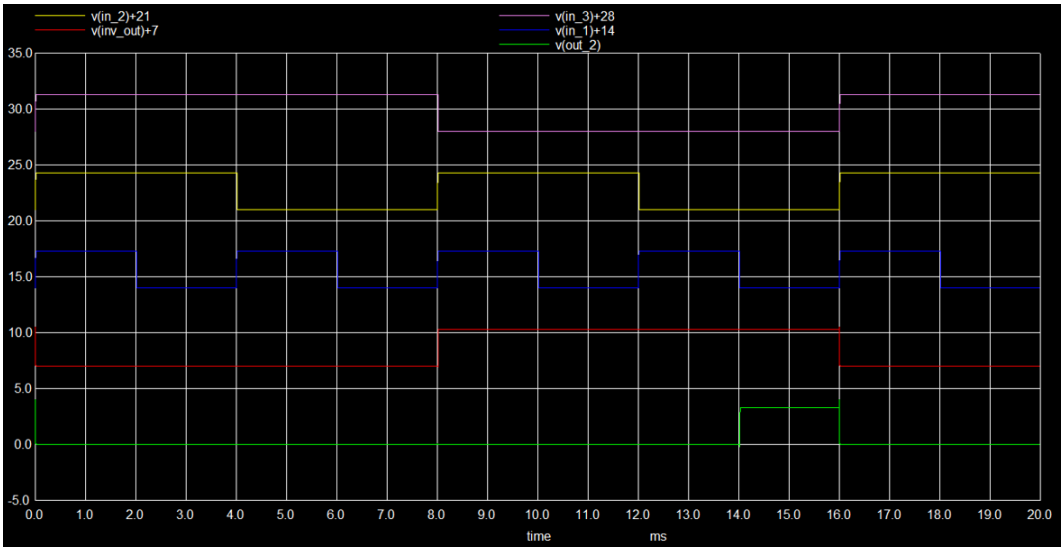

Figure 5.32: Input and Output

5.41 CD4069 IC

It is Hex NOT Gate IC. CD4069 IC [22] is designed with 180nm CMOS technology in eSim consisting six NOR Gates. When all the input is LOW, then only output is HIGH, and vice-versa. It is also known as Inverter Gate.

5.42 Pin Configuration

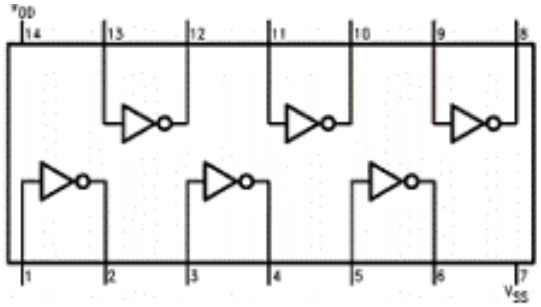

Figure 5.33: CD4069 Pin Configuration

5.43 Subcircuit Schematic Diagram

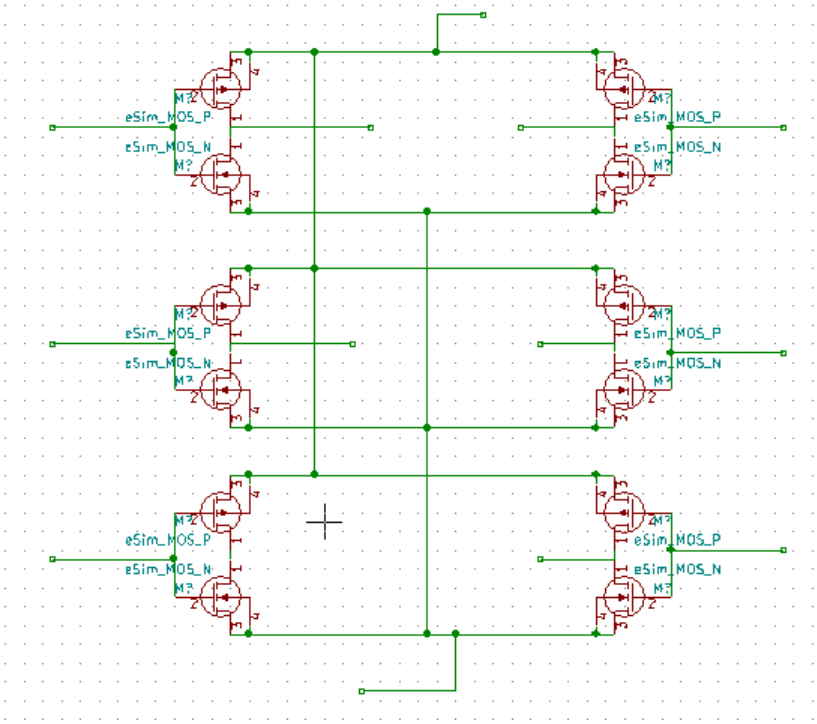

Figure 5.34: CD4069 Subcircuit Schematic Diagram

5.44 Schematic with external circuit

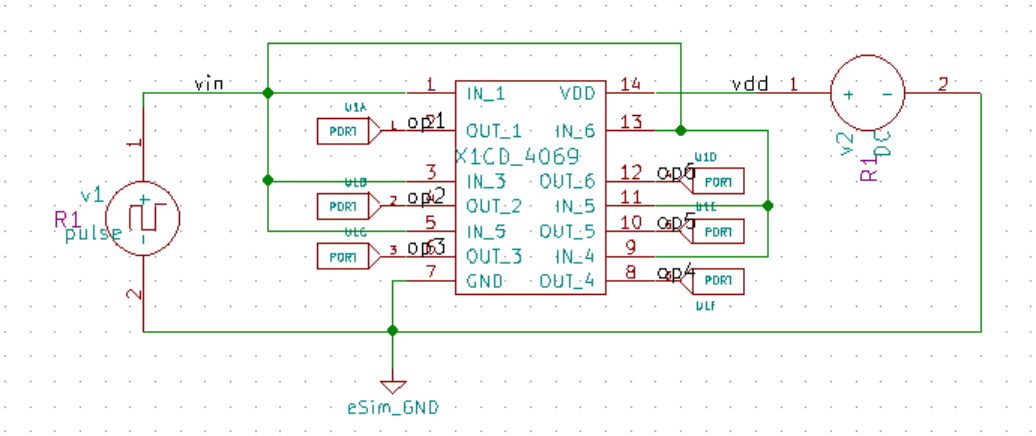

Figure 5.35: Schematic with external circuit

5.45 Ngspice Plots

5.45.1 Input Output plot

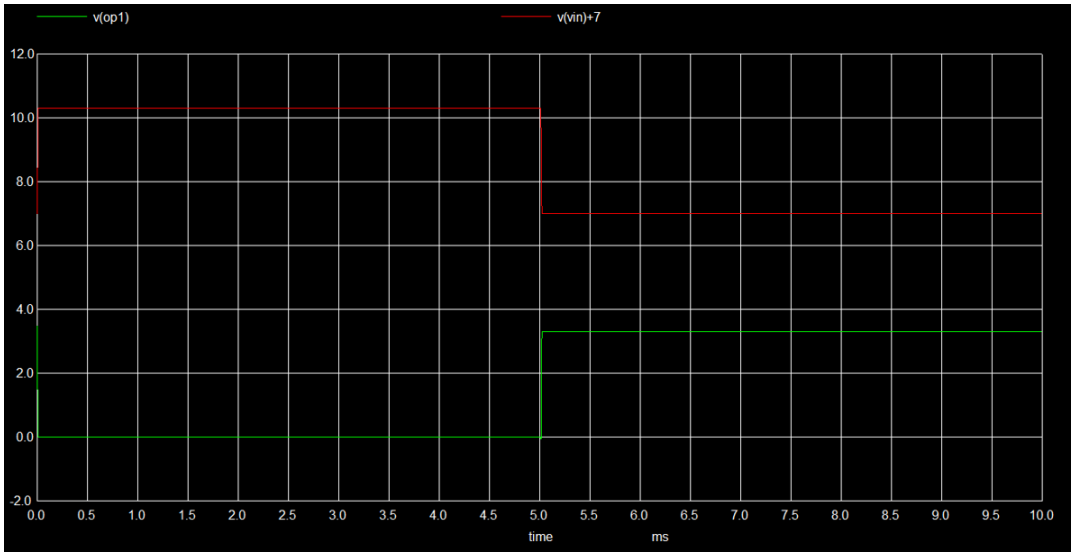

Figure 5.36: Input and Output

5.46 CD54HC157 IC

It is 2:1 Multiplexer IC. CD54HC157 IC [23] is designed with 180nm CMOS technology in eSim. It is 16 pin IC. The output depends on the select lines. Here the output is inverted as you can see in fig 3.28. If Select line is 1, output is I1.

5.47 Pin Configuration

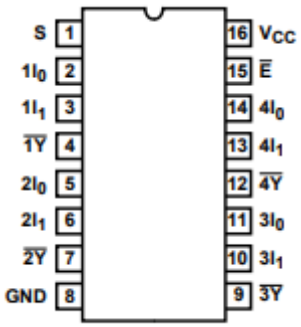

Figure 5.37: CD54HC157 Pin Configuration

5.48 Subcircuit Schematic Diagram

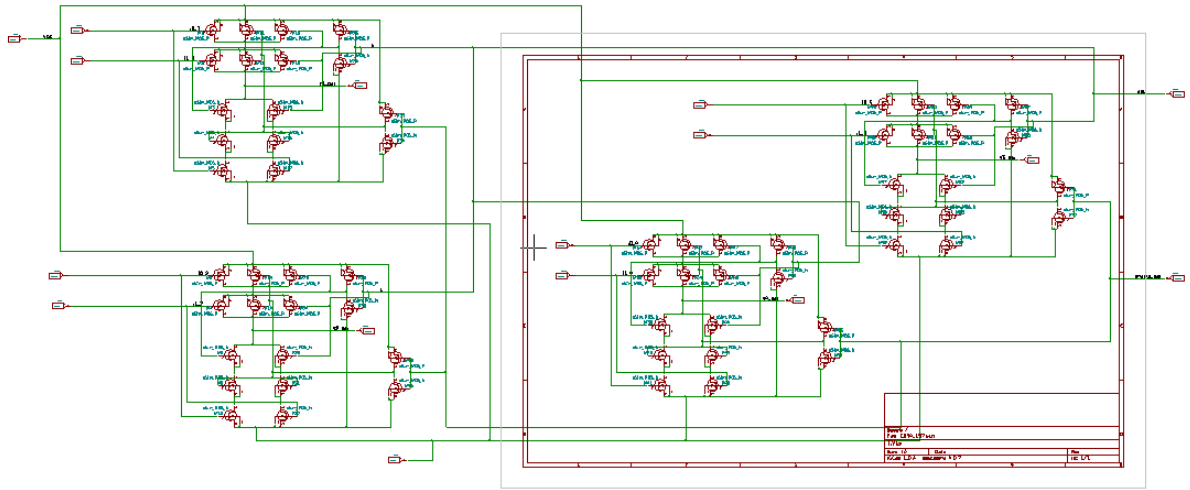

Figure 5.38: CD54HC157 Subcircuit Schematic Diagram

5.49 Schematic with external circuit

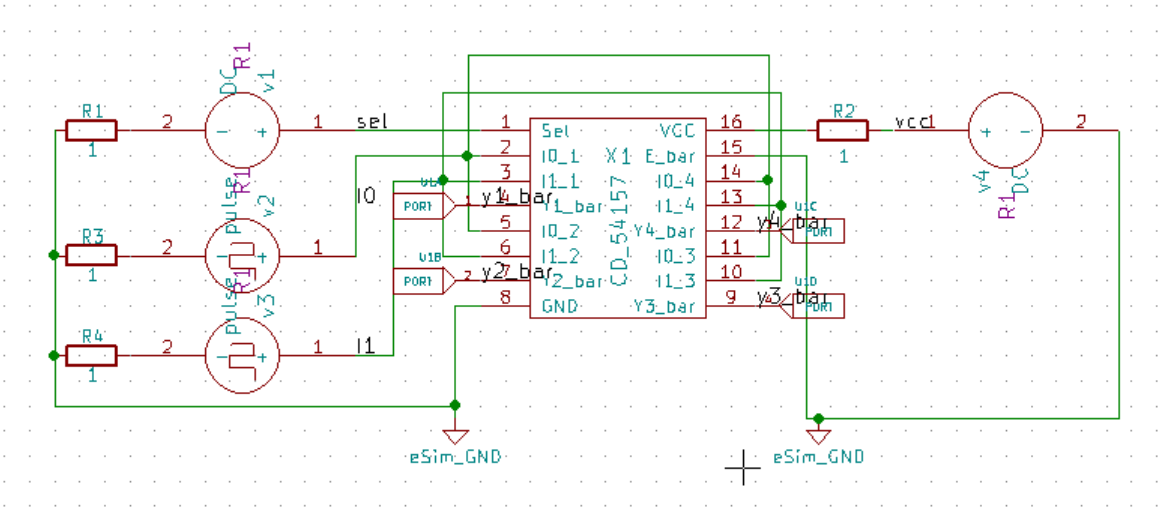

Figure 5.39: Schematic with external circuit

5.50 Ngspice Plots

5.50.1 Input Output plot

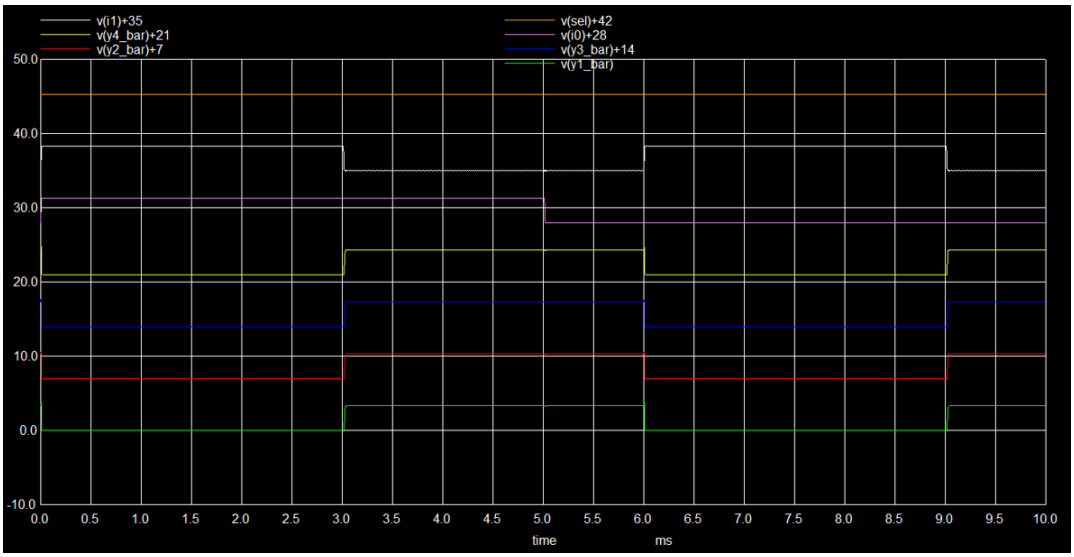

Figure 5.40: Input and Output

5.51 74LVC1G19 IC

Demux is the de-multiplexer circuit that takes one input line and gives multiple output lines. Basically, it's a combinational circuit and It always takes one input line and gives 2^n output line, where n is the number of select lines. It is also, known as a serial to parallel converter or data distributor circuit. The 1:2 Demux consist of 1 input line, 1 select line, and produces 2 output line. as, according to the formula no. of the output line is depends on no. of select line, here, in 1:2 demux, no. of output line = $2^n = 2^1 = 2$.

5.52 Pin Configuration

It's a 6 pin IC named 74LVC1G19 [24] (1:2 DEMUX IC) .

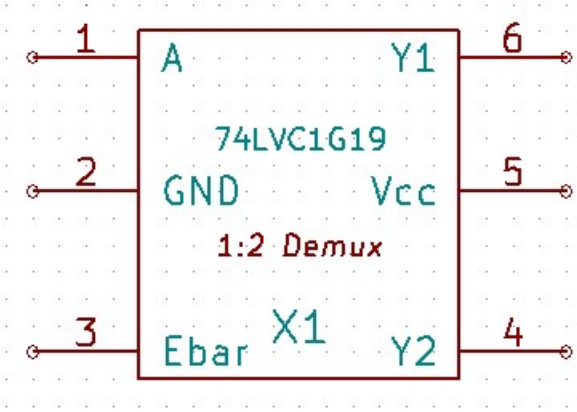

Figure 5.41: Pin Configuration

The name of all pins are

Pin No.	Pin Name	Pin Description
1	A	Input pin of demux.
2	GND	It represents ground.
3	Ebar	It is a select line/enable line.
4	Y2	It represents 2nd Output line.
5	VCC	It represents Input power supply.
6	Y1	It represents 1st Output line.

5.53 Subcircuit Schematic Diagram

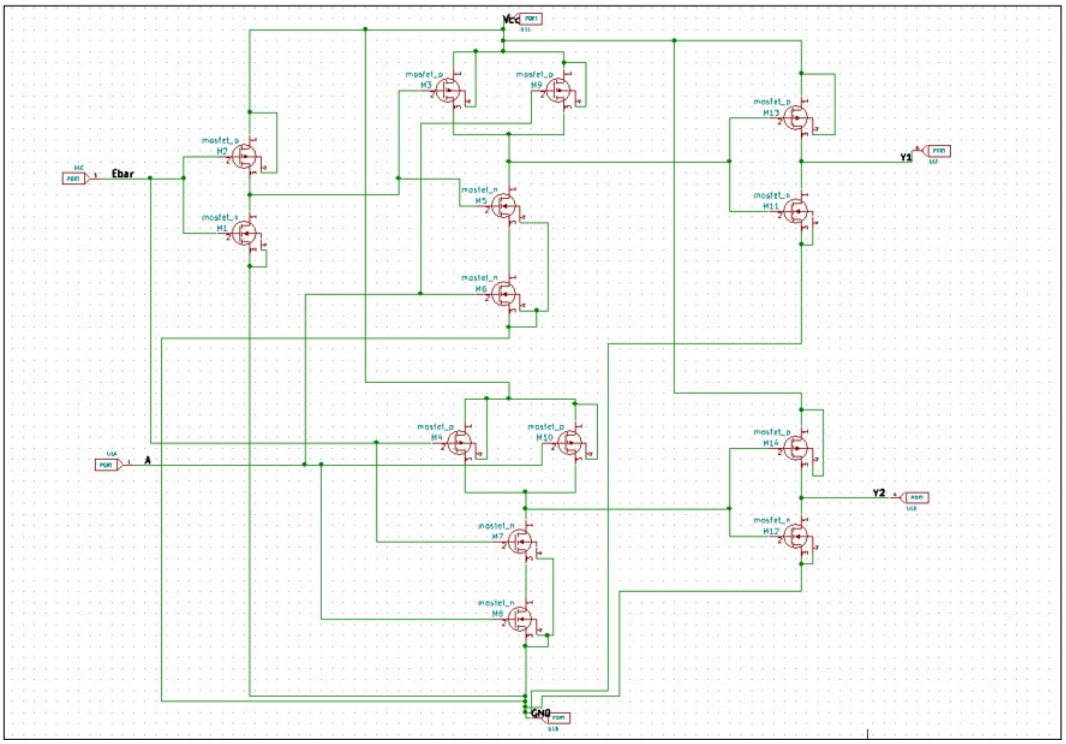

Figure 5.42: 74LVC1G19 Subcircuit Schematic Diagram

5.54 Schematic with external circuit

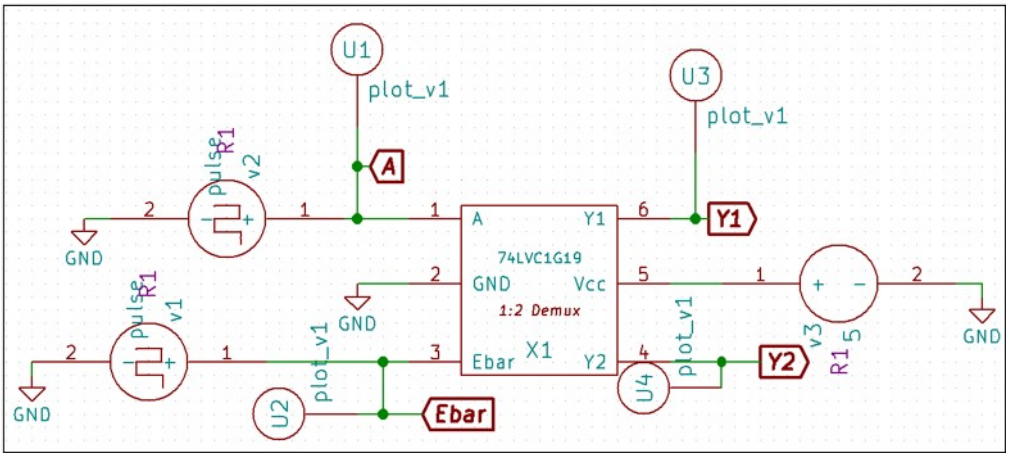

Figure 5.43: Schematic with external circuit

5.55 Ngspice Plots

5.55.1 Input Output plot

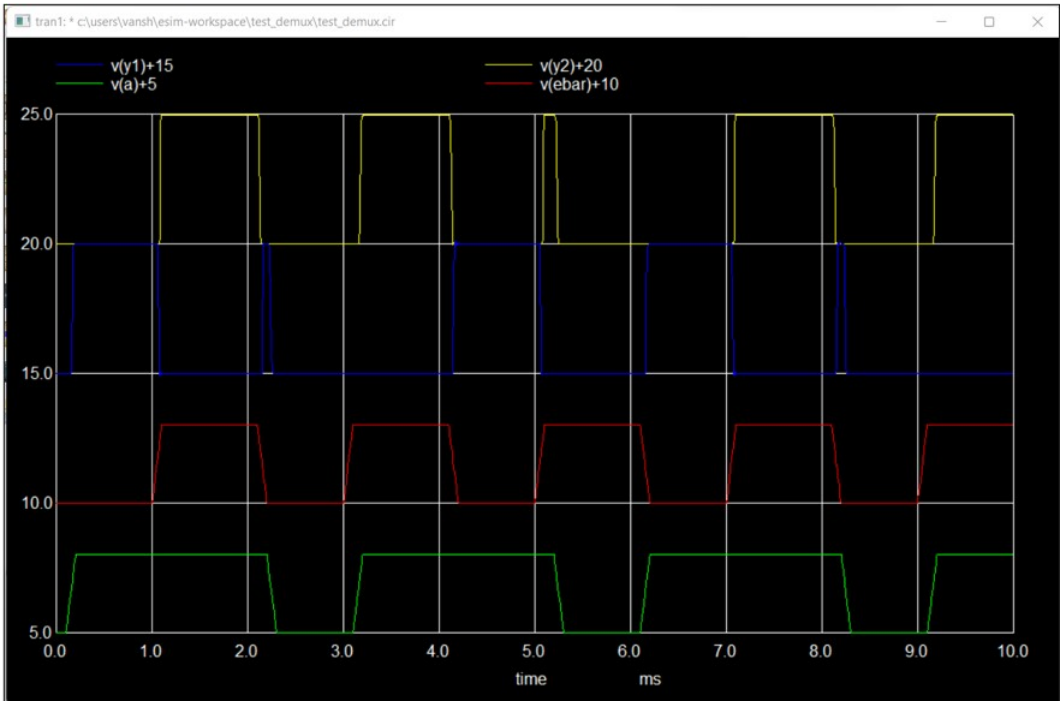

Figure 5.44: Input and Output

5.56 CD54HC153 IC

It is 4:1 Multiplexer IC. CD54HC153 IC [25] is designed with 180nm CMOS technology in eSim. It is 16 pin IC. The output depends on the select lines. Here the output is not inverted as you can see below. If Select lines 0,0 output is I0.

5.57 Pin Configuration

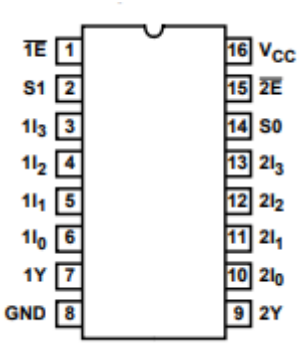

Figure 5.45: CD54HC153 Pin Configuration

5.58 Subcircuit Schematic Diagram

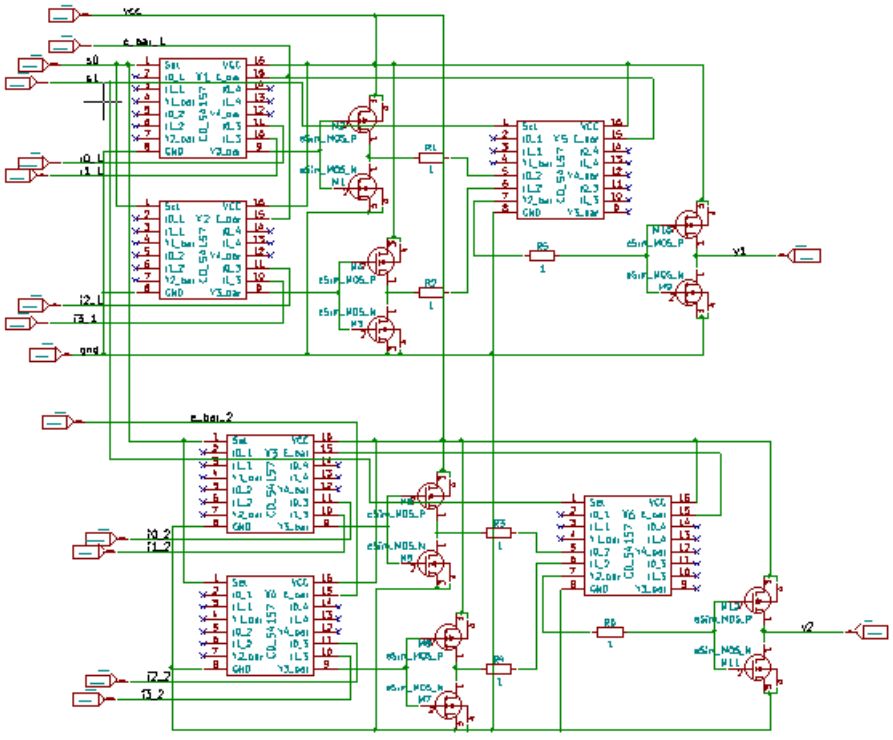

Figure 5.46: CD54HC153 Subcircuit Schematic Diagram

5.59 Schematic with external circuit

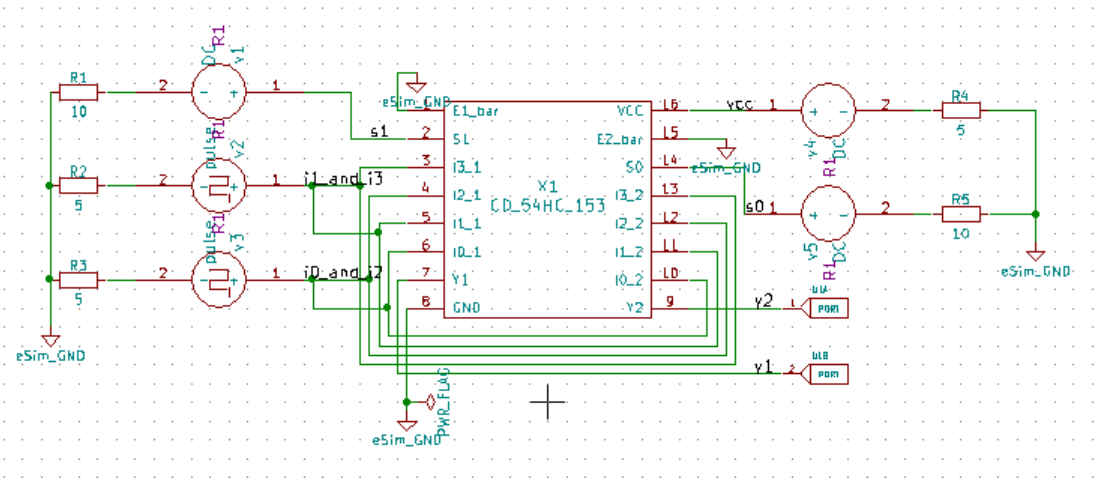

Figure 5.47: Schematic with external circuit

5.60 Ngspice Plots

5.60.1 Input Output plot

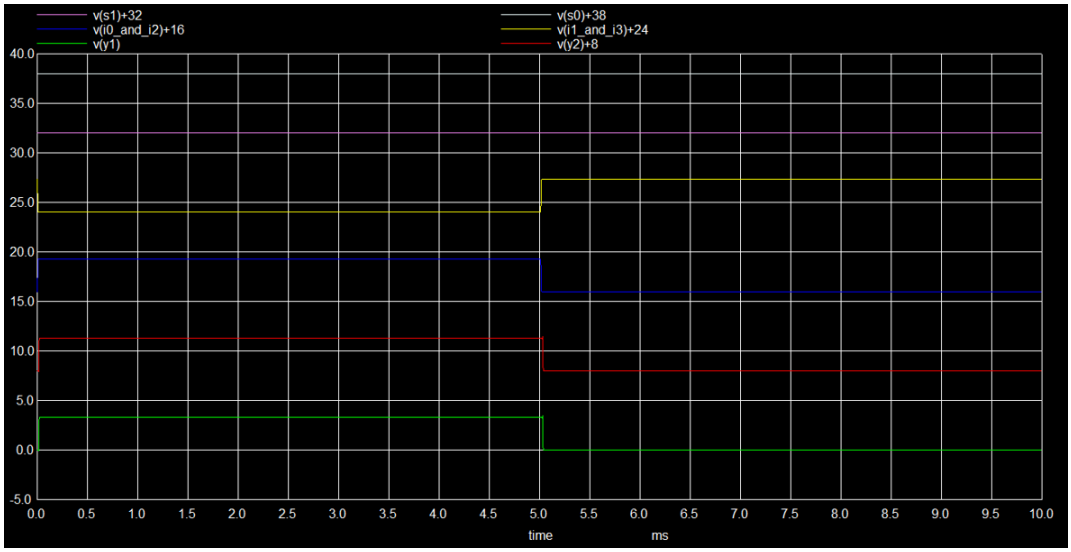

Figure 5.48: Input and Output

5.61 CD54HC151 IC

It is 8:1 Multiplexer IC. CD54HC151 IC [26] is designed with 180nm CMOS technology in eSim. It is 16 pin IC. The output depends on the select lines.

5.62 Pin Configuration

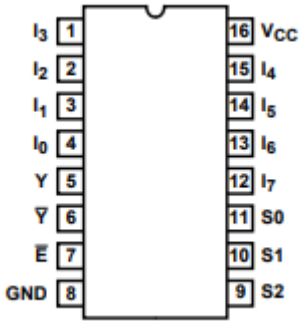

Figure 5.49: CD54HC151 Pin Configuration

5.63 Subcircuit Schematic Diagram

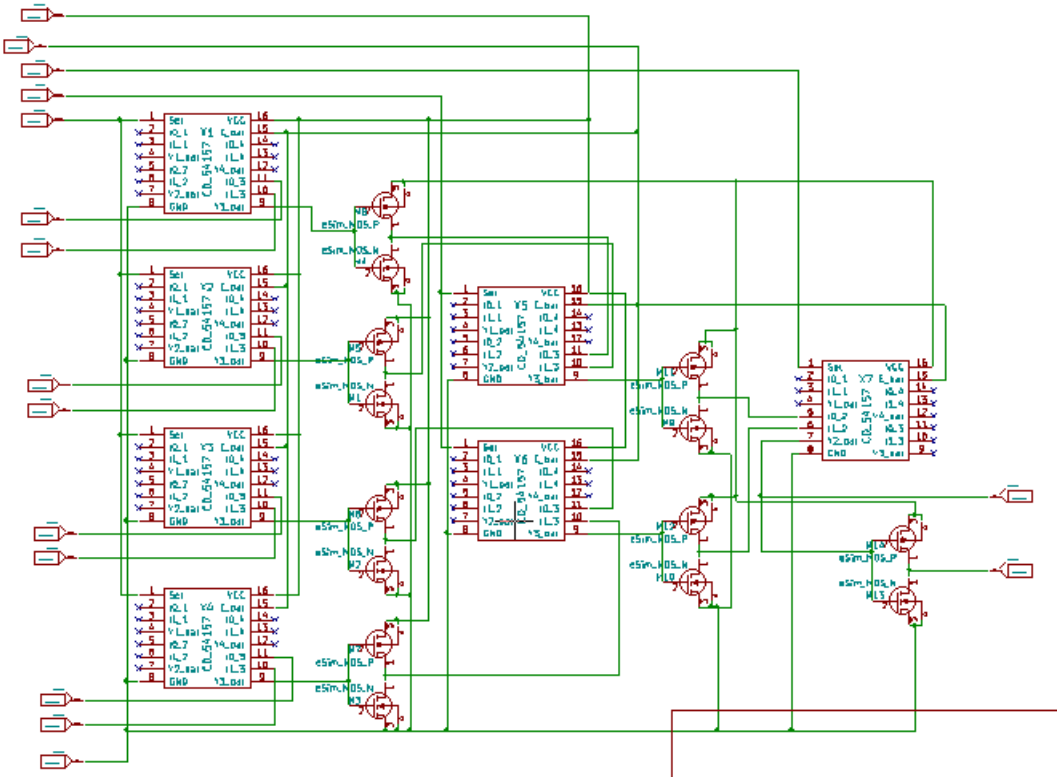

Figure 5.50: CD54HC151 Subcircuit Schematic Diagram

5.64 Schematic with external circuit

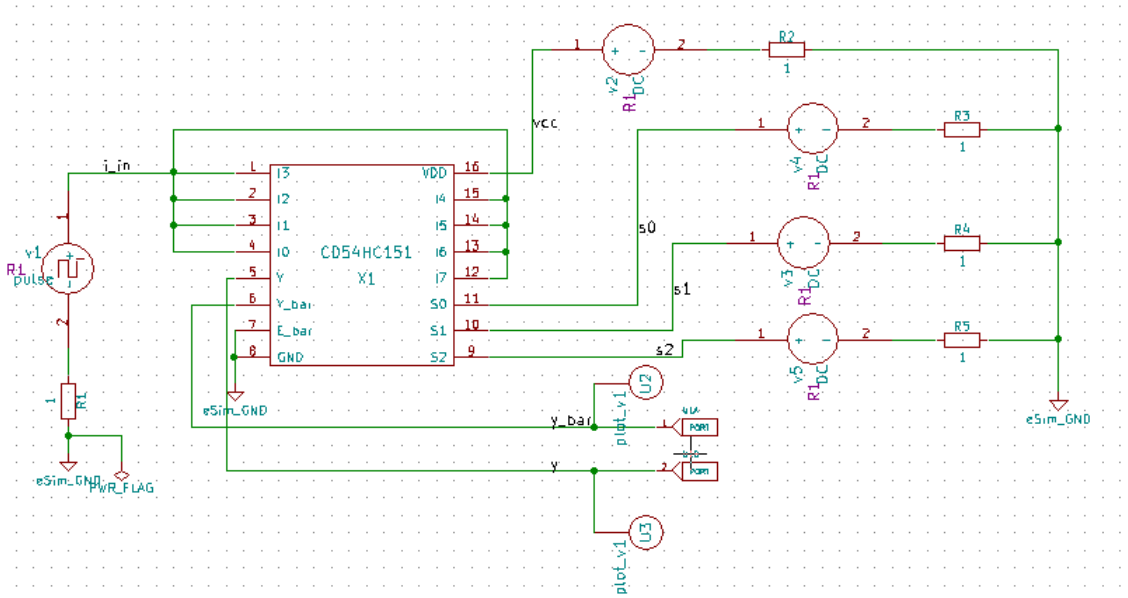

Figure 5.51: Schematic with external circuit

5.65 Ngspice Plots

5.65.1 Input Output plot

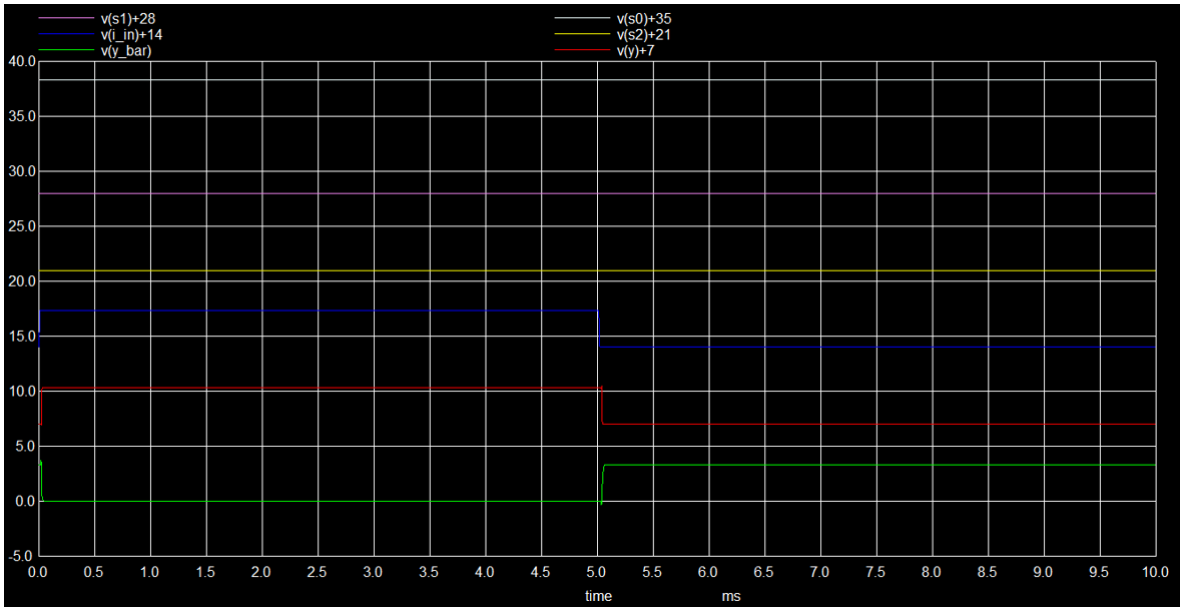

Figure 5.52: Input and Output

5.66 CD4008 IC

It is 4 bit full adder with parallel carry out IC. CD4008 IC [27] is designed with 180nm CMOS technology in eSim. It is 16 pin IC.

5.67 Pin Configuration

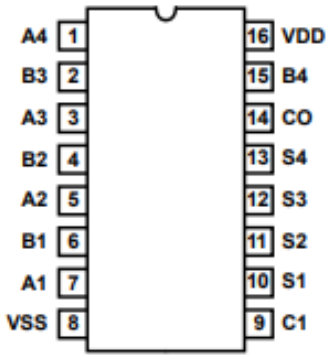

Figure 5.53: CD4008 Pin Configuration

5.68 Subcircuit Schematic Diagram

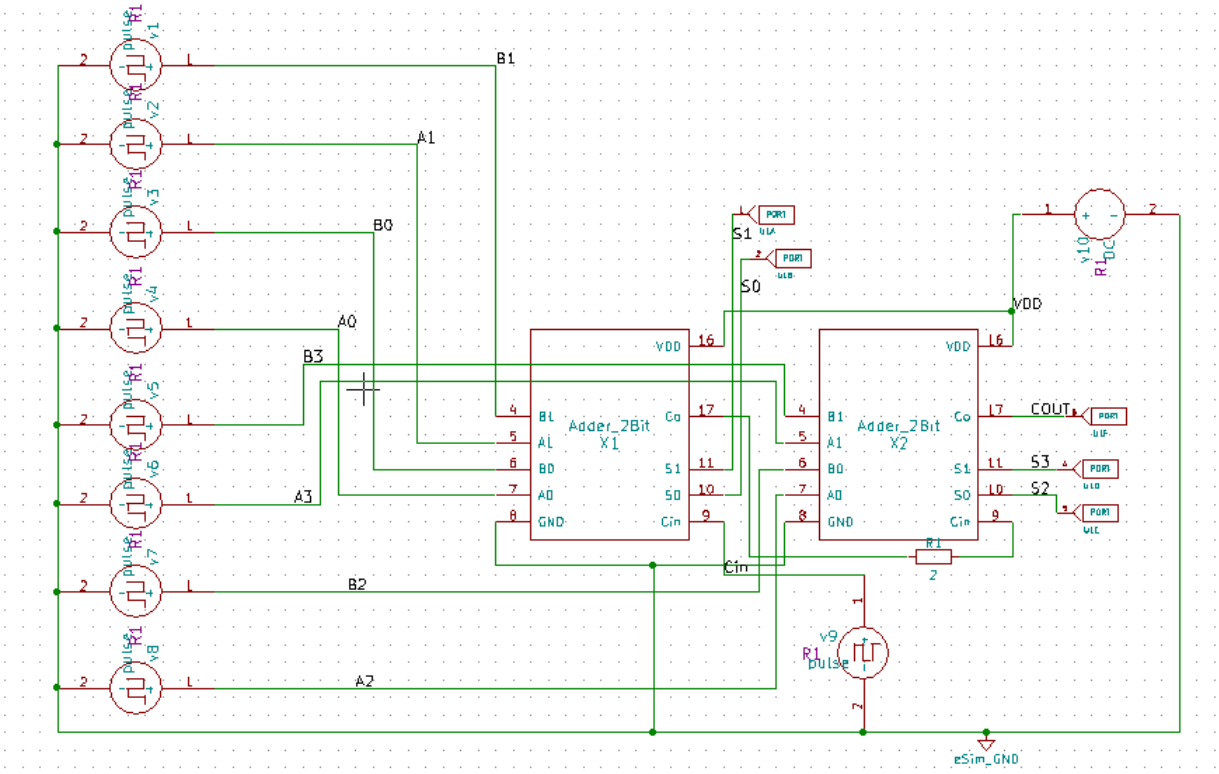

Figure 5.54: CD4008 Subcircuit Schematic Diagram

5.69 Schematic with external circuit

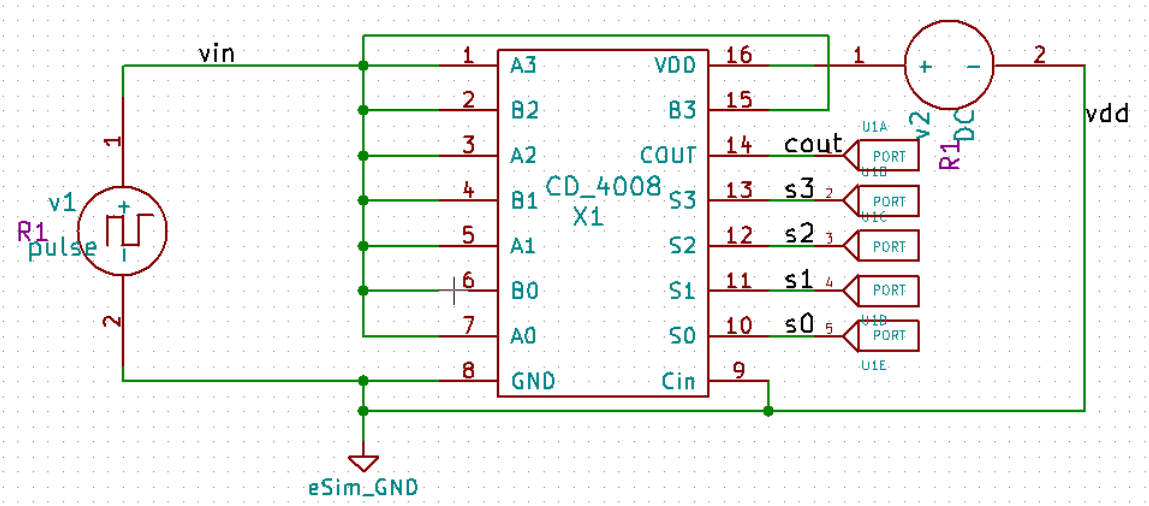

Figure 5.55: Schematic with external circuit

5.70 Ngspice Plots

5.70.1 Input Output plot

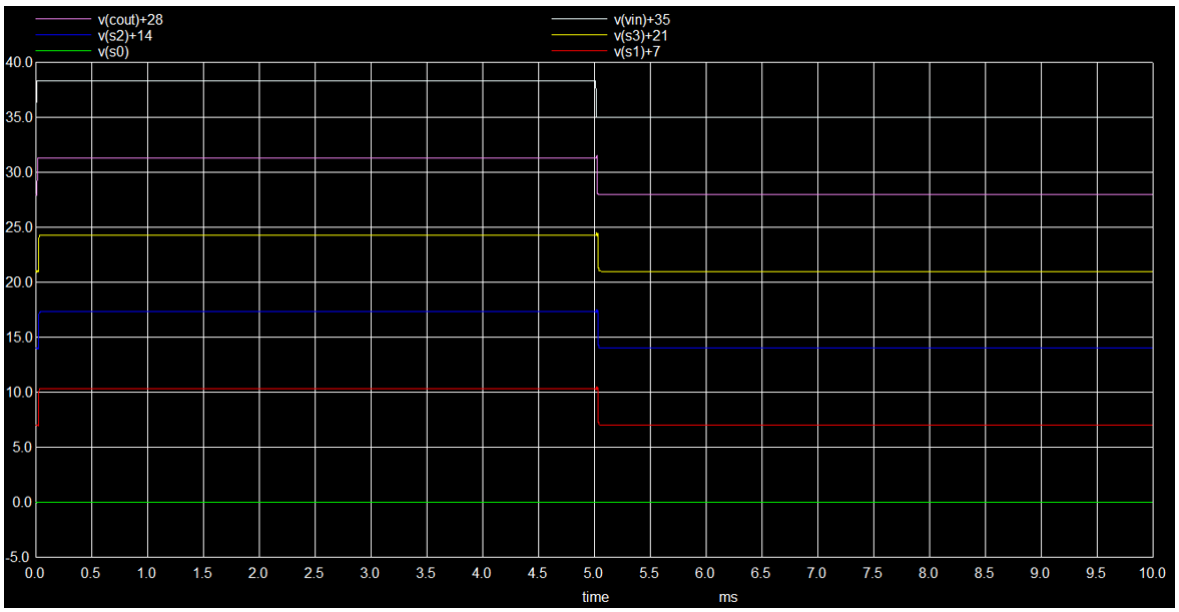

Figure 5.56: Input and Output

5.71 CD4028B IC

It is BCD to Decimal converter IC. CD4028 IC [28] is designed with 180nm CMOS technology in eSim. It is 16 pin IC.

5.72 Pin Configuration

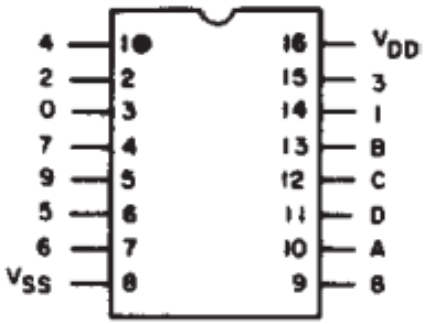

Figure 5.57: CD4028B Pin Configuration

5.73 Subcircuit Schematic Diagram

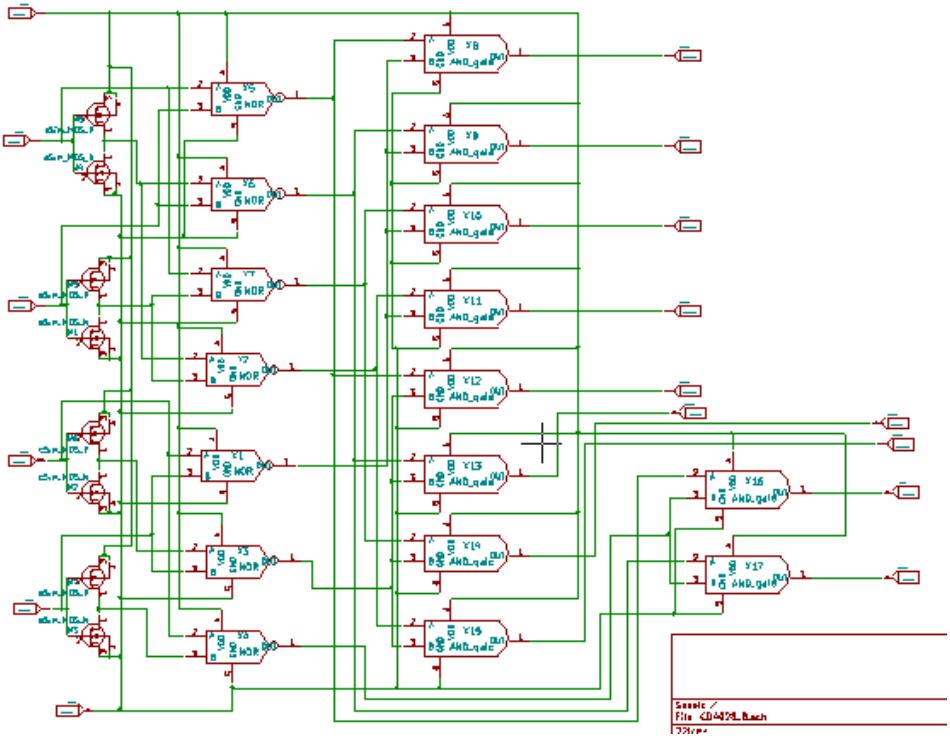

Figure 5.58: CD4028B Subcircuit Schematic Diagram

5.74 Schematic with external circuit

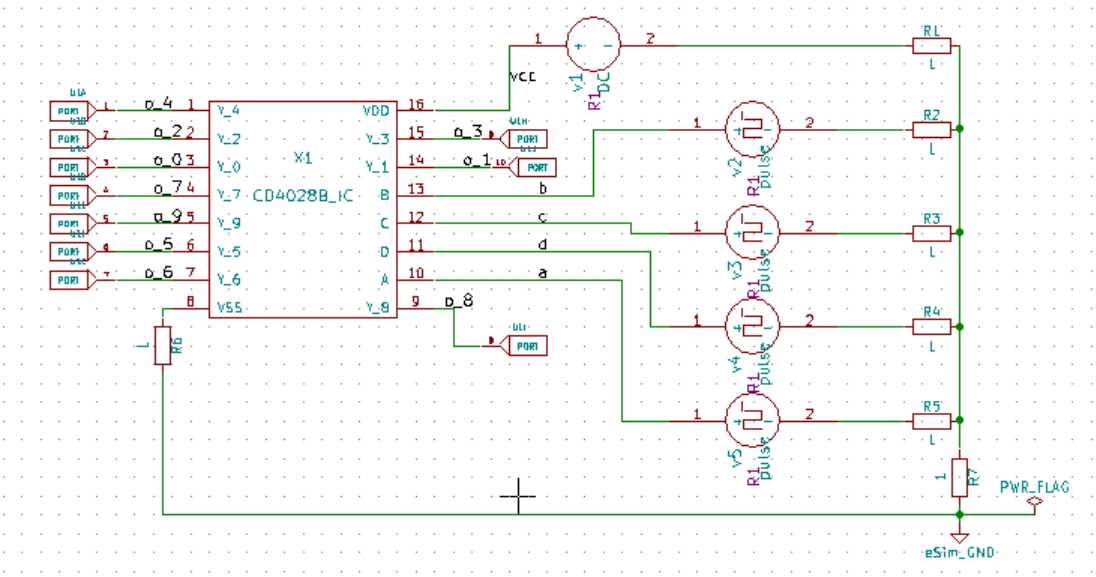

Figure 5.59: Schematic with external circuit

5.75 Ngspice Plots

5.75.1 Input Output plot

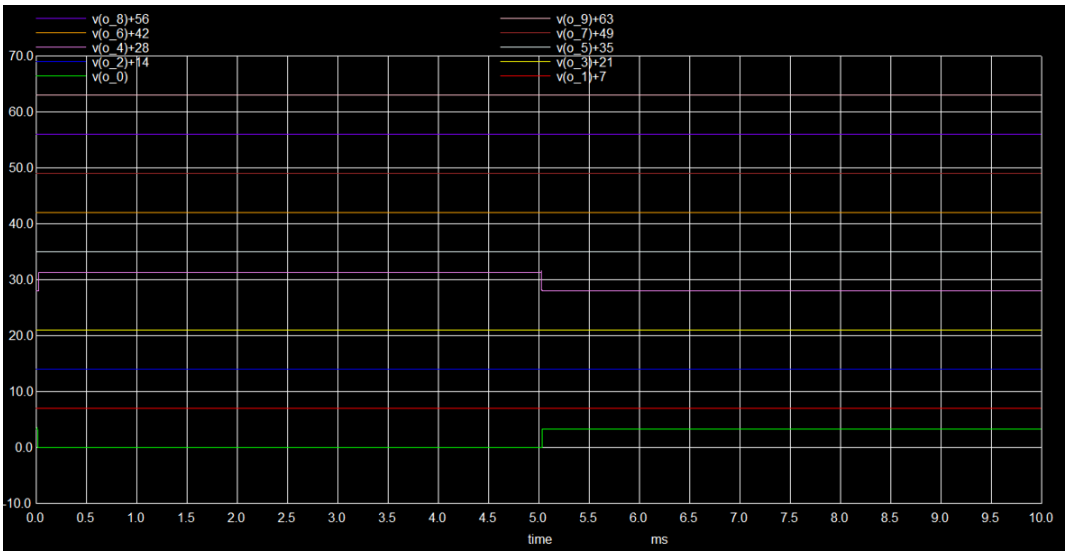

Figure 5.60: Input and Output

Chapter 6

Conclusion and Future Scope

We were successful to achieve the target of developing various subcircuits for both Analog and Digital Integrated Circuits. Each Integrated Circuit Model was developed strictly according to the information contained in their official data-sheets. The output of each IC was verified and tested successfully with the help of their test circuits.
All of these IC Models, developed under this Fellowship are very basic circuit units, such as Op-Amps, Voltage Regulators, Precision Rectifier, Schmitt Trigger, Differential Amplifier, Instrumentation Amplifier, Comparator, Multiplexer, DeMultiplexer and various Logic gate ICs. Each of these ICs is ready to be integrated in the subcircuit library of eSim. Developers & Students can use these ICs in their projects and circuit models as units.
With the development and expansion of the device model library in eSim, We expect more such ready to use IC models be developed to be used in eSim.

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