Summer Fellowship Report

On

Cloud Based SoC generator using eSim

Submitted by

Mihir Rana, Narra Hemanth and Ayush Kashyap

Under the guidance of

Prof.Kannan M. Moudgalya
Chemical Engineering Department
IIT Bombay

October 22, 2022

Acknowledgment

It is a pleasure to acknowledge the help and support that has gone in making this successful project. We express sincere gratitude to Kunal Ghosh (VLSI system design) and FOSSEE Team at IIT Bombay for providing me with this opportunity to work on this project and having faith in my abilities. We would also like to thank the eSim team for giving me such a great opportunity of learning and also for enabling me for their help in offering me the resources and guiding me throughout the project. A special thanks to all my mentors, Sumanto Kar, Rahul Paknikar, and Nagesh Karmali for helping me throughout the internship, sharing a lot of valuable and constructive suggestions during the internship. Finally, We wish to thank our parents for consistently encouraging us and keeping us positive at all times.

Contents

Chapter 1

Introduction

1.1 eSim

eSim is a free/libre and open source EDA tool for circuit design, simulation, analysis and PCB design developed by FOSSEE, IIT Bombay. It is an integrated tool built using free/libre and open source software such as KiCad, Ngspice, NGHDL and GHDL.

1.2 Ngspice

ngspice is the open source spice simulator for electric and electronic circuits. Such a circuit may comprise JFETs, bipolar and MOS transistors, passive elements like R, L, or C, diodes, transmission lines and other devices, all interconnected in a netlist. Digital circuits are simulated as well, event driven and fast, from single gates to complex circuits. And you may enter the combination of both analog and digital as a mixed-signal circuit. ngspice offers a wealth of device models for active, passive, analog, and digital elements. Model parameters are provided by our collections, by the semiconductor device manufacturers, or from semiconductor foundries. The user adds her circuits as a netlist, and the output is one or more graphs of currents, voltages and other electrical quantities or is saved in a data file.

1.3 Makerchip

Makerchip provides free and instant access to the latest tools directly from your browser and from your desktop. This includes open-source tools and proprietary ones. You can code, compile, simulate, and debug Verilog designs, all from your browser. Your code, block diagrams, waveforms, and novel visualization capabilities are tightly integrated for a seamless design experience. While Makerchip introduces ground-breaking capabilities for advanced Verilog design, it also makes circuit design easy and fun!

Chapter 2

Features of eSim

- Draw circuits using KiCad, create a netlist and simulate using Ngspice.
- Design PCB layouts and generate Gerber files using KiCad.
- Add/Edit device models(Spice Models) and subcircuits using the Model Builder and Subcircuit Builder tools.
- Perform Mixed-Signal Simulation.
- Support for Ubuntu and Windows OS.
- Interface with OpenModelica modelling software.

Chapter 3

Problem Statement

The task was to Verify the Analog IP's and check the functionality of the circuit, study about the circuit. After verifying the functionality we have to convert IP into a sub-circuit which is later ported into esim and can be used as an esim component. To solve the confusion in the IP nomenclature, we have created a standard nomenclature for shortened names.

3.1 IP Nomenclature table

Original name	Shortened name
cmos	cm
full	f
adder	add
nmos	nm
pmos	pm
amplifier	amp
bit	b
schmitt	smt
low	l
high	h
speed	spd
power	p
tester	tstr
oscillator	osci
buck boost	bb
converter	convtr
full wave	fw
bridge	bg
low voltage	low power
rail to rail	rr
pseudo	pdo
parity generator	pg
trigger	trigger

Table 3.1: IP Nomenclature table

Original name	Shortened name
stage	st
carry look ahead	cla
dynamic	dym
charge sharing	cs
comparator	comp
sramcell	srcell
barrel shifter	barsft
stage	stg or st
cross	x
decoder	dec
Approximate	aprx
Compressor	cmprsr
Sziklai Pair	sp
Analog	a
Digital	d
Multiplier	mult
resistor	r
phase locked loop	pll
detector	det
frequency	freq
gilbert	gbrt
Current mode logic	cml
latch	latch
dickson	dickson
pump	pmp
charge	c
inverter	inv
wallace tree	wall tree
portable	portable
charger	cr
Bandgap voltage reference	bgvr
Frequency compensated	fc
starved	std
cascode	csde
Mirror	mirror
Folded Cascode	fcsde
Miller Compensated	mc

Table 3.2: IP Nomenclature table

Chapter 4

IPs done by Mihir Rana

4.1 Folded Cascode Amplifier

4.1.1 Circuit details

It is well known that the active cascade gain boosting technique can be used to increase the DC gain of an Op Amp without degrading its high frequency performance. Unfortunately the existence of pole zero doublet will unfavorably affect the settling performance of the gain boosted Op Amp and the effort of pushing up the doublet can raise stability problem. Also in correlated double sampling(CDS) and correlated level shifting(CLS) methods two clock cycles are needed to amplify so the speed may be reduced. The new structure proposed in this paper is based on the conventional folded cascade amplifier. Folded cascode amplifier is a single-pole operational amplifier with a large output swing and has a higher gain compared to the ordinary op amp. It is very suitable for deep negative feedback because of its small signal gain that can be very large. Comparing to the ordinary telescopic amplifiers, folded cascode operational amplifiers have a larger output swing. To increase the DC gain of the Op Amp a new method is presented that uses positive feedback concept. Opposite to conventional techniques this technique does not add extra nodes to the structure of the Op Amp or pole zero doublet to the transfer function of the Op Amp. The folded cascade configuration achieves output impedance comparable to that of a normal telescopic amplifier with lesser number of devices stacked between supplies and ground in the output stage.

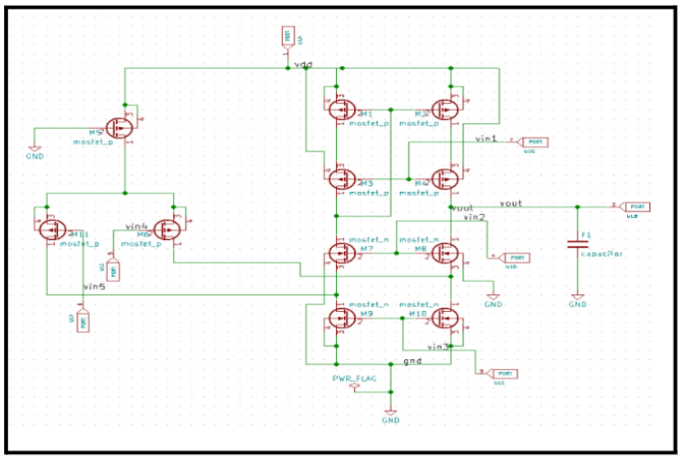

Figure 4.1: Circuit diagram

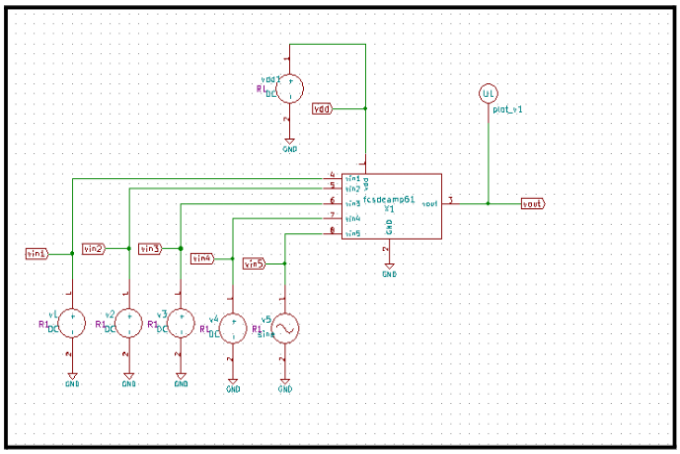

Figure 4.2: Sub-circuit

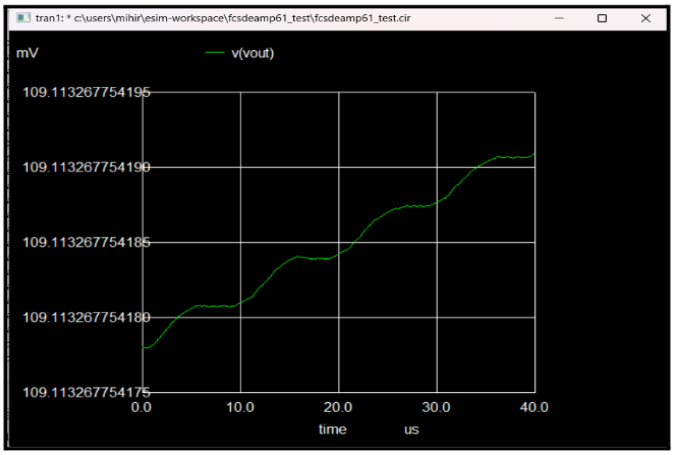

Figure 4.3: Output waveforms

4.2 Low Voltage Low Power Amplifier based on MOSFET Darlington Configuration

4.2.1 Circuit details

The Amplifier which we proposed to be taken is based on MOSFET Darlington pair configuration can be done by using both NMOS transistors or PMOS transistors. The Circuit is designed by using two NMOS or PMOS transistors, DC biasing voltage, Resistors, Capacitors, Input AC voltage source. Here, MOS transistors Q1, Q2 can be used as per requirement. And by considering the value of low dc voltage applied consumption of power is very important to be low while the output power is also low. By giving AC source voltage as Vin. The source voltage will have a phase value, we should give the input frequency and the Amplitude value of voltage taken. Resistors used are Input Resistor (R1), Source Resistor 1 (RS1), Source Resistor 2 (RS2), Drain Resistor (RD), LOAD Resistor (RL). Capacitors used are Input Capacitor CC1, Output Capacitor CC2, Source Capacitor CS. DC biasing voltage (VDD) is the supply dc voltage to the circuit. And the value of dc voltage is low so the output power will be low so by reducing the power consumption (PC) we can get the maximum output power. Now the two MOS transistors are connected through the wire with some resistors and capacitors are connected. And, the DC biasing voltage can be connected to the drain resistor and Q1 transistor through the wire. And then the dc analysis of the circuit can be done (applying dc voltage or current). By performing dc analysis, we come to know that what is the behavior of the circuit which we are taken. Here, in this circuit output is taken across the LOAD resistor (RL).

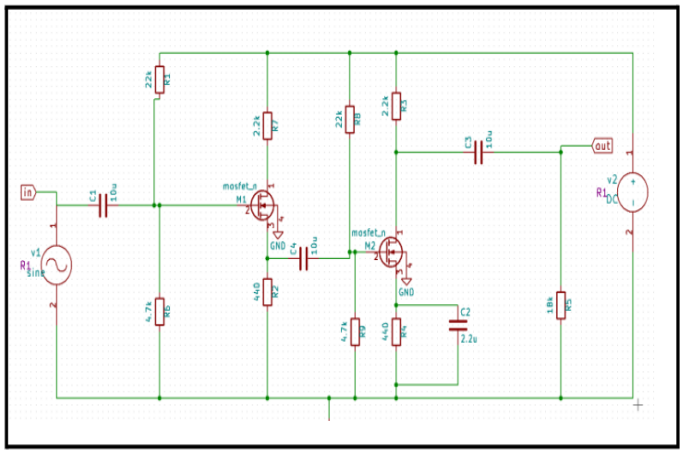

Figure 4.4: Circuit diagram

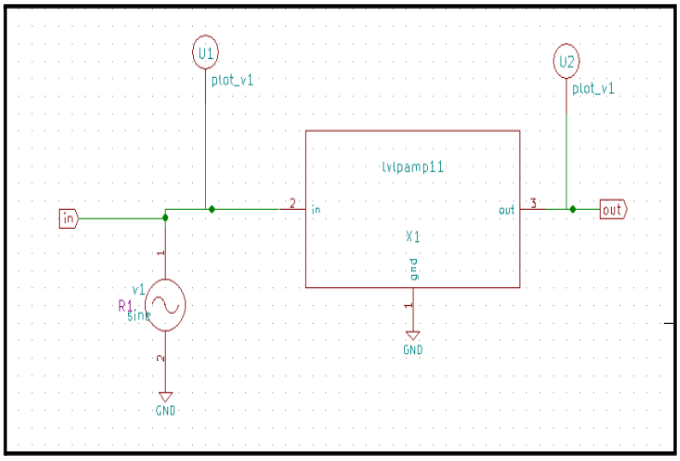

Figure 4.5: Sub-circuit

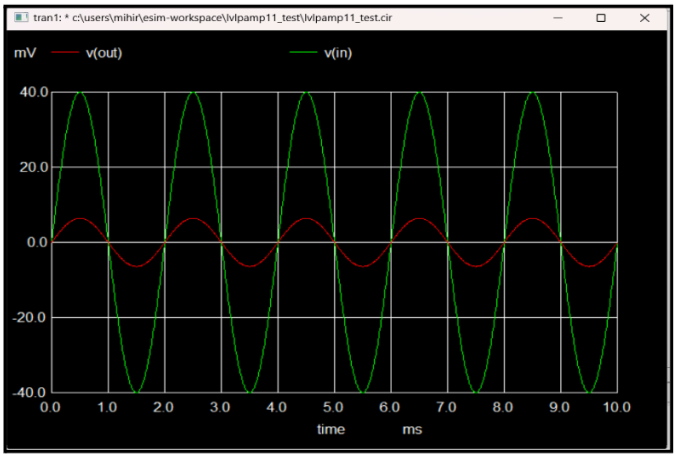

Figure 4.6: Output waveforms

4.3 Design of IC 741 tester circuit

4.3.1 Circuit details

1) Differential input stage: The importance of differential amplifier is to amplify the difference between two input signals. A slight difference in input signals leads to high gain at output. 2) Gain stage: Darlington transistor pair used to provide required gain 3) Output stage: Class AB complementary push-pull We can replace those two diodes with a transistor In this circuit Pin 3 (non-inverting) is kept constant and Pin 2(inverting) is getting changed due to the capacitor(C1).When the capacitor C1 starts charging Voltage at pin 3 is more than pin 2,so led starts blinking. Capacitor C1 is getting charged through R4 resistor. When the Capacitor gets full charged led becomes low. Again when Capacitor is getting charged and voltage at pin 2 is less than that ,then led starts blinking again. This on off will generates the square waveform at the output side. If Led doesn't blink at fixed intervals then we can't get the square waveform so that the IC which we are testing is decided as faulty. 1) Connect voltage supply of 9V to pin 7 and 0V to pin 4 2) Take Vcc=9 (volts) and Vee=0V 3) Connect both the pin4 and pin 7 to ground. Now the output voltage should be 0V 3) Now, connect the pin7 alone to Vcc(9V). The output should now be 9V 4) Now repeat the same with pin4 .the output should be 9V.

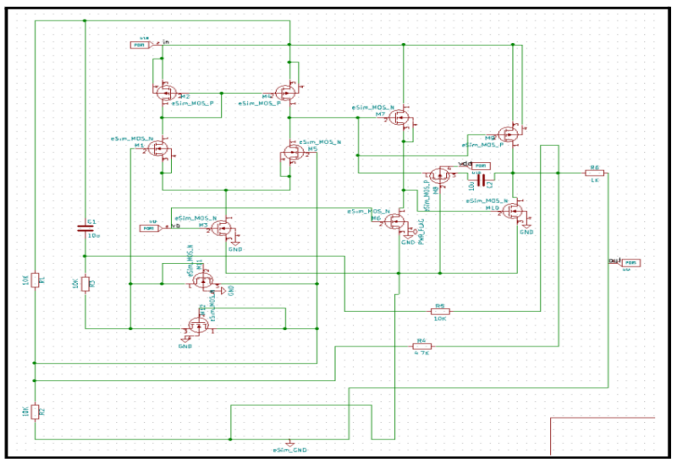

Figure 4.7: Circuit diagram

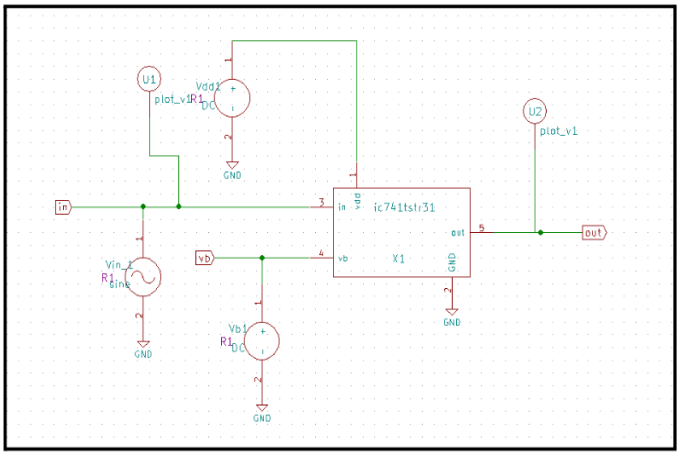

Figure 4.8: Sub-circuit

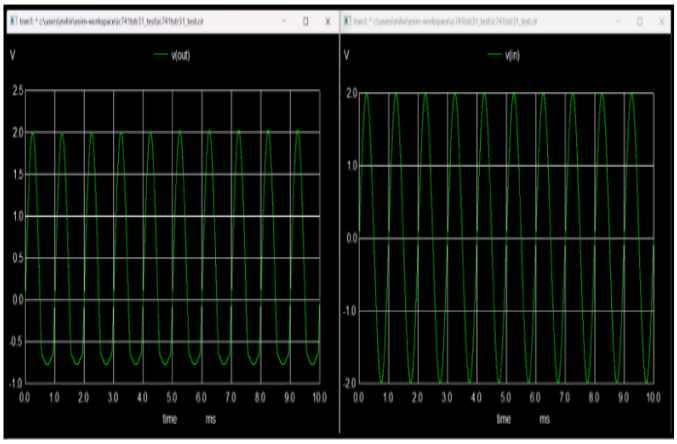

Figure 4.9: Output waveforms

4.4 Design of Half Adder using CMOS technology

4.4.1 Circuit details

Half adder is a combinational circuit that performs simple addition of two single bit binary numbers and produces a 2-bit number. The LSB of the result is the sum and the MSB is the Carry. In the basic approach the half adder is implemented using the primitive logic gates i.e., XOR and AND for sum and carry respectively. Here in the project Half adder is implemented using the principle of the static (CMOS) technology. This helps us in making the size of fabrication more small in terms of nanometre and hence making it compact yet efficient. The (CMOS) comprises of (NMOS) and (PMOS). There are two inputs and two outputs in a Half Adder. Inputs are named as A and B, and the outputs are named as Sum (S) and Carry (C). The appropriate sum and carry logic is realised and the circuit is represented using pull up and pull down transistors i.e. pmos and nmos transistors for the logic. The circuit for sum and carry are separately implemented in the same schematic. Required Inputs are inverted using pmos and nmos inverter design .Here in the circuit the inputs A and B are inverted using the inverter circuit , Ab and Bb are the other two inputs obtained using these respective logic are generated for sum and carry. Required ground and power supply is provided in the circuit. The circuit is annotated and the Netlist is generated using eSim. The python plot for sum and carry are obtained along with ngspice inputs A, B.

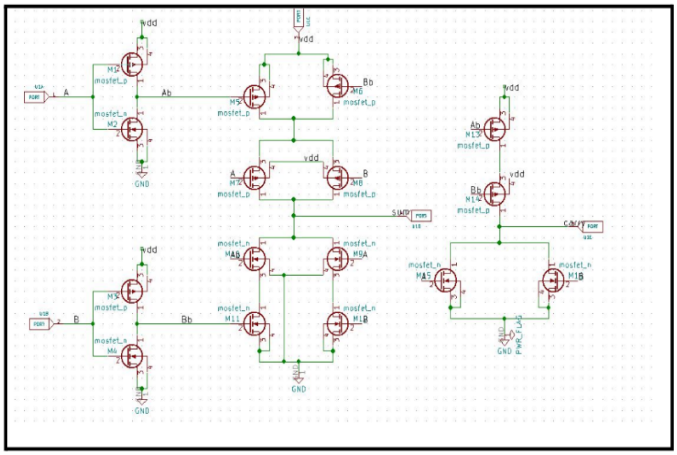

Figure 4.10: Circuit diagram

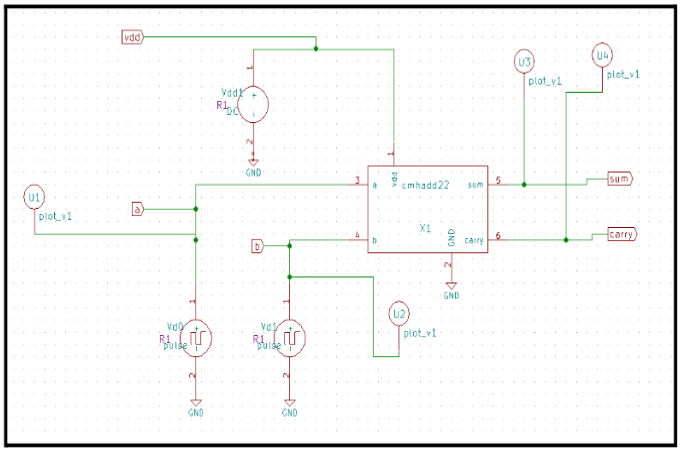

Figure 4.11: Sub-circuit

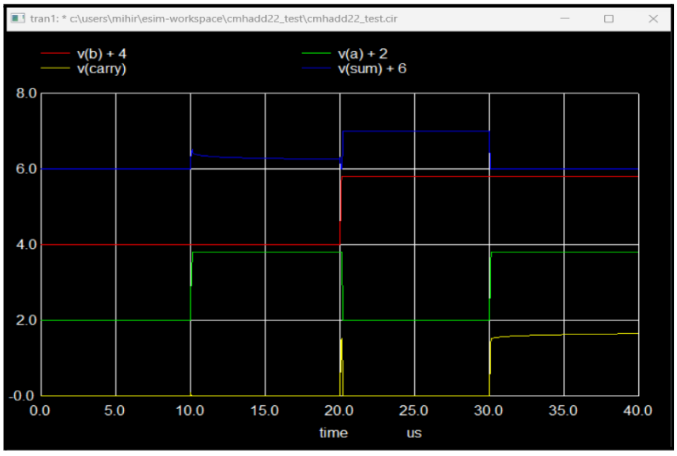

Figure 4.12: Output waveforms

4.5 Design of Approximate compressors

4.5.1 Circuit details

A compressor is a logic circuit that counts the number of ones in the input. Approximate compressor have j inputs and compute j/2 outputs by using novel approach aimed to minimize the error probability and the average error. The outputs of proposed approximate compressors do not have carry outputs this is different from standard compressors which consists of carry. In this design we implementing 5/3 compressor i.e 5 inputs and 3 outputs 6/3 compressor i.e 6 inputs and 3 outputs .These approximate compressors implemented using AND and OR gates For AND gate, whenever both inputs are high then output will be high otherwise output will be low and For OR gate, whenever both inputs are low then output will be low otherwise output will be high. We can also use higher order compressors i.e 7/4 8/4 9/510/5 11/6 12/6 13/7 14/7 15/8 16/8 17/9 18/9 19/10 20/10 etc. These higher order compressors are implemented using 2/1 3/2 4/2 5/3 6/3.. The output of the multiplier are divided into two parts MSB and LSB .The LSB bits are given to the approximate compressors and MSB bits are given to exact compressors.The output from both compressors are given to the adder circuit for multiplier output includes sum and carry outputs. Approximate compressors are used in the least-significant bits of the multiplier outputs. The approximate multiplier produces output which is approximately equal to the exact multiplier output.

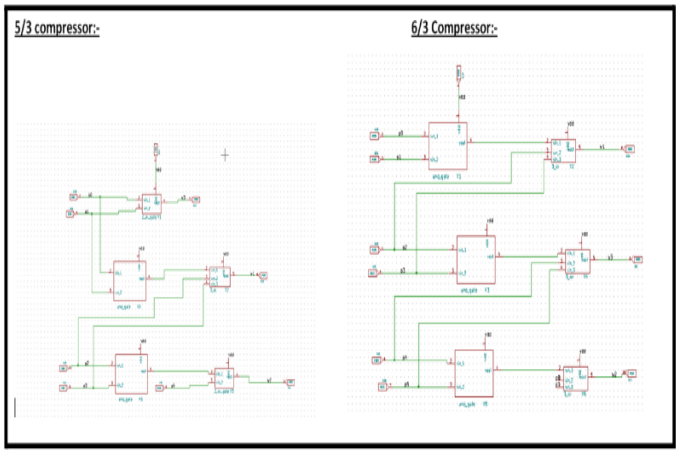

Figure 4.13: Circuit diagram

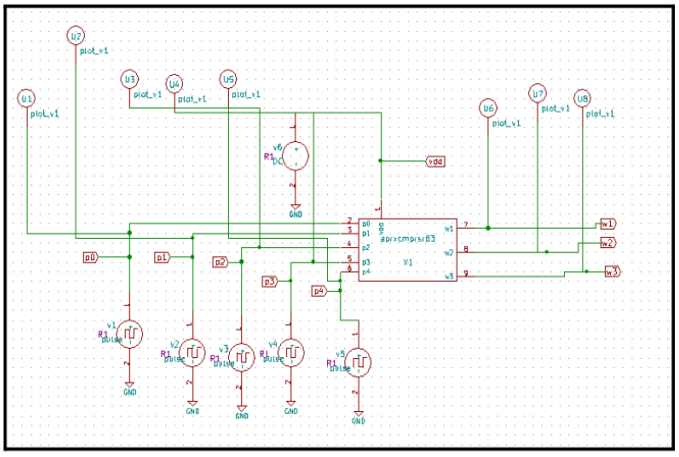

Figure 4.14: Sub-circuit

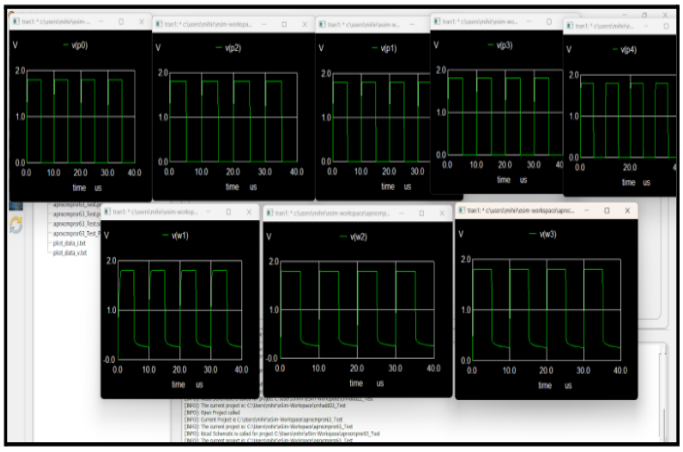

Figure 4.15: Output waveforms

4.6 Design and Analysis of Dickson Charge Pump using CMOS technology

4.6.1 Circuit details

The Dickson Charge Pump consists of the pumping capacitors which are arranged in a parallel fashion, which reduces the output impedance and increases the voltage gain as the number of stages increases. A diode-connected NMOS transistor is used for the construction of this CP. Here Vdd is the power supply voltage, NMOS transistor acts as switches, and V1 is the node voltage at the upper plate of the capacitor. Two clock sources Clk1 and Clk2 which have the same peak voltage, complementary phase, and are non-overlapping are applied to each stage in an alternative manner. When Clk1 is low, Clk2 will be high due to the complementary phase and subsequently, the switch MD1 is turned ON and the first capacitor is charged by the voltage source Vdd to the maximum voltage of Vdd - Vt at node V1. In the next half clock, MD1 turns OFF, and the voltage Vdd provided by the Clk1, gets added to the voltage Vdd - Vt which is already present, and as a result, the voltage at node V2 becomes 2Vdd - Vt. At the same period, the switch MD2 becomes ON and the next capacitor is charged through MD2 by the voltage 2Vdd-Vt, to a maximum voltage of 2Vdd - 2Vt. In this way, the charge gets pumped from one stage to another and the node voltages at pumping capacitors of higher stages increase continuously. The final capacitor doesn't add any voltage as it is grounded and it smoothens the output. The transient analysis performed to the circuit for a Vdd of 1.8V gave an output between 4.1-4.2V for 7.5us and saturated at 4.8V for a 130nm CMOS process, and the simulation was done using eSim and SKY130 PDK.

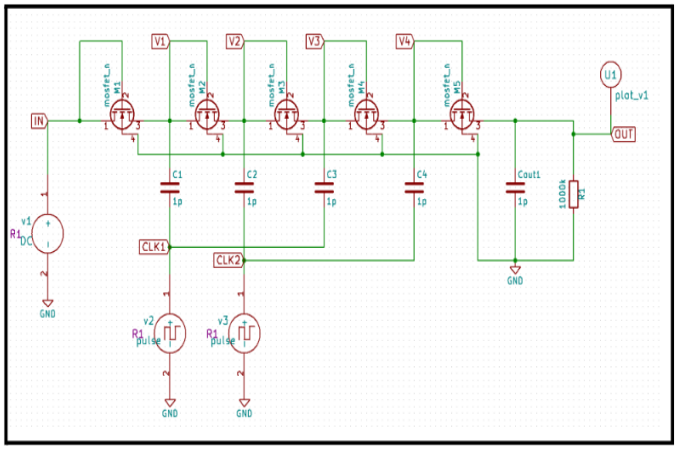

Figure 4.16: Circuit diagram

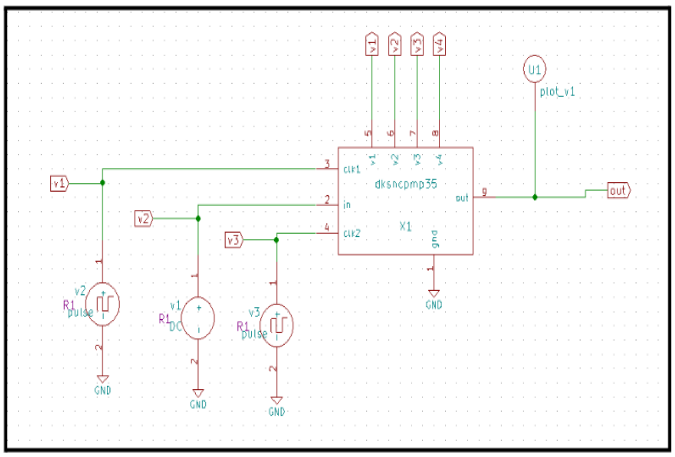

Figure 4.17: Sub-circuit

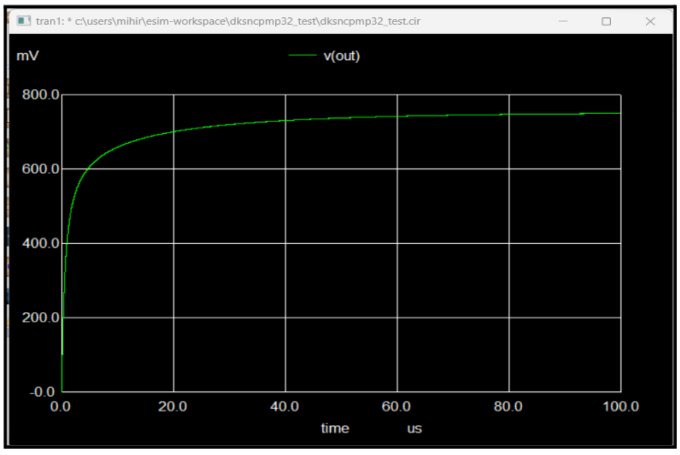

Figure 4.18: Output waveforms

4.7 Low Power CMOS Analog Multiplier using skywater 130nm pdk

4.7.1 Circuit details

The analog multiplier is used to multiply two continuous input signals, say v1 and v2 and produces output as v which is the linear product of two inputs. The output can be expressed as v=k v1 v2, where k is the gain. The circuit design proposed in this paper is used to eliminate extra voltage reference to provide a compact circuit design. By using CMOS technology with 130nm, the device density and performance can be improved. Low power consumption can be also achieved using the same technology. The circuit consists of a pair of common source amplifier with input transistors m9 and m10. The output is the squared function of input voltages v1 and v2. The circuit is built using 8 PMOSs and 2 NMOSs with two resistors. Transistors of m1 to m8 are of the type PMOS and transistors of m9 and m10 are of the type NMOS. The resistor value is taken as 2.5kOhm to make all the transistors present in the circuit to work in proper region. Transistors m1 to m8 acts as square root circuit in non-linear cancellation path. The output current from the input transistors m9 and m10 are directed into the square root circuit block which results in producing differential output voltage or current which is the multiplication of the input signals v12 and v34. v12 signal is the difference between v1 and v2 input signal, whereas v34 signal is the difference between v3 and v4 input signal. The resulting output signal v is the differential output of vout1 and vout2. The circuit can be able to operate with an input voltage of 1 to 1.2v and the measured power consumption is between 35uW to 98uW.

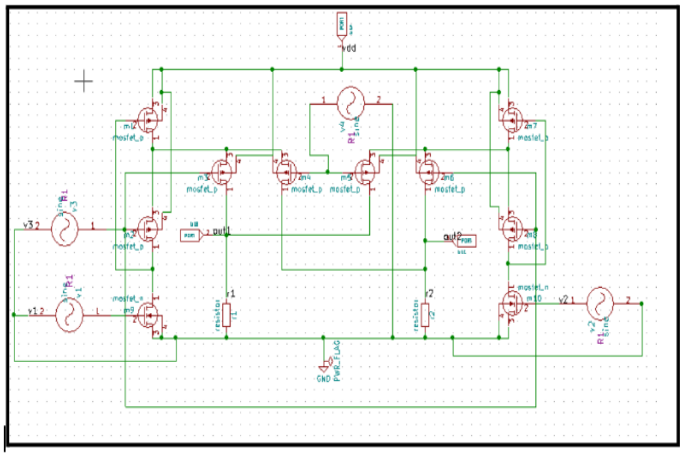

Figure 4.19: Circuit diagram

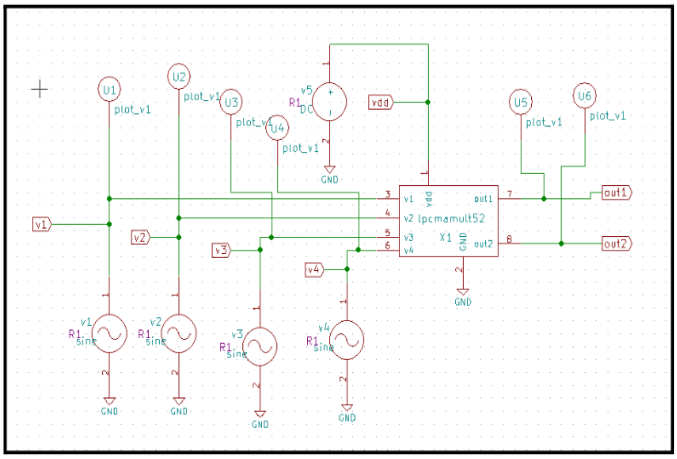

Figure 4.20: Sub-circuit

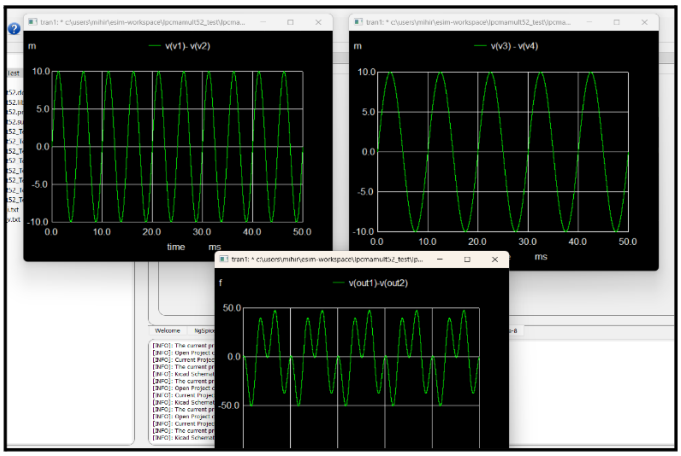

Figure 4.21: Output waveforms

4.8 Darlington amplifier

4.8.1 Circuit details

we proposed various modifications in small signal pair amplifier circuit and calculated some different results that may be useful for various applications. In comparison to bipolar conventional pair, we can also design a MOSFET configuration to reduce supply voltage (VDD) and dc consumption power. If we increases the collector current in pair amplifier, DC consumption power also increases and noise also increases, we can remove this disadvantage by designing a single input single output (SISO) amplifier based on MOSFET pair configuration. In this design NMOS and PMOS is used wherein here the the output of NMOS is given as the input for PMOS that is CMOS. Some resistances and capacitors are used with different values. One capacitor is used as load capacitor and another one input capacitor is also on this circuit. In electronics, amplifying signal by using pair is very important. The value of resistances used are 22kohm, 5kohm, two 100ohm, two 1kohm. Two capacitors are used in the proposed circuit one at the input terminal and one at the output terminal as a load. and the value of capacitors used are 22u and 1u. Recently Darlington cell and Darlington topology have been reported high gain and good bandwidth for modern application. In transient response time is varying with voltage and current. Other parameters and DC biasing supply that are used to design respective circuits. The performance of pair amplifier is very poor at high frequency and then the output will be verified.

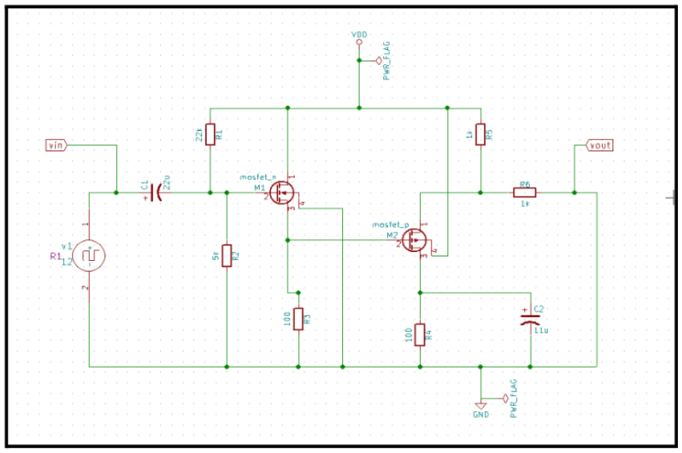

Figure 4.22: Circuit diagram

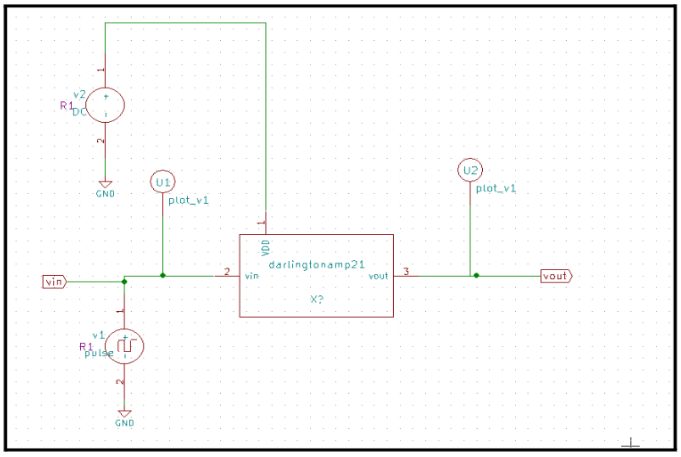

Figure 4.23: Sub-circuit

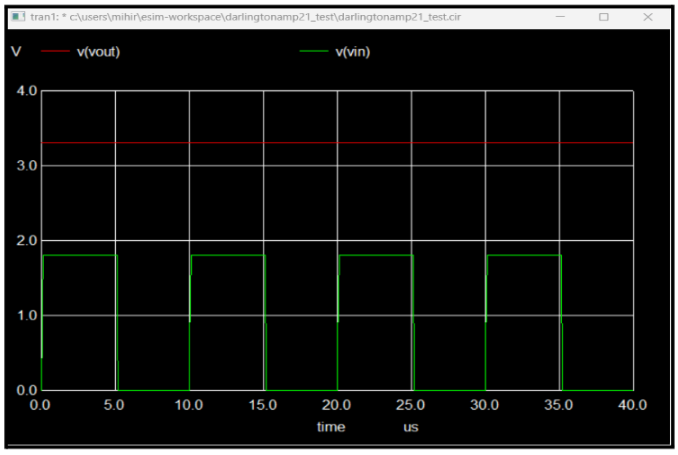

Figure 4.24: Output waveforms

4.9 2:4 Decoder using mixed logic CMOS gates

4.9.1 Circuit details

A 2:4 line decoder has two inputs, A and B where A is the MS bit and B is the LS bit. It has four minterm outputs, D0 = A'B', D1 = A'B, D2 = AB' and D3 = AB. It can be designed by using TGL or DVL gates as it takes 16 transistors which includes 12 AND/OR gates and 2 inverters. By using some proper signal arrangement, we can eliminate one of the two inverters A or B; Here D0 and D2 is implemented by using DVL logic, while D1 and D3 is be implemented by using TGL logic. For D0 and D2, A is the propagate signal, and for D1 and D3, B is the propagate signal; this eliminates the inverter B. Hence, the 14-transistor decoder consists of 9 NMOS and 5 PMOS for the low power decoder. The same low power 2:4 decoder can also be realised if we interchange the position of the TGL and DVL of the minterms in the above configuration. This is called inverting topology. Here also the elimination of inverter B is done. Thus, there is overall reduction of two transistors, logical effort, switching activity and also power dissipation in both the topologies. The topologies can be termed as 2:4 LP and 2:4 LPI, I for invert. In our circuit, the 2:4 LP decoder will be implemented and simulated. The necessary circuit diagrams are attached.

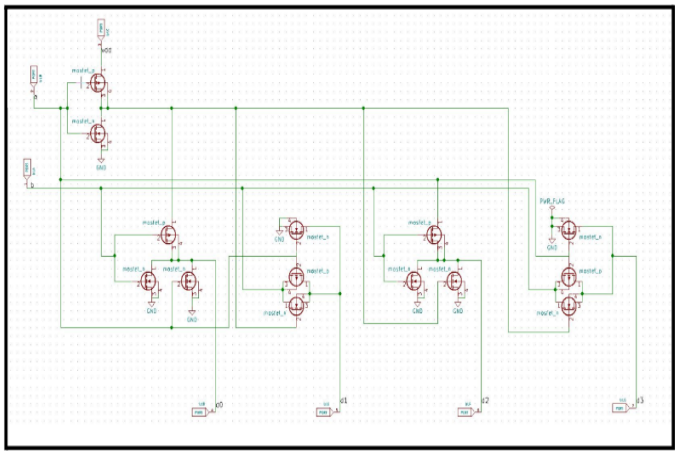

Figure 4.25: Circuit diagram

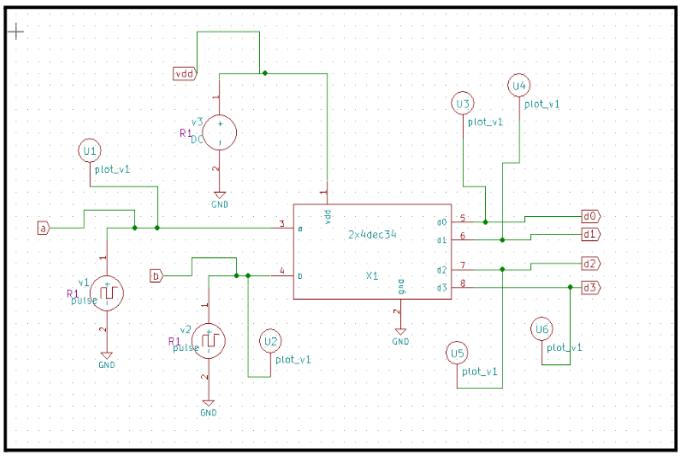

Figure 4.26: Sub-circuit

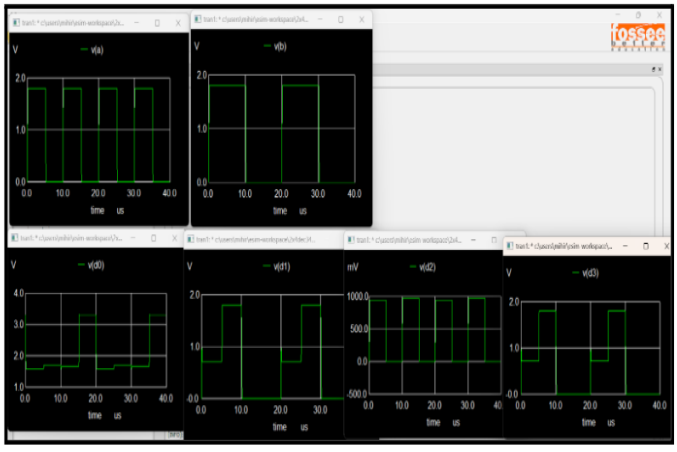

Figure 4.27: Output waveforms

4.10 Implementation of Full Adder using SkyWater 130nm PDK

4.10.1 Circuit details

Till today, different types of full adder cell are made and designed with different logic styles in digital world. In that some of them are good low power consumption, some of them for high speed and few for minimum area requirement but all these circuits have its own merits and demerits. According to the required application these full adders are used. Few of the full adder cells which are already implemented are convectional full adder, Static Energy Recovery Full Adder cell, Gate Diffusion Input full adder cell, etc. For most of the complex computational circuit requires full adder are used. Due to this, the whole power consumption and speed of computational circuit can be managed by the implementing the low power and high speed adder cell. So performance is totally depends on full adder. A full adder cell consists of three inputs and two outputs. Some of them are Expression for sum and carry out Sum = A'.b'.Cin +A'.B.Cin'+ A.B'.Cin'+ A.B.Cin = (A xor B) xor Cin Carry out (Cout) = A'.b.Cin +A.B'.Cin+ A.B.Cin' +A.B.Cin = A.B + B.Cin + Cin.A = (A xor B) Cin + (A xor B)' B This circuit is implemented with help of ten transistors. This circuit was implemented by using XOR gate. It uses two XOR module section and one inverter section. Each XOR module section is made by using 2 PMOS and 2 NMOS transistors. This is done which gives a better power and delay when compared to other circuits of full adder.

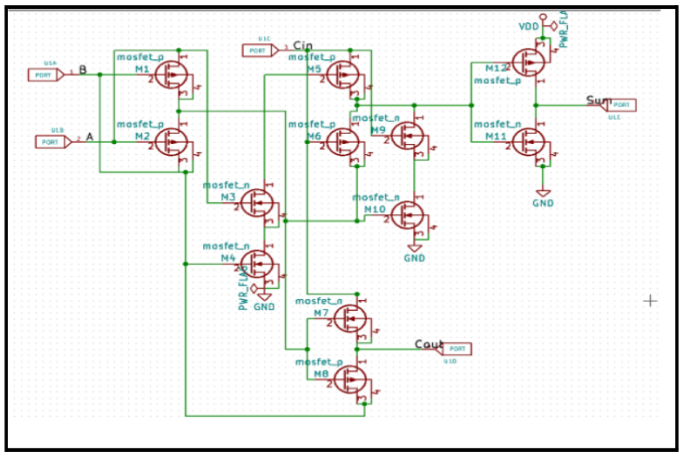

Figure 4.28: Circuit diagram

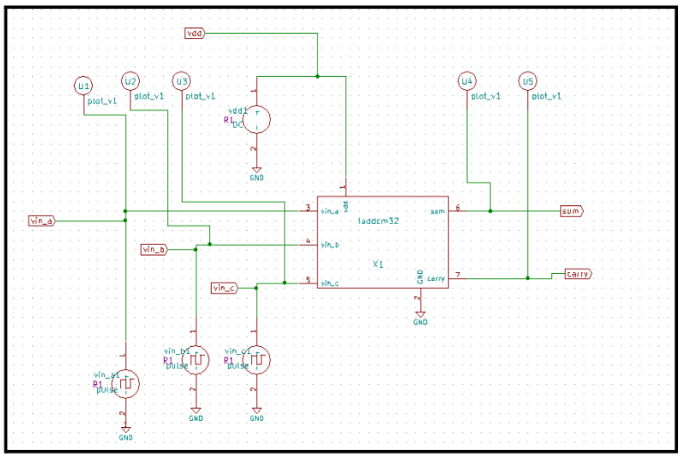

Figure 4.29: Sub-circuit

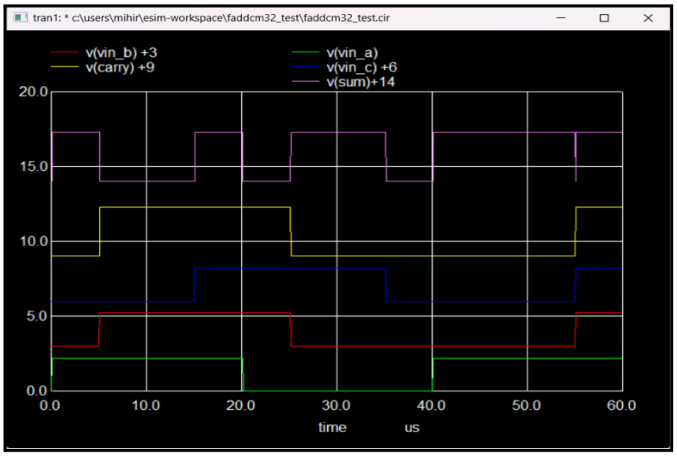

Figure 4.30: Output waveforms

4.11 The Two Stage CMOS Operational Amplifier with Frequency Compensation

4.11.1 Circuit details

Operational Amplifiers, Op Amps for short are play a very crucial role in the Linear Integrated Circuit Design. It can perform mathematical operations which make it "operational" amplifier, amplifier, comparators, PLLs, Integrators, Filters are few notable circuits that use Op Amp. They play a vital role in biomedical field for amplifying weak biomedical signals, which is important for gaining insights into the signal. The Operational Amplifier design is achieved through skywater 130nm technology. This circuit employs a NMOS differential amplifier M1 and M2 with two input terminals, with a PMOS load M3 and M4. This circuit is provided bias with the help of a current mirror circuit M5 and M6 provided with a constant current source. The output is taken as a single ended output and the gain of the differential amplifier thus obtained is further increased with the help of a Common Source Amplifier M7 which is also biased with the current mirror circuit of M5 and M8. The capacitors provide a stability against the poor phase margin of the circuit by trading off the fast response of the amplifier. Hence for better phase margin an external compensation is a must. The circuit employs different aspect ratio for different MOSFETs for the correct bias and operation of the circuit. The circuit provides a gain of nearly 40dB with a gain bandwidth product of 4.7MHz and about 3KHz 3dB cut off, which makes the operational amplifier circuit to amplifier a 1mV peak to peak to about 2V peak to peak thus weak signals can easily be amplified.

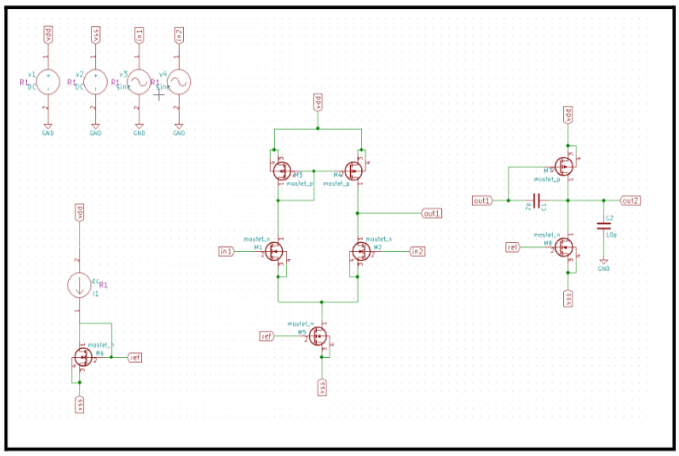

Figure 4.31: Circuit diagram

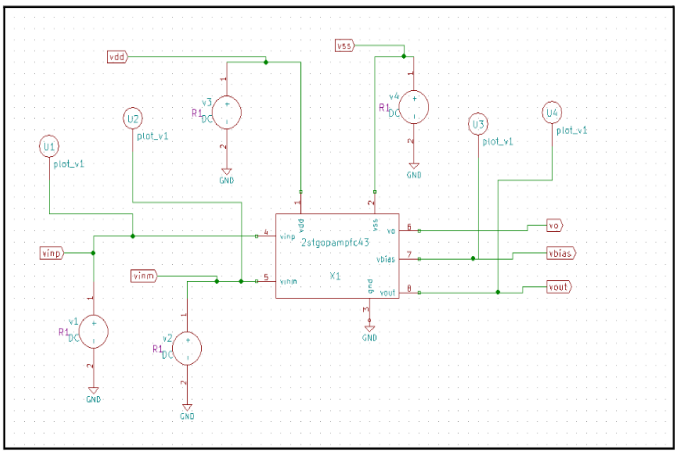

Figure 4.32: Sub-circuit

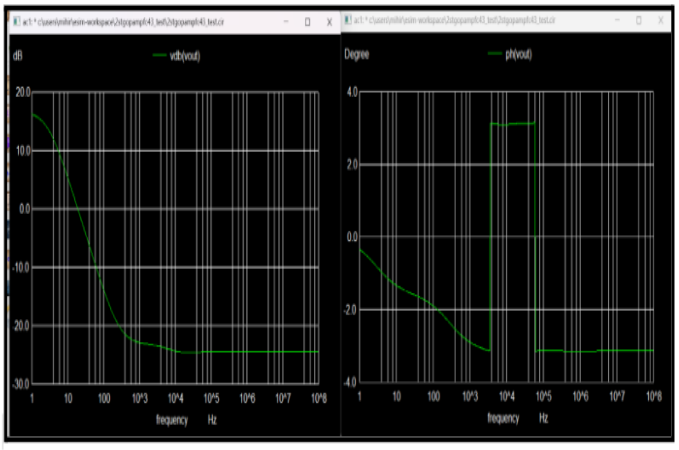

Figure 4.33: Output waveforms

4.12 Designing and Plotting the characteristics of a Cascode Current Mirror

4.12.1 Circuit details

The intent here is to design the cascode current mirror and study its various characteristics. Herein, this design uses the "cascoding" topology of the transistors. Cascoding can be simply defined as subsequent cascading of two stages,i.e., common source stage and common gate stage. Due to this cascode connection, the overall output impedance of the circuit increases which is also necessary to keep the output current constant.In the process of designing a simple current mirror, we generally ignore the "channel length modulation" effect, and this makes the circuit less accurate. In case of cascode current mirror, along with the simple current mirror circuit, two more MOSFETs are used to ensure the proper matching of the transistors, that means, equal drain-source voltage of the transistors.So, here, in this circuit a Cascode current mirror is implemented using four MOSFETs and its transfer characteristics, i.e., between output current and input current, and the output characteristics,i.e. between output current and supply voltage is plotted and studied. The sizing of the transistor can be done to achieve the desired and accurate results. Also, the region of operation of all the MOSFETs should be "Saturation" and in the results, it is expected that the cascode current mirror should be much more accurate than simple current mirror.

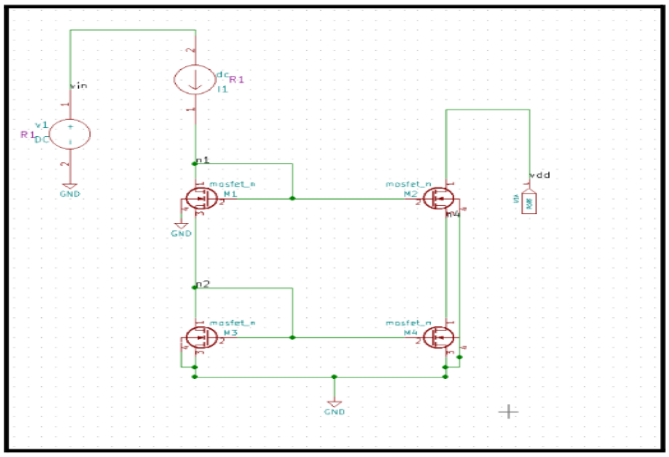

Figure 4.34: Circuit diagram

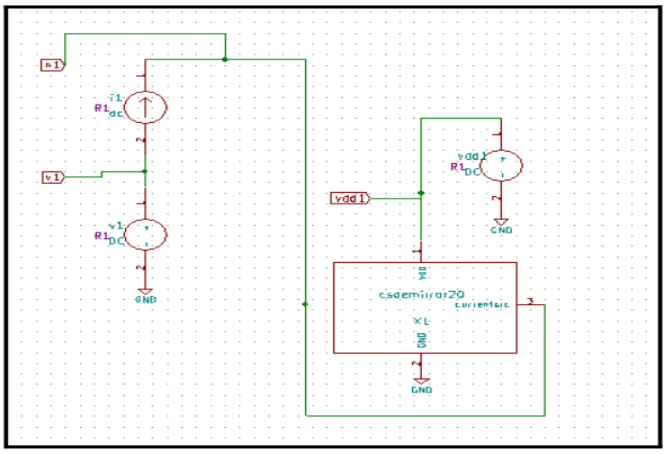

Figure 4.35: Sub-circuit

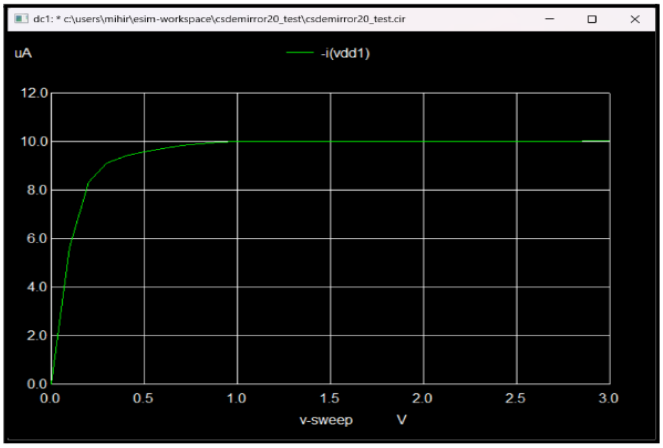

Figure 4.36: Output waveforms

4.13 Full wave Bridge rectifier using CMOS

4.13.1 Circuit details

The full wave rectifier circuit used with the combination of full wave rectifier to form a bridge is known as bridge is known a bridge rectifier. A CMOS based rectifier is designed using the MOS transistors which consist of filer and load. For the proper pulsating DC power output supply waveform. A MOS is introduced in the full wave bridge rectifier which act as diodes in the process of rectification. Four MOS are used PM1, PM2, NM1, and NM2 which regulated the power supply current to generate the required output DC supply wave form. When one of the terminal becomes negative, then the other becomes more positive than the other. This means the NM1 ,assuming the upper part, is turn OFF and PM1 is ON then current is flowing through the PM1 to NM2 to Load and getting pulsating DC output convert sustained output. Similar happens vice versa. Since CMOS has low static power consumption, high noise immunity and very low static power consumption is becomes much more efficient than their counterpart pn junctions diode. For each case the direction of the current is the same, so we have unidirectional current flow, which is DC voltage. The output of this circuit is the rectified signal and a full wave signal. The proposed rectifier circuit has been compared with its conventional rectifier circuit. It explains the efficiency of the proposed circuit which is much improved and increased than its conventional circuit.

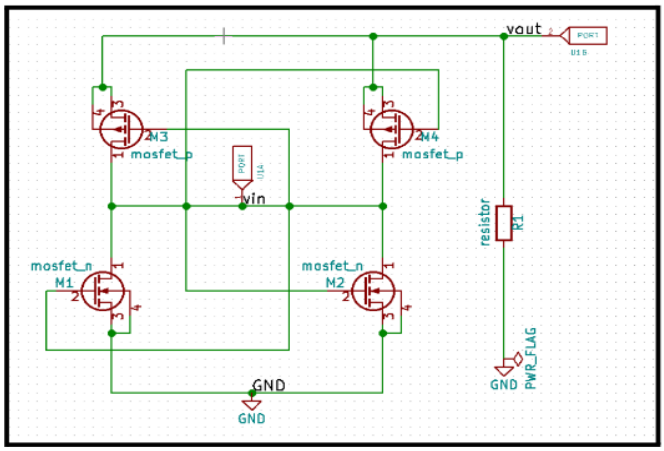

Figure 4.37: Circuit diagram

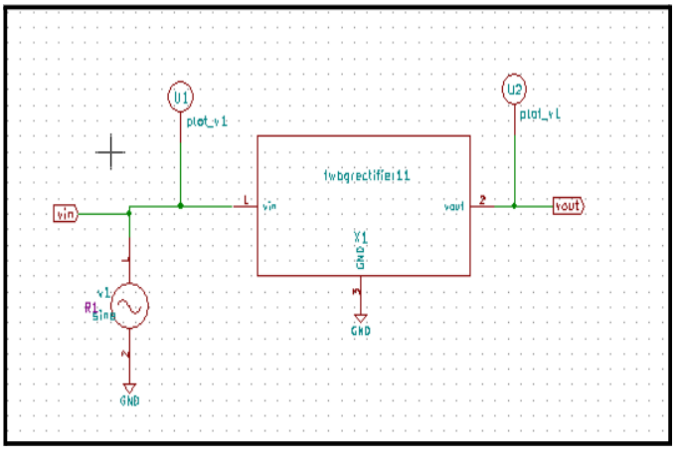

Figure 4.38: Sub-circuit

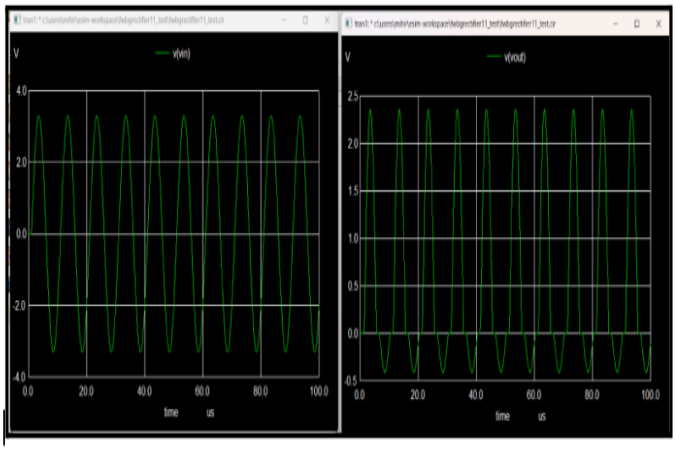

Figure 4.39: Output waveforms

4.14 CMOS Rail-to-Rail Operational Amplifier

4.14.1 Circuit details

Rail-to-rail op-amps allow signals to swing from negative supply rail to the positive supply rail. Nowadays, rail-torail operational anplifiers play a significant role in various biomedical applications. Earlier rail-to-rail op-amps were designed using BJTs, now CMOS technology is utilized. CMOS transistors have an edge over BJT in terms of very high input impedance, high speed, and low leakage current. The topology of the input stage is based on the folded cascade op-amp with a PMOS differential pair and NMOS cascode load. Due to the usage of PMOS transistors at the input terminals, the input voltage can come close to the negative rail. NMOS differential input pairs, unlike PMOS differential input pairs, operate near the positive supply rail. By combining the combination of both configurations, a parallel-connected PMOS and NMOS differential stage reaches operational mode at both rails. The rail-torail output stage reduces voltage drops at the output branch so that the output can reach the rails. The output stage is configured with a common-source NMOS and PMOS connected at the drain. The operating point is one of the most important factors to consider when designing the push-pull inverter output stage. The voltage input of this stage is the output voltage from the preceding stage. Two transistors in the push-pull inverter output stage are in the saturation region at this voltage. The current is largely dependent on the size of the transistors because there is no current bias network.

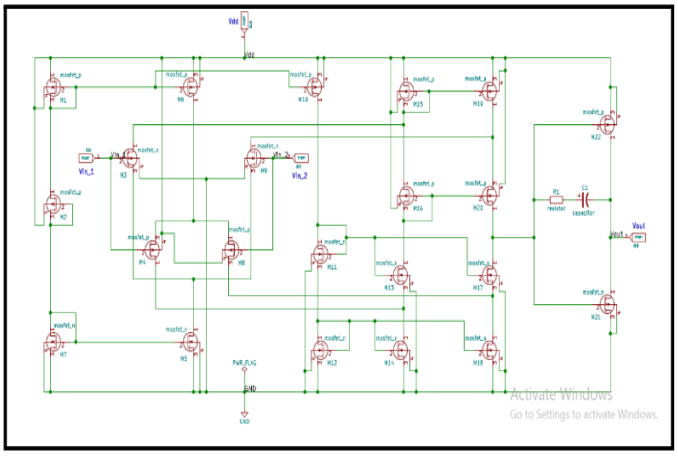

Figure 4.40: Circuit diagram

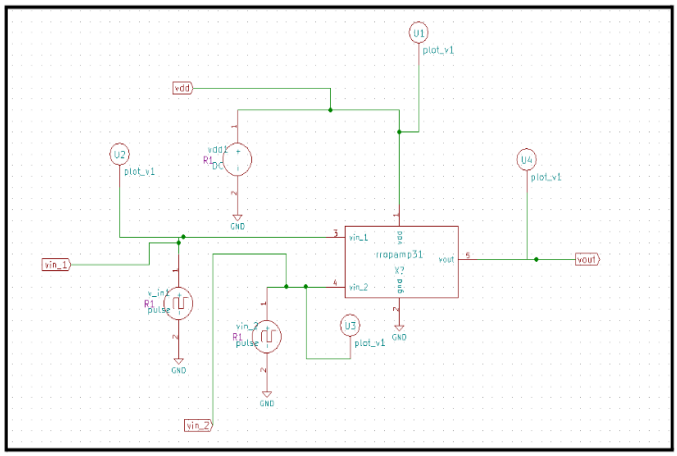

Figure 4.41: Sub-circuit

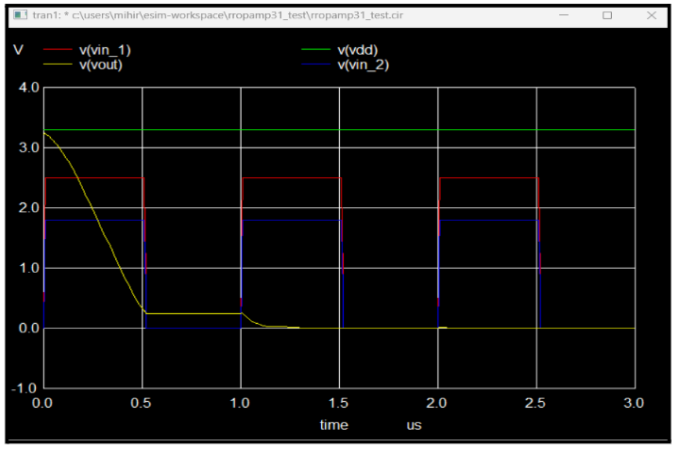

Figure 4.42: Output waveforms

4.15 RC Phase Shift Oscillator using FET

4.15.1 Circuit details

To create oscillation and sine wave output we need an active component, either Transistor or Op-amp in inverting configuration, and we need to feed back the output of those components to the input through the three pole RC network. It will produce a 360-degree phase shift at the output and produce a sine wave. To build the circuit we need the following things 1. Breadboard 2. 3 pcs of .1uF ceramic capacitors 3. 3 pcs of 680R resistor 4. 2.2k resistor 1 pc 5. 10k resistor 1 pc 6. 100R resistor 1 pc 7. 68k resistor 1 pc 8. 100uF capacitor 1 pc 9. BC549 Transistor 10. 9V power supply The output is provided as the input of the RC-networks which is again provided across the base of the transistor.If By cascading there RC network, we will get 180-degree phase shift. The RC networks are providing the necessary phase shift in the feedback path which is again altered by the transistor. The Phase shift oscillator can be made as variable phase shift oscillator which can produce a wide range of frequencies depending on the pre-set value determined. This can be done easily by changing only the fixed capacitors C1, C2, and C3 with a triple gang variable capacitor. Resistor value should be fixed and same in such cases.The initial starting point of the sinusoidal wave is 0 degree in phase and if we identify each positive and negative peak and 0 points, we will get 90, 180, 270, 360 degree phase. So, when a sinusoidal signal starts it's journey other than the 0-degree reference, we call it phase shifted differentiating from 0-degree reference.

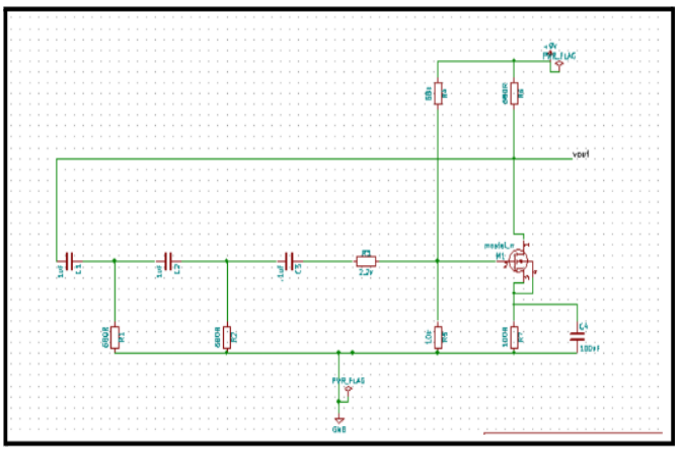

Figure 4.43: Circuit diagram

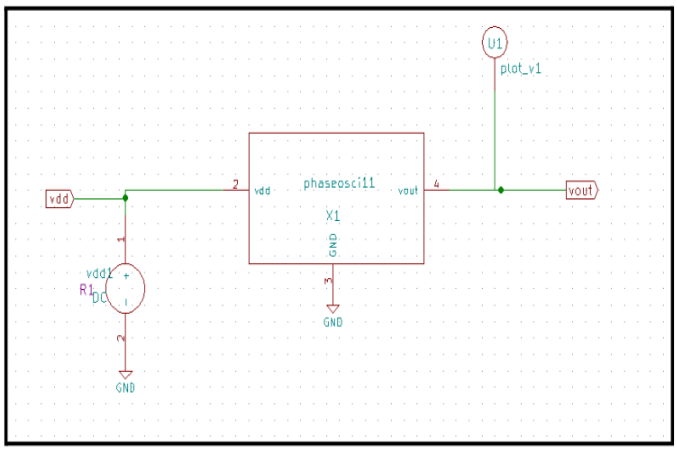

Figure 4.44: Sub-circuit

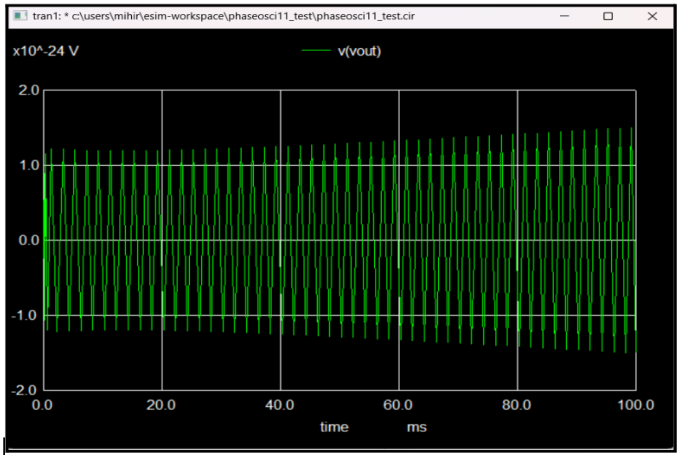

Figure 4.45: Output waveforms

4.16 Ring Oscillator Using Sky130

4.16.1 Circuit details

The design of conventional ring oscillator is made up of odd number of inverters connected in series that form a closed loop path. The stated design uses the similar concept in addition to power switching current starved inverters. The generation of high current is done by the symmetrical load, through which circuit becomes sensitive to very light variations in the input. The circuit is driven by proving the input Vin voltage set to 1 Volt pulse input, and reference voltage Vref is set to 1 Volt DC. MOS Transistor sizing is done with ratio of width to length as 240 nanometre to 130 nanometre respectively for nMOS and ratio of width to length as 600 nm to 130 nm respectively for pMOS in ideal conditions. The width of pMOS is double to overcome the drawbacks of pMOS and making pMOS work at almost the same speed as nMOS which in turn makes the resistance lower. If the input voltage is increased then the output of the circuit gets distorted. As the developed design circuit is used in applications which consume low power like biomedical appliances, chemical appliances, the lesser the provided voltage gives us the smoother output. With respect input, the output of the circuit is at the 0.06 percent of the input. For example, considering the input voltage as 1V, the oscillating output ranges between 0.7V to 1V. The output in real time simulation is not as same as the reference waveform, but is affected with high noise when there is transition from lower potential to higher potential.

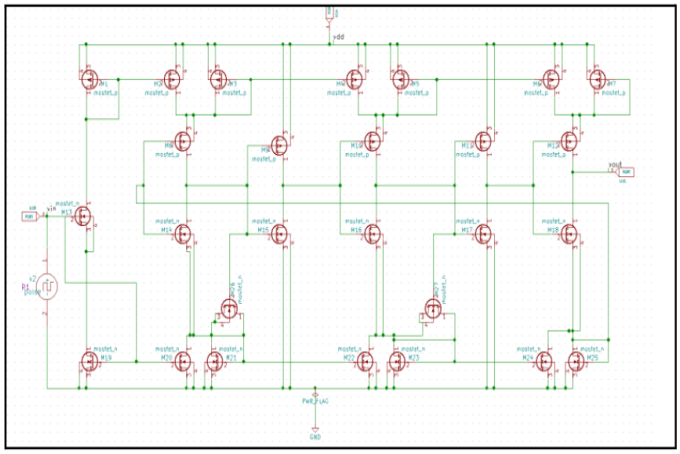

Figure 4.46: Circuit diagram

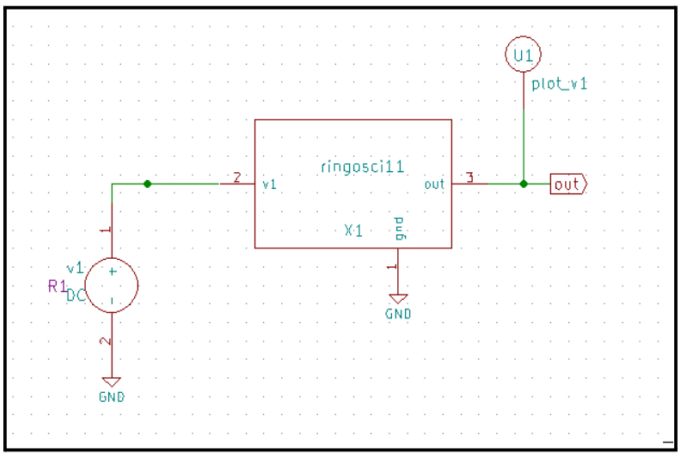

Figure 4.47: Sub-circuit

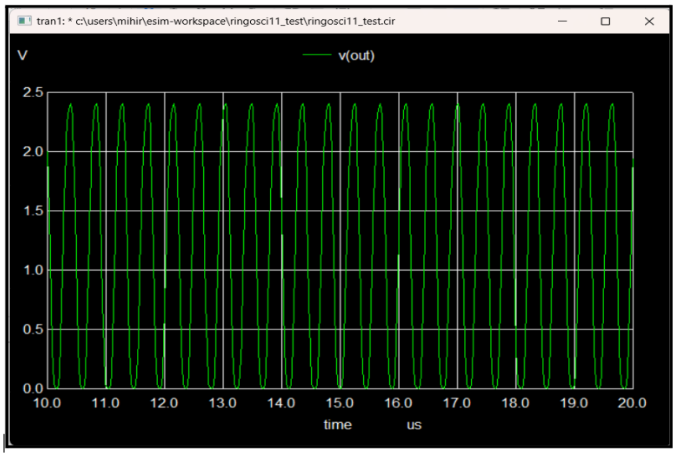

Figure 4.48: Output waveforms

4.17 Miller compensated two stage operational amplifier

4.17.1 Circuit details

The circuit will have open loop gain of greater than 70dB phase margin greater than or equal to 60 degrees load capacitance of 10 pico farad and a minimum total power consumption.The load is assumed capacitive. compensation capacitor Cc can be treated open at low frequency.There are varieties of applications that opamp is applied on due to its linear device characteristic. In order to produce a good product differential inputs are applied to the amplifier to obtain a higher gain. The input differential amplifier block is designed to provide high input impedance large CMRR and PSRR low noise high gain and low offset voltage. The second stage of the opamp performs level shifting which added gain as well as the conversion of differential to single ended The circuit has a current mirror at the top differential pair in the middle and a tail current mirror.It also has a bias circuit at the left which is used to stabalize the transistor transconductance of opamp. The bias circuit supplies bias current to the circuit. Biasing circuit is independent of power supply voltage variations.The tail current mirror acts as a current source to the opamp.The input is given to the differential pair.The first stage of opamp is a differential pair with current mirrors and the second stage is a common source amplifier.The gain does not seem to be affected much to first order. The miller capacitance Cf is connected in negative feedback fashion across one of the internal gain stages typically the second stage.

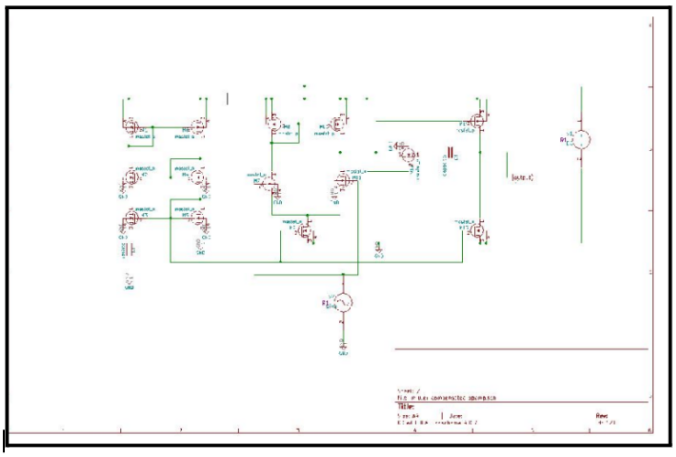

Figure 4.49: Circuit diagram

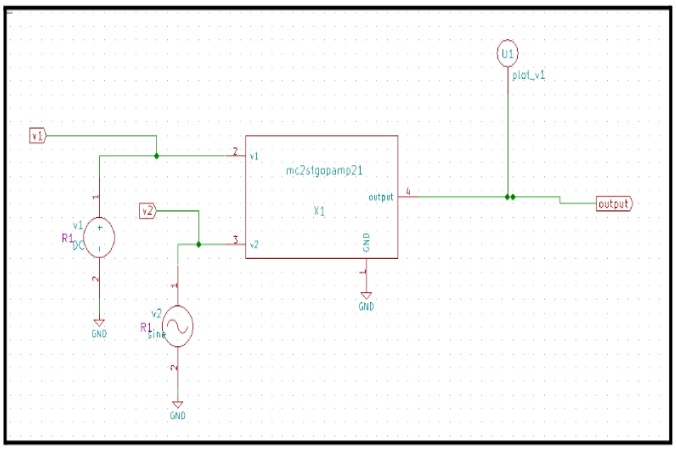

Figure 4.50: Sub-circuit

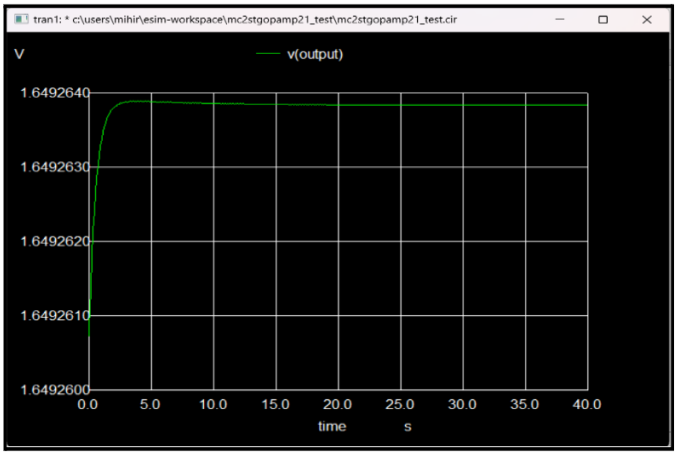

Figure 4.51: Output waveforms

4.18 Current mode logic CML latch

4.18.1 Circuit details

CML latch has the two sub parts: CML buffer and regenerative latch. The basic CML buffer is the simple differential amplifier with two resistor loads value R. Both transistor should be in saturation. The transistor which is closest to getting into triode is the one whose input is at VDD which can be treat as boundary condition. Hence, we must choose the logic swing Io into R to be less than threshold volatge of transistors. A regenerative latch in CML logic can be implemented by connecting the output to the input of CML buffer to get the positive feedback. For regeneration and latching, we need gm greater than 1/R. The input clocks of CML buffer and regenerative latch are complemented. To make sure all transistors are in saturation we must use appropriate common mode voltage. When clock is low, the second stage with positive feedback is disabled, and the circuit is a simple differential amplifier. This is the phase when the output tracks the input with some gain. When the clock goes high, the input amplifier stage is disabled, and the regenerative second stage is activated. The second stage then regenerates from where the amplification stage left the outputs and produces a logic output depending on the sign of the initial voltage. The designed circuit is only a latch. To make a flip flop that samples on every clock edge we need to use two latches in a master slave fashion.

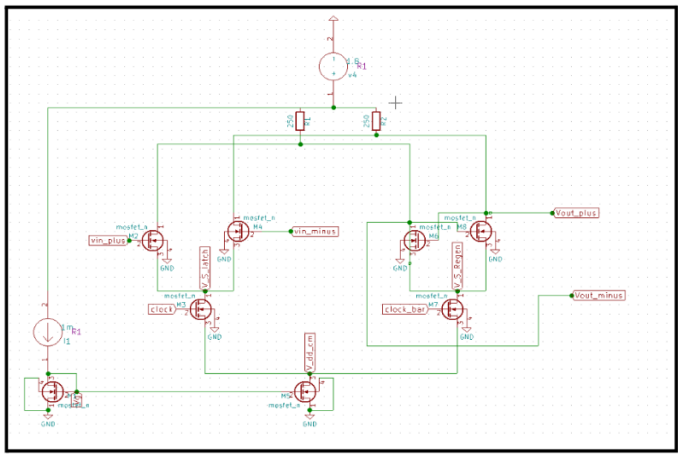

Figure 4.52: Circuit diagram

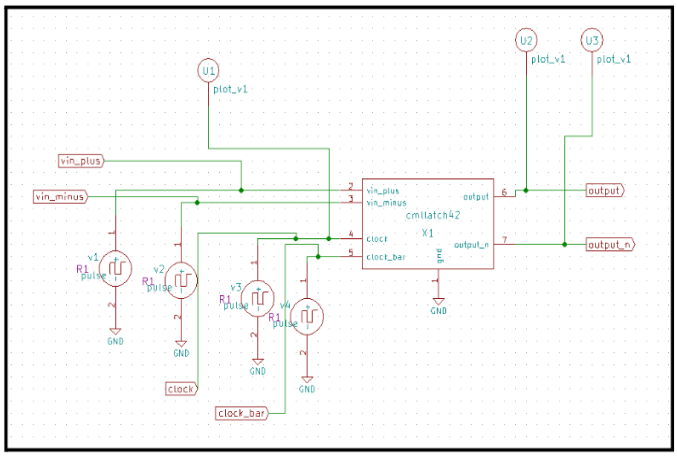

Figure 4.53: Sub-circuit

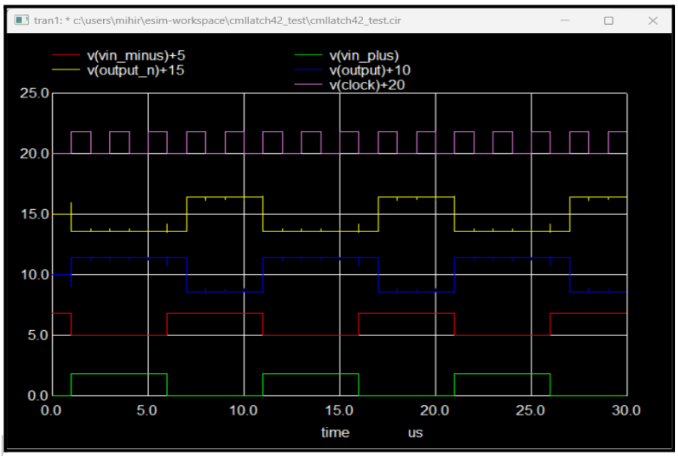

Figure 4.54: Output waveforms

4.19 High Efficiency Dc-Dc Buck Boost Converter

4.19.1 Circuit details

The circuit is made by joining two converters, a buck converter, and a boost converter. Buck converter is a DC to DC power converter which steps down the voltage from its input to its output. Boost converter works exactly opposite to buck converter; it steps up the voltage from its input to its output. The circuit works on both principles of the buck converter and boost converter. The designed circuit is a combination buck and boost converter parallelly, therefore, we have to connect inductor L2 and diode D2 in the circuit. The proposed DC-DC buck-boost converter will produce negative output voltage with a low duty cycle and produce high voltage gain. The MOSFET present here worked as a high-frequency switch. Inductor L1 stores energy when the MOSFET switch is closed and supplies it to load and capacitor when the MOSFET switch is open. To store energy to transfer to output and filter it to get smooth voltage is the function of the capacitor. The proposed converter is arranged by 5V input DC source for superior efficiency, a MOSFET switch which is considered as a switching device where the switching has been set to 20KHz, as well as inductors L1 L2 set at 35mH, load resistance RL at 50Ω and output filter capacitor CL at 1.1µF. The output voltage of the proposed DC-DC buck-boost converter is controlled by altering its MOSFET switch. DC-DC Buck-Boost converters can be developed by architecture improvement and by lowering parasitic resistance and capacitance.

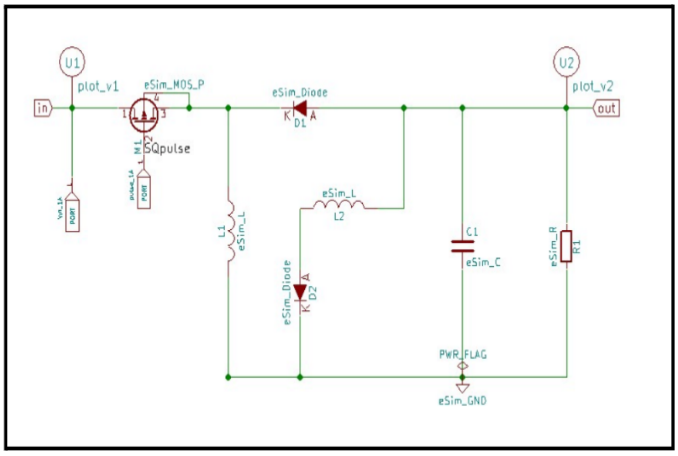

Figure 4.55: Circuit diagram

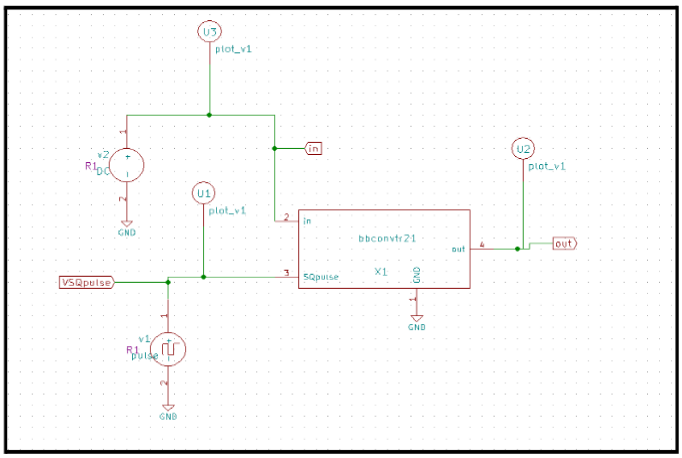

Figure 4.56: Sub-circuit

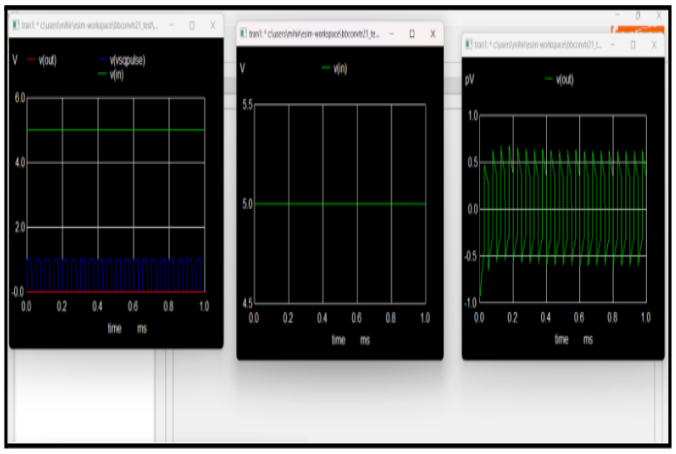

Figure 4.57: Output waveforms

4.20 Gilbert Multiplier Cell

4.20.1 Circuit details

The Gilbert Multiplier Cell is an enhanced version of the source coupled cell and this allows four quadrant multiplication. Two cross coupled source coupled pair forms the structure of the circuit. It produces a particularly useful transfer characteristic. The circuit consists of mainly 4 transistors namely M1, M2, M3, M4. The DC transfer characteristics of the multiplier circuit are the product of the hyperbolic tangent of the two input voltages. The multiplier cell always remains in the saturation region during normal operation. Used in this way the circuit is capable of performing precise multiplication of one continuously varying analog signal by another. the input signal is given at the source terminal junction of the two source coupled cells and the output is taken at the drain terminal of each source coupled cells. Furthermore, the collected output from the drain terminal is passed to a series of three inductor capacitor networks thereby preventing the loading effect at the output terminal of the device. The circuit can operate at lower supply voltages and better noise performance due to the low parasitic ohmic resistance of the inductors. The lower common-source transistors are fed by the differential mm Wave LO signals and the upper quad is composed of thick oxide transistors ensuring reliability against high swings at the drain nodes.

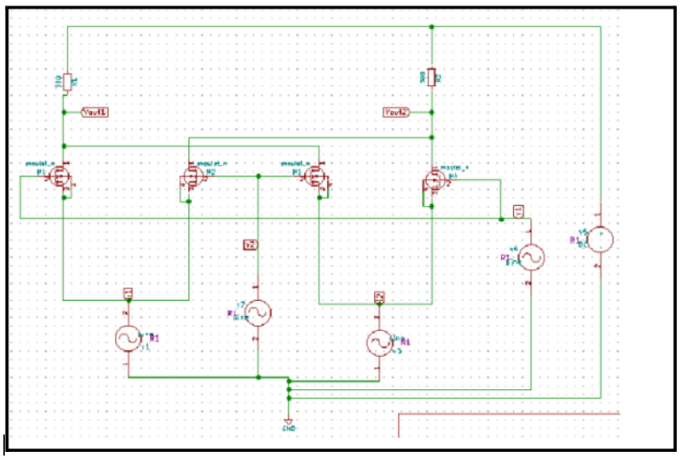

Figure 4.58: Circuit diagram

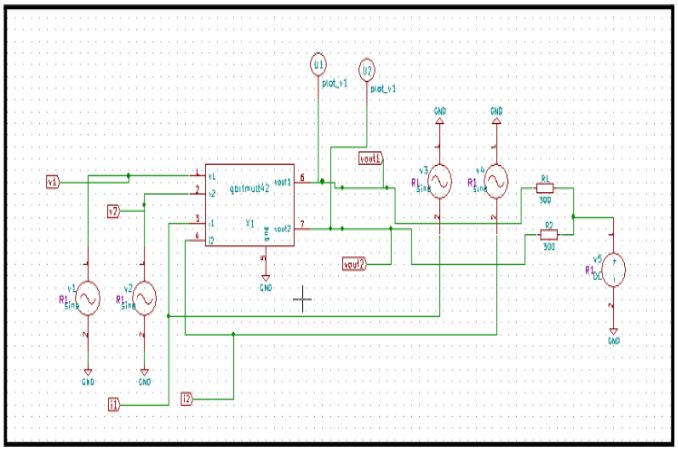

Figure 4.59: Sub-circuit

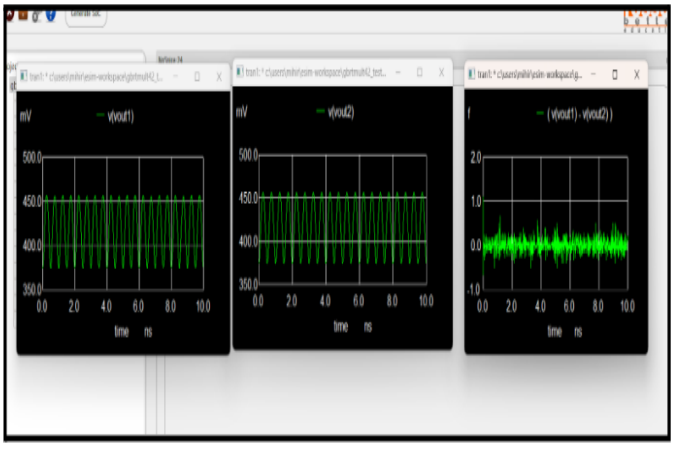

Figure 4.60: Output waveforms

4.21 32-bit ALU

4.21.1 Circuit details

The proposed ALU is capable of 4 operations- addition, subtraction, logical AND, logical OR on 32 bit numbers. here, I have implemented addition & subtraction & with addition of logical AND which is already part of Full adder logical OR, this block can be called as 1 bit ALU such 32 blocks are cascaded to form 32 bit ALU of which operation can be controlled by 4:1 MUX. Talking about 32-bit ALU which i studied for this project (reference website in readme file) 32-bit ALU which takes two 32-bit values is capable of 4 operations – addition, subtraction, bitwise AND, bitwise OR which is selected by 2 control lines generate one 32-bit output. Along with that, it also has 3 status outputs – zero, carry, overflow. A typical 32-bit ALU is rather much more complex than this but its simplified version of ALU which can be easily implemented using basic logic gates. The 4 logic gates which are used in this are AND, OR, NOT XOR. Along with that to choose between various operations to perform, multiplier is used which is controlled by control signal connected to its select lines. VLSI runs on 3 main factors – Area, Power & Performance, & therefore, to use area in efficient manner, we are going to use inversion for one of the inputs while performing subtraction which in result allow us to use same adder circuitry for subtraction purpose too.

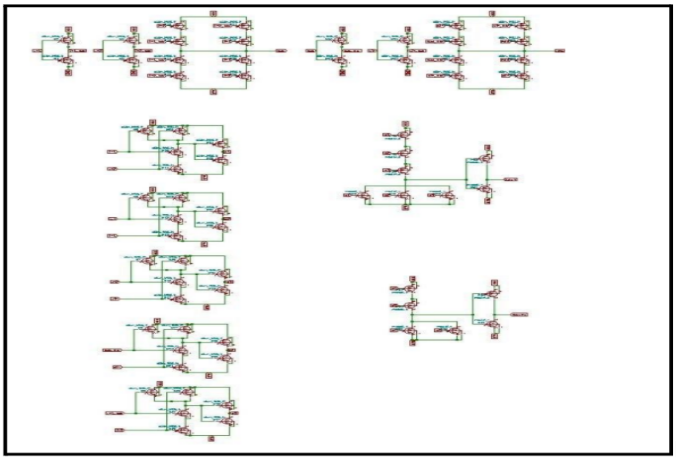

Figure 4.61: Circuit diagram

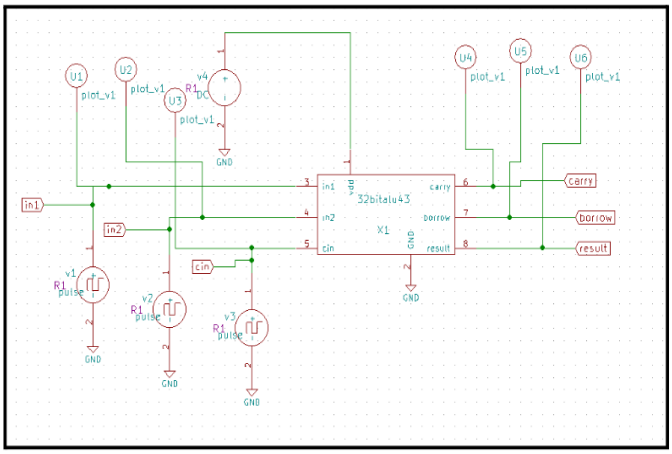

Figure 4.62: Sub-circuit

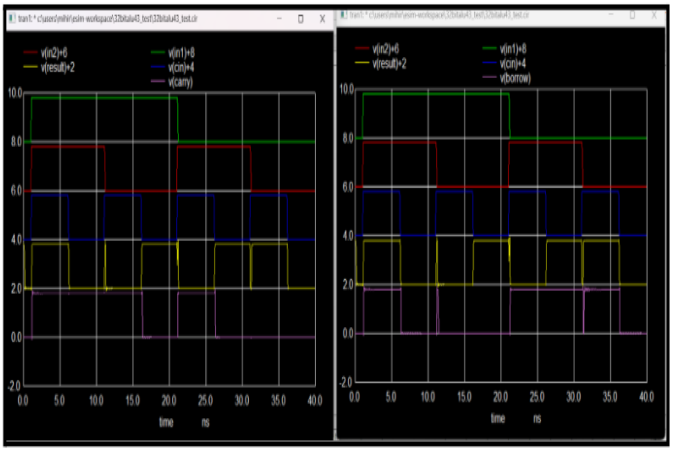

Figure 4.63: Output waveforms

4.22 Full Adder using CMOS

4.22.1 Circuit details

The full adder circuit has 3 inputs – A, B and Cin. It has 2 outputs – Sum and Cout, and thus there are 2 sets of pull-up and pull-down networks. As we know, the pull-up network consists of pMOS and the pull-down network consists of nMOS transistors. In the circuit for the Carry output, there are 5 of both pMOS and nMOS transistors. Now, we know that the equation for the Sum output is conventionally given by (A exor B exor C). But, this gives rise to complications in designing the circuit as there would be a lot of transistors, and the circuit would be very expansive. Thus, we go for an alternative path and take the Cout bar output and feed it into the Sum circuit as the 3rd input. This eases the equation for the Sum output by expressing it in terms of A, B, Cin and Cout, rather than exor operations. It also reduces the number of CMOS transistors required in the Sum circuit and hence the overall design. We obtain the required number of both pMOS and nMOS as 7 for the Sum. Also, since CMOS circuits always provide an inverted output, we need to add inverter circuits to both the Sum and Cout outputs to acquire the originally required outputs - hence costing us 2 more of both pMOS and nMOS for each output inverter. The number of CMOS transistors used thus comes to a total of 28. NOTE : The waveform obtained although correct and in accordance with the truth table of Full Adder, does not exactly resemble the reference waveform provided in the literature survey report.

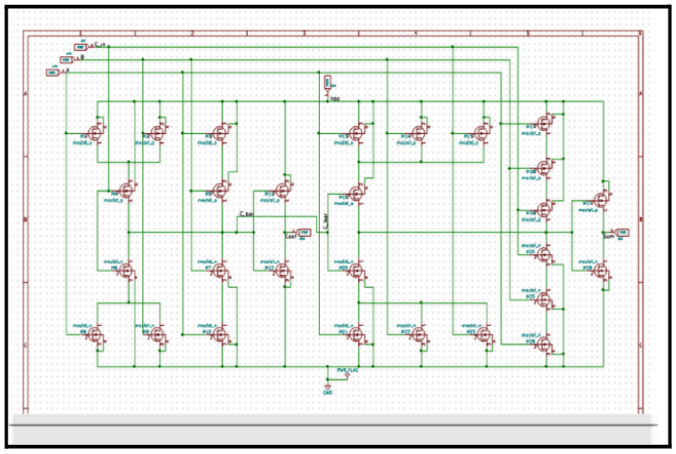

Figure 4.64: Circuit diagram

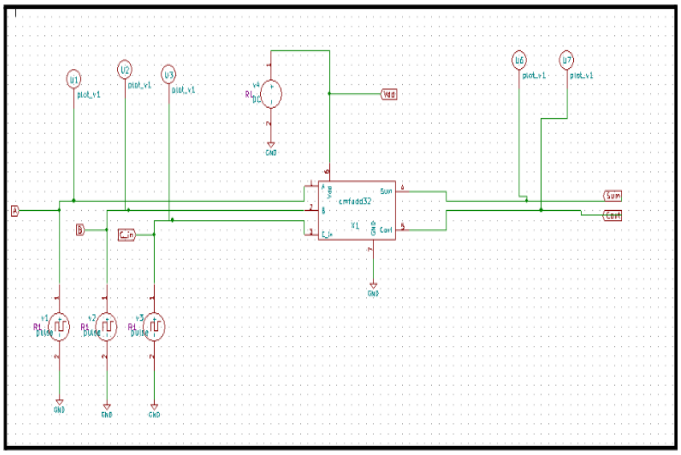

Figure 4.65: Sub-circuit

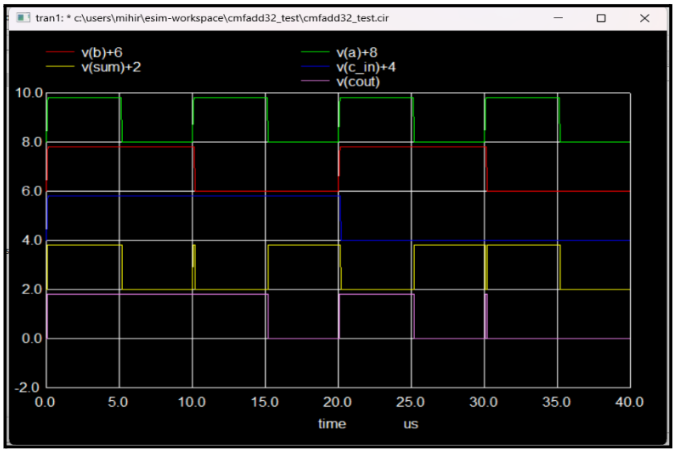

Figure 4.66: Output waveforms

4.23 Full Adder implementation on Dynamic CMOS Logic

4.23.1 Circuit details

The circuit is implemented using the using CMOS logic (combination of MOSFETS(i.e.NMOS and PMOS)) . The Full adder circuit Has two output (i.e. Sum output and Carry ouput). At first, The circuit. Equations are reduced for implementing the circuitry. The circuit totally consists of 40 mosfets considering both Sum and carry circuit. As CMOS logic gives an inverted output an Inverter is used For realising the Actual output. The inputs to the circuit Are A, B, cin. A1, B1, cin1. Here A1, B1 and cin1 are the inverted values of input A, B and cin respectively Which are used While realising The Ouput of Sum Circuit. The equation realised for obtaining Sum output is A1(B1cin+Bcin1) + A(B1cin1+Bcin). Similarly the equation realised for obtaining Carry output is cin(A+B)+AB. The Complete circuit simulation is done Through esim simulator Where Annotations check,Electrically rule check and Netlist generation Tasks are proceeded. The Output of Simulation(Netlist) is mapped with Librabries of Skywater 130nm PDK . Here Skywater 130nm technology is a mature 180nm-130nm hybrid technology Developed by Cypress semiconductors and Later Collabarated with Google which is open sourced for industry usage . The Output Waveforms for the Designed circuitry with Generated Netlist Mapped with SKY130 nm Libraries are checked using Ngspice (Which is also a open Source Spice simulator Tool). Thus the output waveform is Then checked for correctness and functionality For the implementation of Full adder circuit.

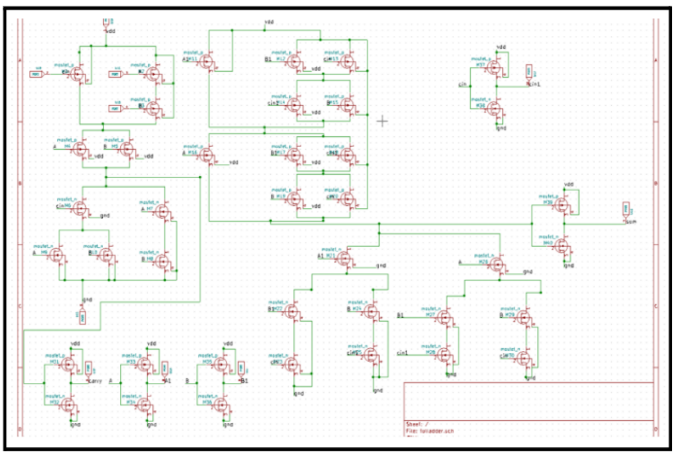

Figure 4.67: Circuit diagram

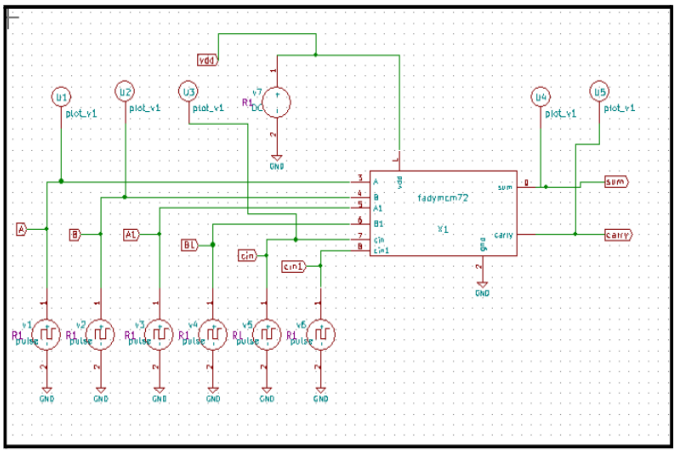

Figure 4.68: Sub-circuit

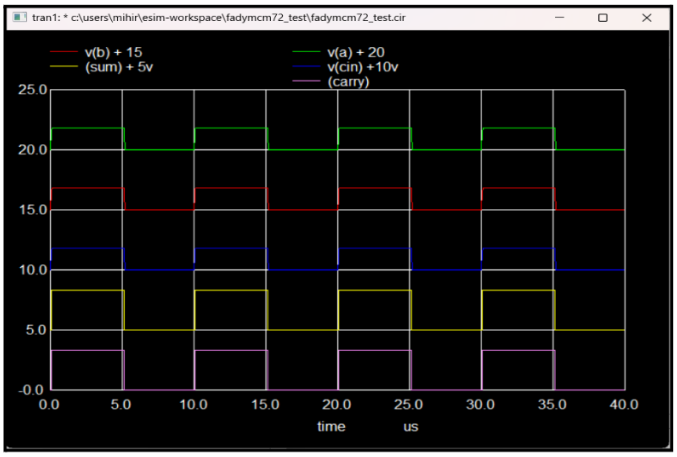

Figure 4.69: Output waveforms

4.24 CMOS SCHMITT TRIGGER

4.24.1 Circuit details

The input of the Schmitt trigger is tied to the gates of four CMOS devices. The upper two are PMOS and the lower two are NMOS. Transistors M6 and M3 act as source followers and introduce hysteresis by feeding back the output voltage. The Schmitt trigger circuit can be divided into two parts depending on whether the output is high or low. When the output is low and the input is high the transistors M5 and M4 are OFF and M6 is ON. As M6 is ON it creates an additional path to the ground for node X. When Vin makes the transition from Vdd to 0, transistors M5 and M6 will turn ON. But some current charging output will be diverted through this node X to the ground until the output goes high and turns OFF M6.So Vin has to go much lower for the transition. Similarly, When the output is high and the input is low the transistors M1 and M2 are OFF and M3 is ON. So when M3 is ON there will be a path to the Vdd for the node Y. When Vin makes the transition from 0 to Vdd, transistors M1 and M2 will turn ON and will try to pull the Vout to the ground but before that, it has to sink the additional current from Vdd, until the output goes low and turns OFF M3. Hence, Vin has to go much higher to make the output low. The upper and lower threshold voltages of the Schmitt trigger are set by choosing appropriate W and L of PMOS NMOS transistors.

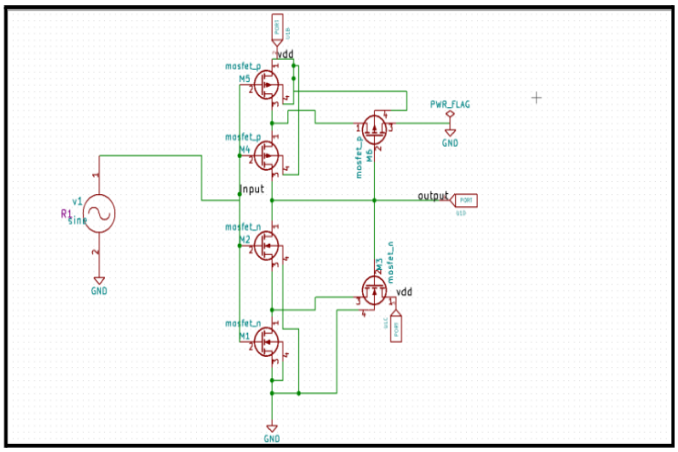

Figure 4.70: Circuit diagram

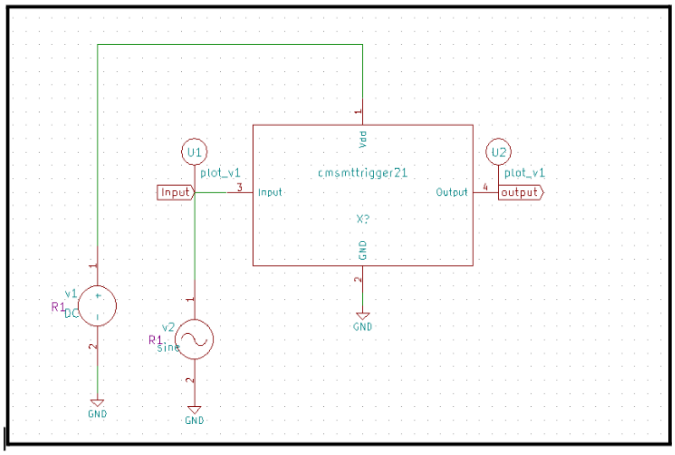

Figure 4.71: Sub-circuit

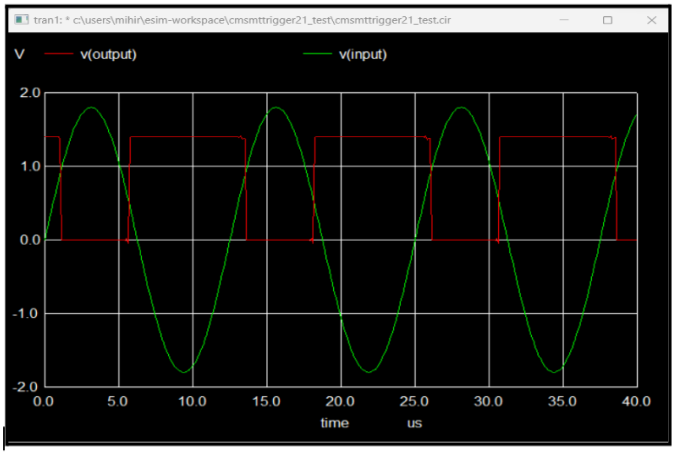

Figure 4.72: Output waveforms

Chapter 5

IPs done by Ayush Kashyap

5.1 Ideal Circuit:Design of low transconductance OTA

5.1.1 Circuit details

Operational Amplifiers Opamps were widely used in many analog circuit implementations.But due to power hungry and frequency limit characteristics Opamps has been replaced by Operational Transconductance Amplifier OTA.OTA is widely used for the conversion of voltage to current. In OTA differential input voltage produces current as output and it is a voltage controlled current sources VCCS.Low transconductance transconductor and low power is required for biomedical applications. Transconductance has importance in CMOS analog circuits it indicates the ability of device to transfer input voltage to output current. The PMOS current mirrors are placed in series and parallel to achieve the Transconductance. An ideal Operational Transconductance Amplifier OTA has two input voltages with infinite input impedance. The voltages Vin- as v1 and Vin+ as v2 are the inverting and non-inverting input voltages applied to the circuit. The current Ibias is the bias current which mainly helps in controlling the gain of the amplifier. The bias current Ibias is proportional to the transconductance of Operational Transconductance Amplifier OTA.The transconductance can be calculated by using series parallel as Gm is equal to gm1/N2 where transconductance of the transistor M7 is gm1 and Number of transistors in series and parallel is N. series parallel current division was applied in symmetrical OTA to achieve low transconductance with extended linear region.

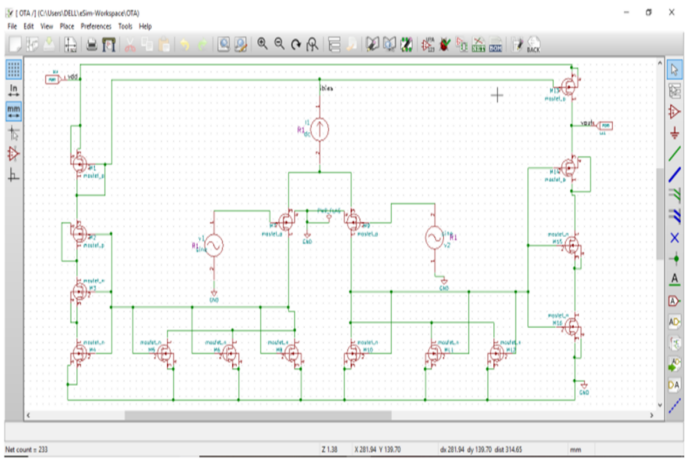

Figure 5.1: Circuit diagram

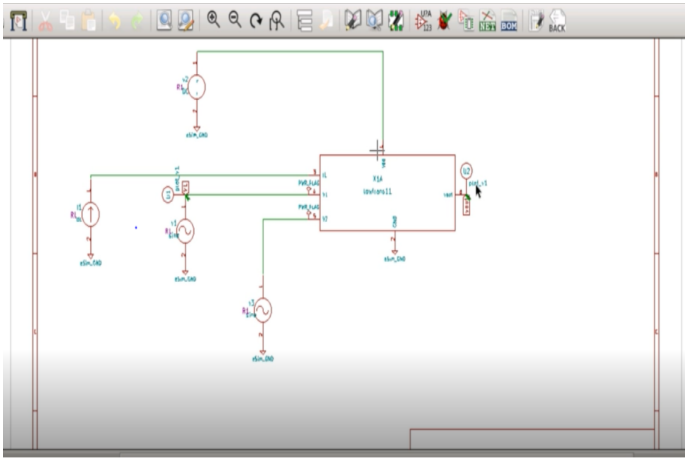

Figure 5.2: Sub-circuit

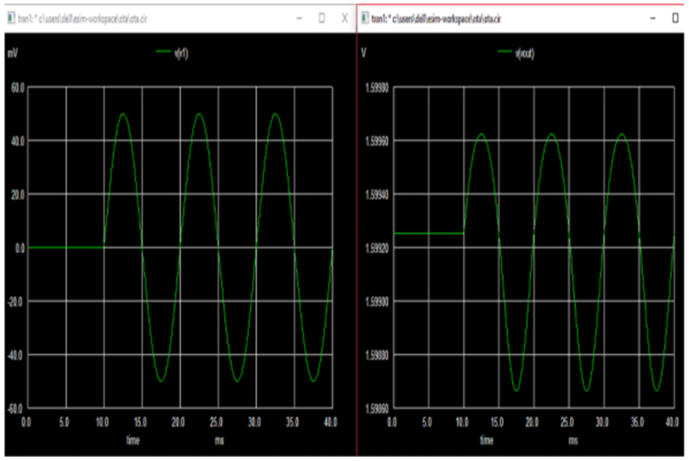

Figure 5.3: Output waveforms

5.2 RING OSCILLATOR

5.2.1 Circuit details

Odd number of stages gives the inverted output when the input voltage is given at once to the first stage,the oscillation starts. When oscillation begins, Barkhausen Criteria must be satisfied to sustain stable oscillation. Ring Oscillators are composed of a number of inverters or delay stages connected to each other in the form of a chain, with the output of the last stage fed back to the input of the first The most important factor in ring oscillator is gate delay because in devices fabricated with MOSFET, gate cannot switch immediately. The gate capacitance needs to be charged before current flows between drain and source so that every inverter takes time to give output. Therefore increase in the number of stages of ring oscillator increase the gate delay. Odd number of inverter stages used to give the effect of single inverter amplifier with a negative feedback gain of greater than one so that the output will be in opposite direction to the input and it will be amplified with an amount more than the input. Amplified,inverted output is then propagated to the input with delay where it is amplified and inverted again. Digital and analog circuits have an important factor known as the propagation delay or gate delay. Propagation delay in ring oscillator is defined as the time difference between input and output. And the applications are Ring oscillators can also be used to measure the effects of voltage and temperature on a chip. The voltage-controlled oscillator in most phase-locked loops is built from a ring oscillator.

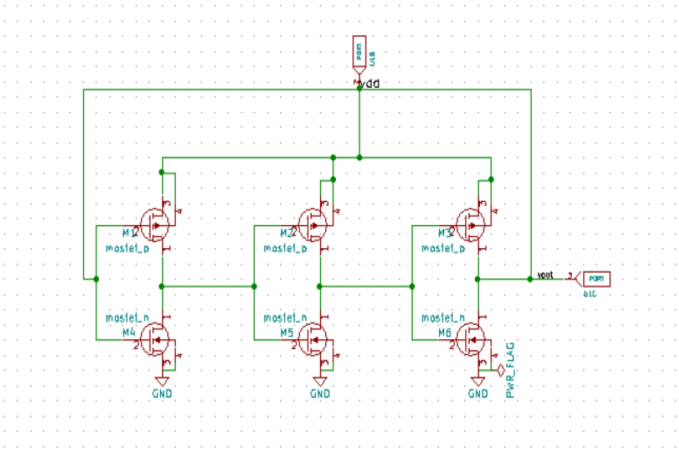

Figure 5.4: Circuit diagram

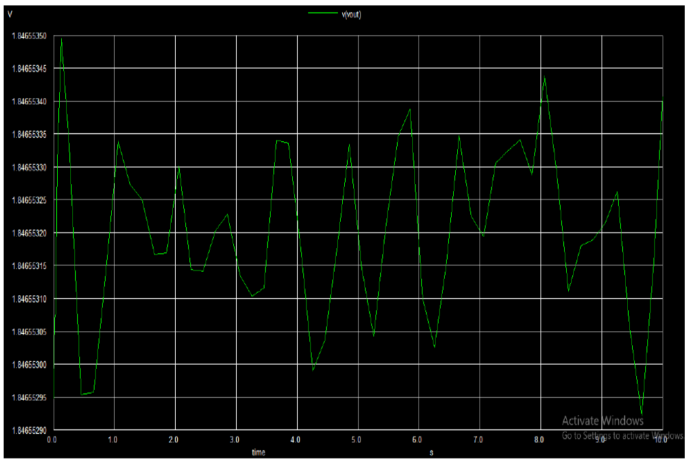

Figure 5.5: Output waveforms

5.3 CMOS Differential cascade voltage switch logic(DCVSL) XOR-XNOR

5.3.1 Circuit details

When the differential pairs of MOSFET devices are cascaded into strong combinational logical tree networks, then we can achieve a design leverage in CVSL which is within a single circuit delay and is capable of implementing complex Boolean logic. A DCVS Logic is based on 2 to 1 Multiplexer which is used as an important element in many various circuit designs such as implementation of memory circuits and FPGA. A differential gate requires that each input is provided in a complementary format, and it produces complementary output in return. The feedback mechanism ensures that the load is turned off when it is not needed gives rise to the DCVSL family in CMOS circuits. The circuit uses 2 static PMOS in the pull up network. The pull down networks PDN1 and PDN2 are built using NMOS and are mutually exclusive. The PDN networks are connected as the inputs to the PMOS in a crossed manner. In general, the PMOS devices are deemed to be active low devices i.e conducts when given low voltage and NMOS being active high devices i.e conducts when given high voltage. The low GND and high VDD voltages that are supplied are mapped to the binary 0 and 1. When inputs are given to the a and b terminals, the actual and complementary values are taken. There is only one PDN active at the same time consideringthe logic. The PDN that is not active is isolated from the VDD and the ground. This circuit can further be used in adder and multiplier circuits. The outputs of the xor and xnor gates are obtained simultaneously

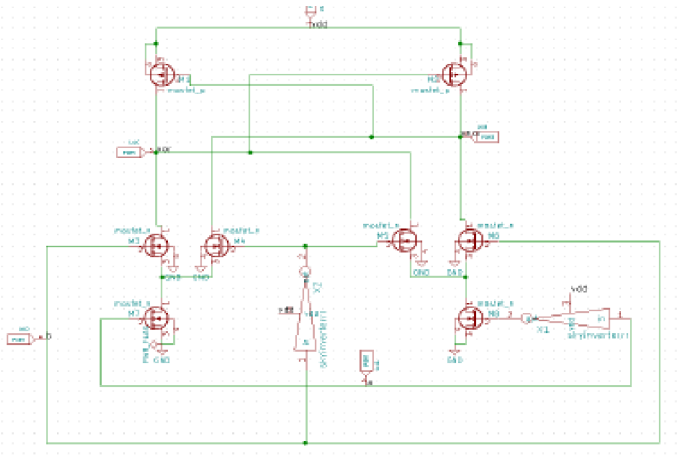

Figure 5.6: Circuit diagram

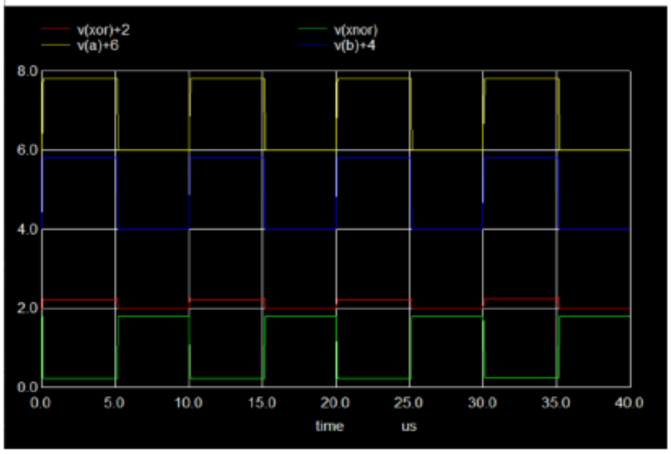

Figure 5.7: Sub-circuit

5.4 Low Noise Low Power Amplifier for Biomedical Applications

5.4.1 Circuit details

CMOS technologies paved way to increasing market of mobile and portable electronic devices. This growth is driven by the continual integration of complex analog and digital building blocks on a single chip. The operational transconductance amplifier is an important analog building block and for many applications is the largest and most power consuming. Recently, one of the most commonly used architectures whether as a single-stage or first stage in multistage amplifiers had been the folded cascode amplifier for its high gain and reasonably large signal swing in the present and future low voltage CMOS processes. Biomedical signals have weak amplitude and low frequency so we need to amplify these signals. Amplifiers should have basic features like high CMRR low power consumption low input referred noise for good performance in the field of biomedical engineering. There are many ways to design the amplifier with above conditions. For example implementation here is two stage gate driven folded cascode amplifier. In addition to reduce the flicker noise PMOS input transistors with large gate areas are used for low power operation. Ib current in M0 Mc1 and Mc3 is mirrored by Mb then M0 supplies the first stage current. M13 and M14 currents are controlled byMc1 and Mc2 .Equal drain potentials is maintained by M13 and M14 across the Ma3 Mb3 and Ma4 Mb4 in order to improve matching. Cc and Rc are used between the drain of M8 and output terminal for compensation, So it improves the phase margin and GBW

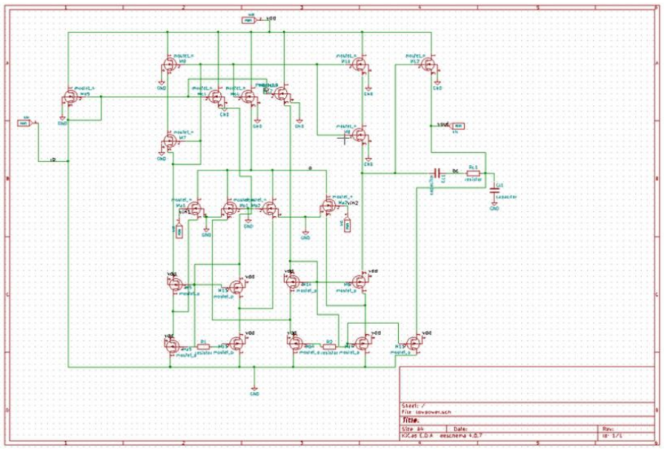

Figure 5.8: Circuit diagram

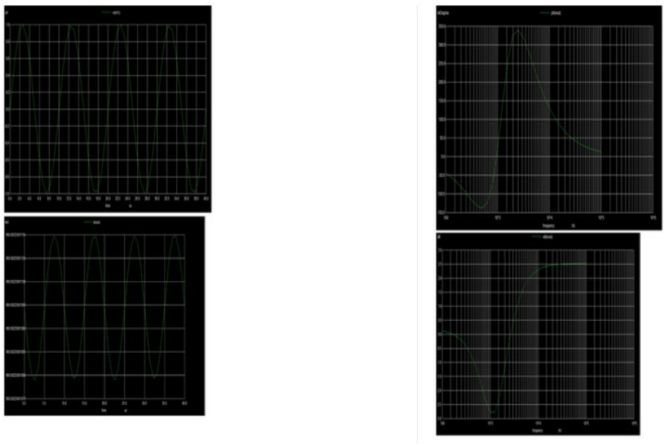

Figure 5.9: Sub-circuit

5.5 ONE BIT MIRROR ADDER

5.5.1 Circuit details

One bit Mirror adder adds up three binary inputs – A, B, Cin and produce 2 binary outputs – Sum and Carry out. Mirror adder does not have complementary pull-up and pull-down circuit. Instead, it has symmetric mirroring circuit. Which means, the same circuitry is found for both NMOS logic and PMOS logic. The circuit that needs to be implement a onebit mirror adder is shown in Fig1. The design implemented gives us Sum and Cout and the equations are obtained from normal one-bit full adder sum and carry out equations. If you see 1-Bit mirror adder you might not see much difference in processing time but if you construct multi-bit mirror adder, the advantages mentioned below can be observed especially in Carry ripple adder. Advantages: 1. In carry ripple operation, the critical path is from Cin propagated till Cout so Carry will be computed fast in mirror adder which will help in fast up the multi bit carry ripple adder. 2. A smaller number of transistors were used to implement logic i.e., 28 transistors. 3. We do not need inverted inputs. 4. It will have a uniform layout. For simulating the spice generated from the eSim, ngSpice is used. The inputs in the spice were added in such a way that 8 combinations of the inputs can be verified. To get the proper output I have same width and length ratio for all NMOS and PMOS.

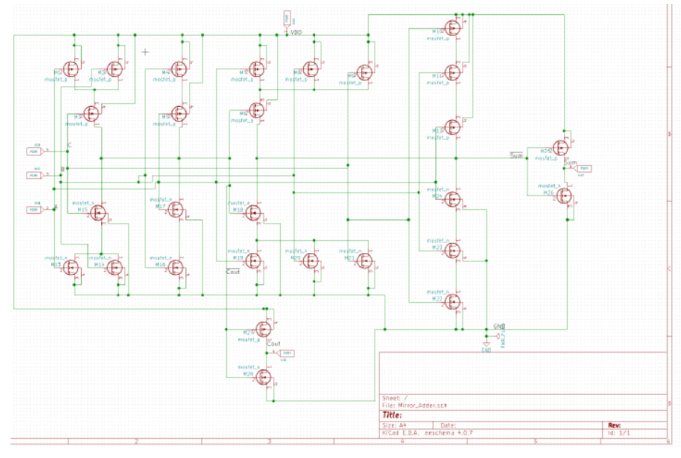

Figure 5.10: Circuit diagram

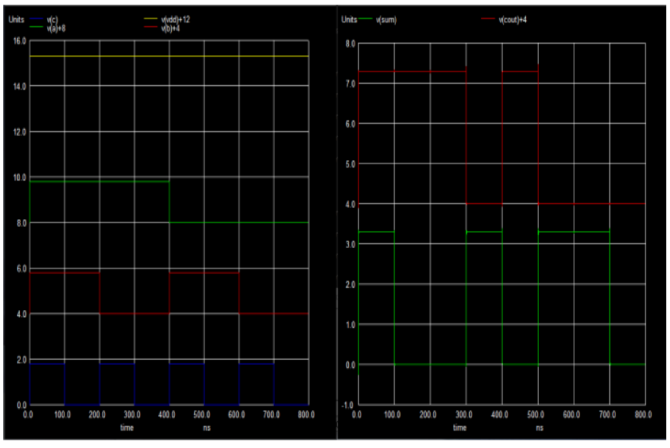

Figure 5.11: Sub-circuit

5.6 MIRROR WITH MULTIPLE OUTPUTS

5.6.1 Circuit details

The current mirror circuits are simple current sources whichgives constant current In other words we can define it as a A two terminal circuit whose output current is independent of the output terminal voltage and depends only on the input current Generally it is used to generate a replica of given reference current The current mirror circuits are based on the principle if the gate to source voltage of two identical MOSFETs are equal then the drain current flowing through them is equal A current mirror can be thought as a current controlled current source Ideally the output impedance of a current source should be infinite and capable of generating or drawing a constant current over a wide range of voltages A current flows through M1 corresponding to VGS1 Since VGS of all the MOSFETS are shorted ideally the same current has to flow through the all other MOSFETS but by adjusting the W to L ratio we can get a different current as per our requirement a multiple of the current in M1 or the fraction of the current flows through M2 M3 M4 M5 If the MOSFETs are of the same size the same drain current flows in each MOSFET provided M2 M3 M4 M5 stays in the saturation region The circuit diagram for the basic current mirror with multiple output currents has been uploaded in the reference circuit file this circuit is obtained by extending the basic current mirror to give multiple outputs here i have used all n type MOSFETS

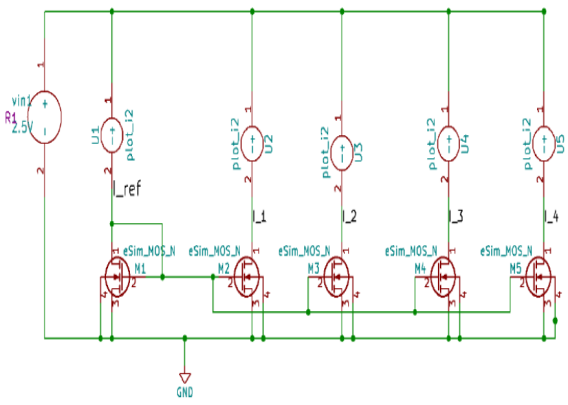

Figure 5.12: Circuit diagram

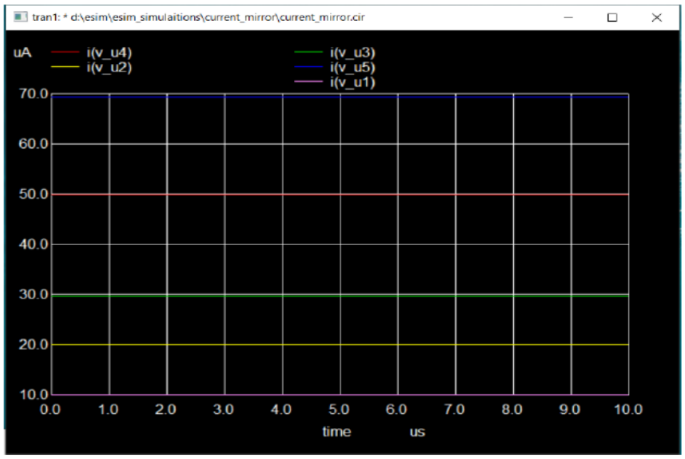

Figure 5.13: Sub-circuit

Chapter 6

IPs done by Narra Hemanth

6.1 THREE PHASE INVERTER

6.1.1 Circuit details

The schematic diagram considered here is a nine-phase voltage source inverter where a DC supply is converted to a nine-phase AC supply. There are three, three-phase inverter sub circuits in the circuit shown in figure.1. Each sub circuit consists of six electronic switches as shown in the sub circuit figure .2, Switches in the same limb should not conduct simultaneously as it leads to a short circuit of the supply. The excitation sequence is S1, S6, S3, S2, S5, and S4. Each switch conducts for 180 degrees and delays by a phase angle of 60 degrees as mentioned in the previous sequence. The output from this inverter is fed to a 3-phase balanced load. The output voltage is 120 degrees out of phase. As a three sub circuit works combined to get the nine-phase voltage. The simulated circuit does not use any anti-parallel freewheeling diode connected across each electronic switch. In this case, the output drove only for R load, if we use L C load then we should use an anti-parallel freewheeling diode to protect switches from discharging current. The combined Waveform of loads A, B, and C are shown in the figure. waveform.1. The other three wave forms show quasi-square wave forms between each combined load of A and B, similarly, B and C, C and A, as shown in the figure. Waveform.2, Waveform.3, Waveform.4. The input Dc voltage is 25v given to the inverter and the output drawn from the inverter is 40v Ac Here the schematic diagram is drawn using esim and simulated by ngspice.

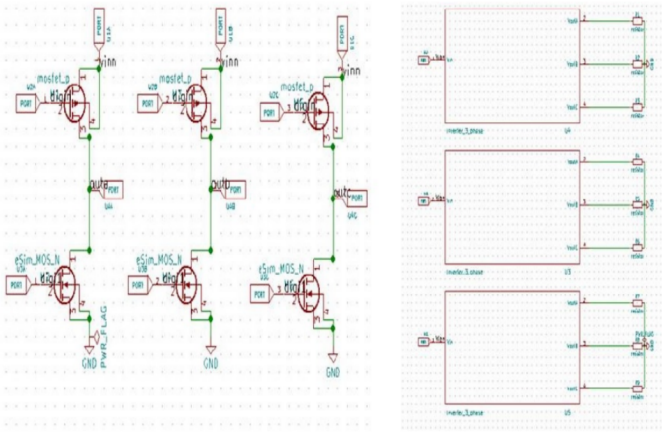

Figure 6.1: Circuit diagram

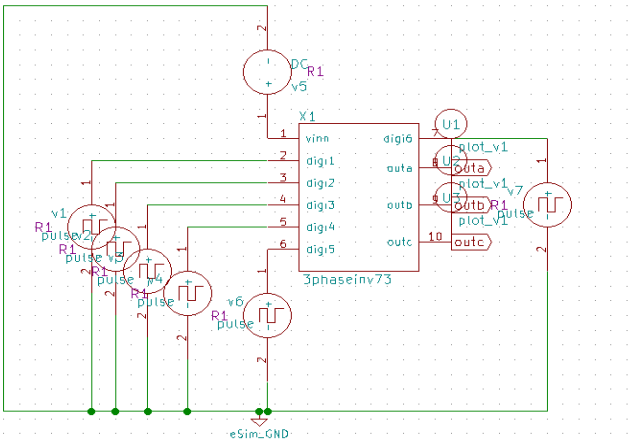

Figure 6.2: Sub-circuit

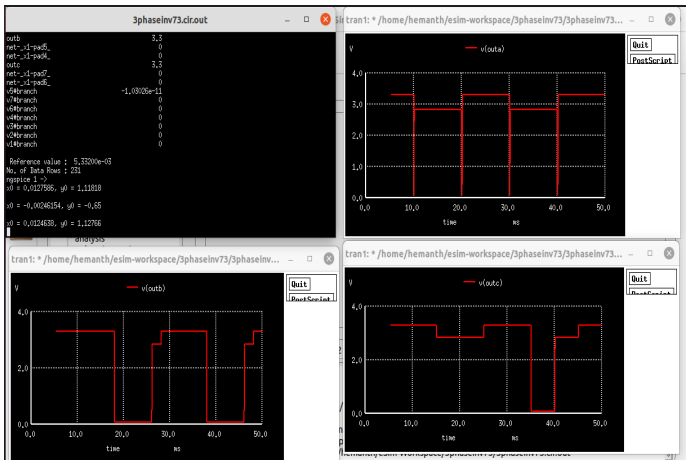

Figure 6.3: Output waveforms

6.2 Low power and High speed 1 bit full adder circuit

6.2.1 Circuit details

Many applications like DSP architectures which are application specific and microprocessors have been widely used in many VLSI Systems. In most of these systems, the adder is a component of the Critique, which defines the systems overall performance. As a result, enhancing the performance of the one bit adder cell is a critical objective as Due to the rapid rise of technologies in mobile communication and computing, the construction of low-power VLSI systems has recently acquired traction. Battery technology, on the other hands not growing as quickly as microelectronics technology. However, the amount of energy available to mobile systems is restricted . As a result, designers are faced with increased constraints, such as high speed, high performance, tiny silicon area, and low power consumption. So, in today's VLSI world, developing a low-power, high performance adder cell is essential. This adder is made up of ten CMOS transistors with a 4T XOR logics. This design is known as a low-power adder since it does not have a direct link to the ground and can re-apply the load charge to the control gate, which is why it is also known as a Static energy recovery complete adder . The design technique takes three inputs and produces two sum and carry outputs. The low power consumption of this circuit is a benefitted in small area and less PDP compare to pass transistor logic (PTL).

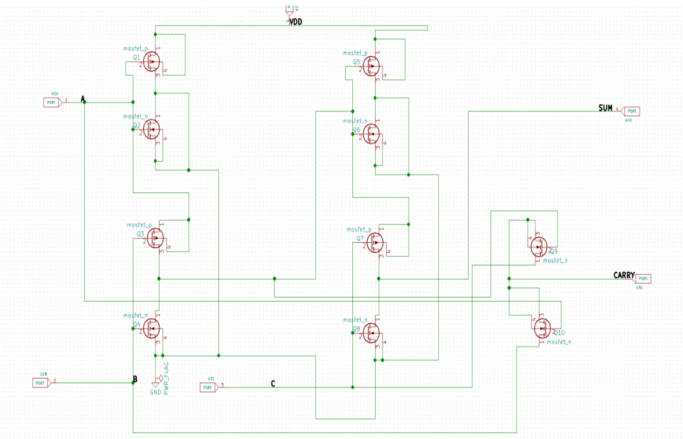

Figure 6.4: Circuit diagram

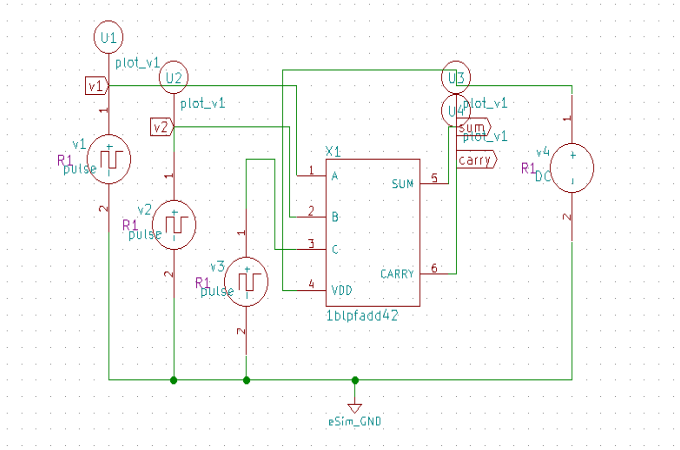

Figure 6.5: Sub-circuit

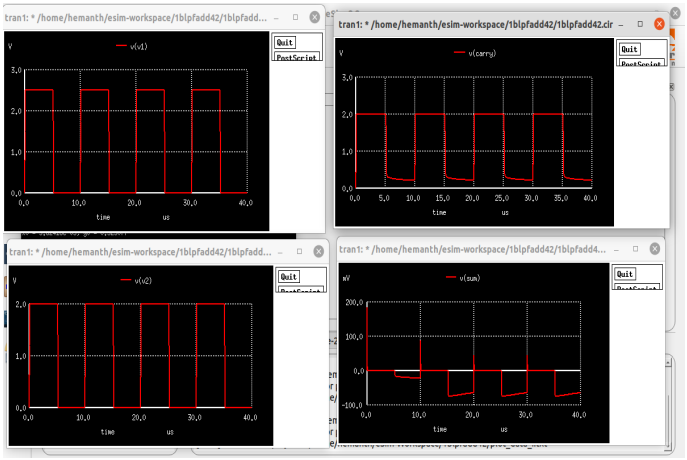

Figure 6.6: Output waveforms

6.3 Sziklai Pair Amplifier

6.3.1 Circuit details

This project focuses on design of a Sziklai Pair Amplifier using Google Skywater (sky130) Technology node with operating voltage of 1.8V and 3.3V. The project is build using Open Source Tools like Magic, Sky130PDK and eSim. Refer following website for more details on Sziklai Amplifier: https://en.wikipedia.org/wiki/Sziklai pair.

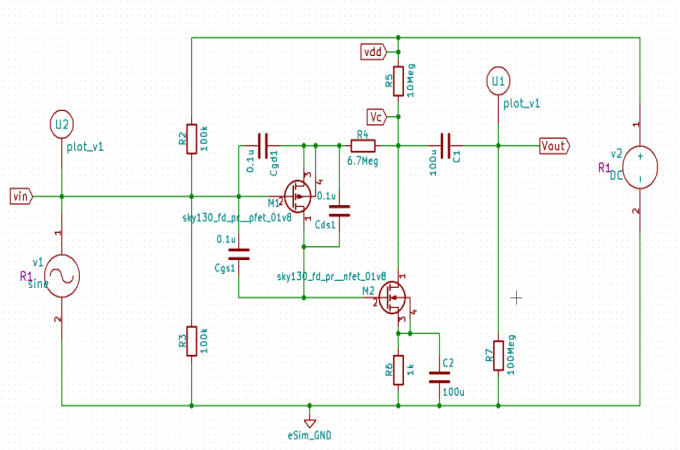

Figure 6.7: Circuit diagram

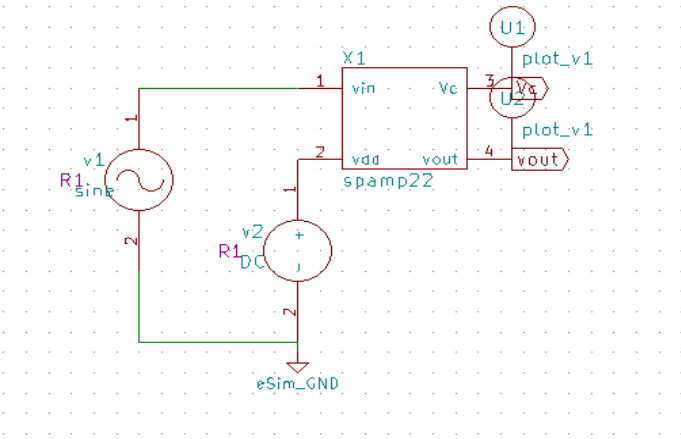

Figure 6.8: Sub-circuit

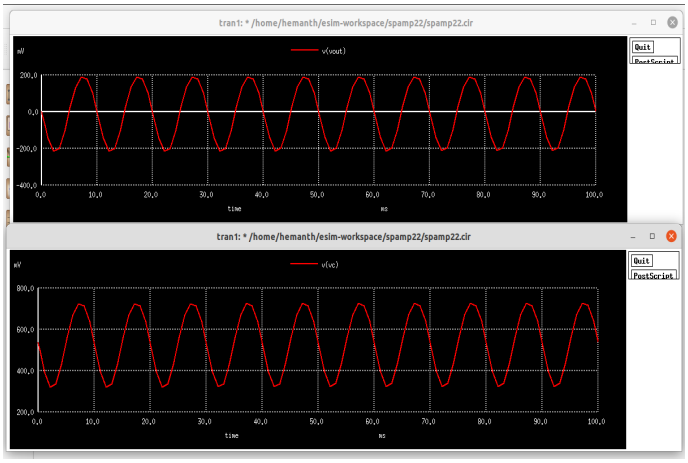

Figure 6.9: Output waveforms

6.4 Implementation of a 3-bit CMOS Wallace Tree Multiplier

6.4.1 Circuit details

In CMOS technology both NMOS and PMOS transistors are used to realize the logic which is an advantage of CMOS over NMOS and bipolar technology, also has lesser power dissipation[1]. This helps in reducing the area covered by the circuit and allowing to occupy more gates per square area. The structure is implemented using half adders, full adders, XOR and AND gates. In Wallace tree reduction, every bit is multiplied with every bit of the other number, then these partial products which have weight equal to the product of its factors are further reduced to obtain the respective weights by using half adders or full adders based on the size. The final result is calculated by the weighted sum of all these partial products. Through esim software, schematic was designed and netlist of the schematic was exported to perform simulation using ngspice. During simulation, I have passed four patterns to both the inputs "a" and "b" each 3 bits wide, which results in a 6-bit value. The first pattern inputs are a2a1a0 = 101, b2b1b0 = 010 so the output here is z5z4z3z2z1z0 = 001010, the second pattern inputs are a2a1a0 = 000, b2b1b0 = 011 and output z5z4z3z2z1z0 = 000000, the third pattern inputs are a2a1a0 = 111, b2b1b0 = 110, output z5z4z3z2z1z0 = 101010, the fourth pattern inputs are a2a1a0 = 100, b2b1b0 = 001 so the output here is z5z4z3z2z1z0 = 00100 A 3 x 3 multiplier designed using CMOS technology based on sky130 design elements shows a significant improvement in performance.

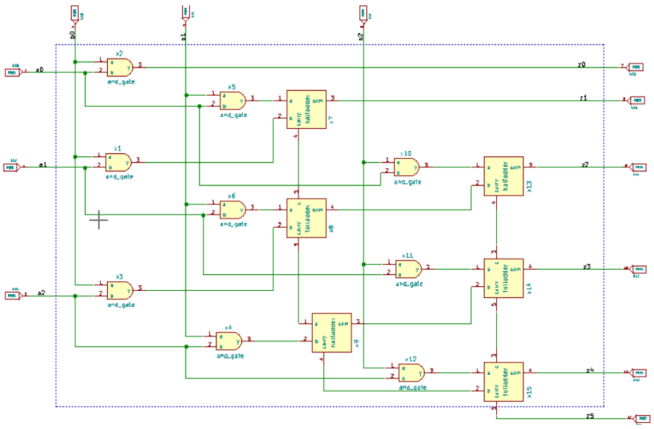

Figure 6.10: Circuit diagram

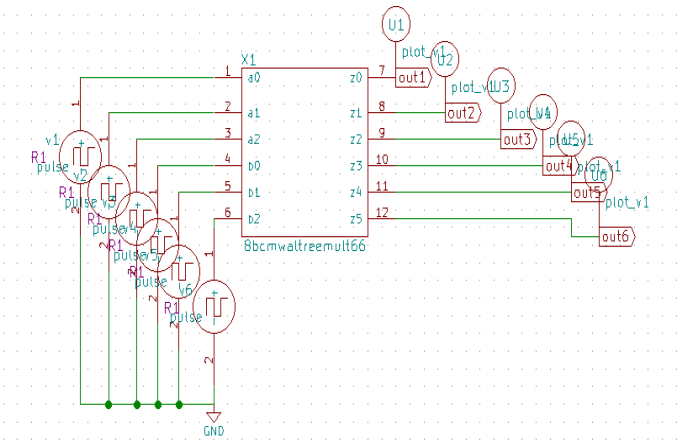

Figure 6.11: Sub-circuit

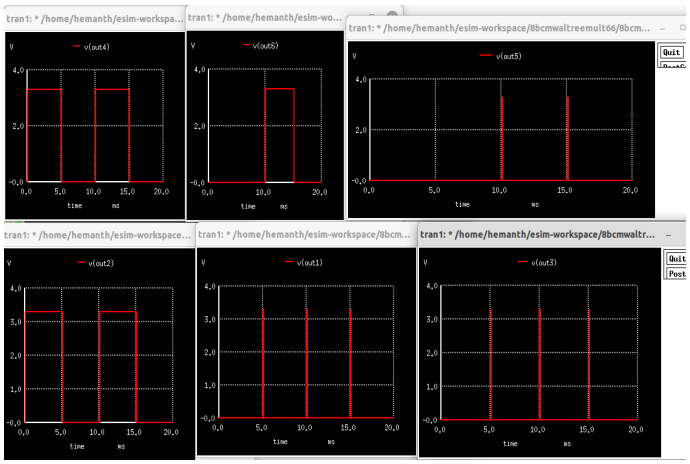

Figure 6.12: Output waveforms

6.5 Low Voltage CMOS Schmitt Trigger

6.5.1 Circuit details

CMOS Schmitt Trigger has two possible states trigger for circuit to change states is the input voltage level and changes only as input crosses a predefined threshold . Standard Schmitt Trigger is formed by a combination two sub circuit P and N sub circuit containing PMOS and NMOS respectively .Power consumption of CMOS consists of dynamic and static components . Since P sub circuit is connected to the path between the source voltage and output while the N sub circuit is connected between the path of output and ground. Therefore no static power consumption due to no direct path between source voltage and ground.In Low voltage Schmitt trigger circuit Part 1 of the designed circuit forms a NAND gate. Two PMOS M1 and M2 by a parallel and two NMOS M4 and M5 are formed by a series connections. Designing the PMOS in parallel the resistance of the P sub circuit is reduced by halves thus propagation delay can be reduced . Part 2 of the designed Schmitt Trigger consists of a PMOS M3 and NMOS M6 where both the MOSFET is directly connected through the gate terminal of each. The M3 act as pull up while M6 act as a pull down for the output at each case.By increasing width of PMOS it moves the switching threshold voltage towards vdd which makes hysteresis width more rectangular .When input vin is low only the P sub circuit will be considered and causes output to be high where both M1 and M2 are on but M3 is off hence the output voltage is pull to vdd . When input increases to vdd M4 and M5 is turned on while M6 is off. Output voltage is pull down to GND .It is taken across vout.

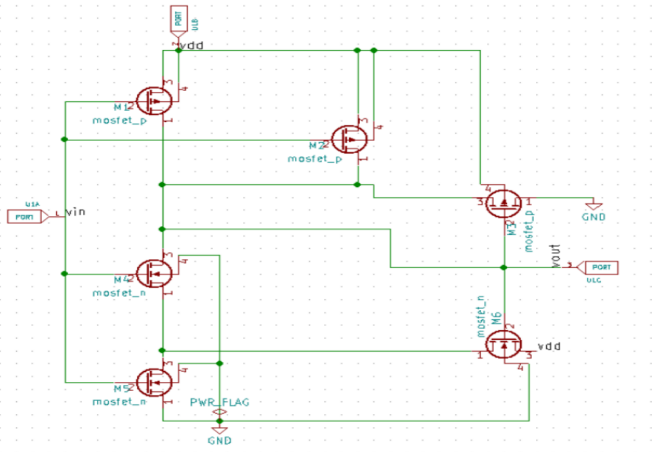

Figure 6.13: Circuit diagram

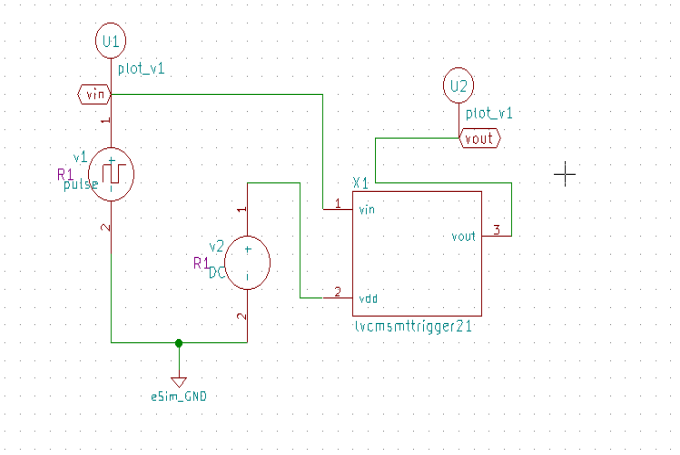

Figure 6.14: Sub-circuit

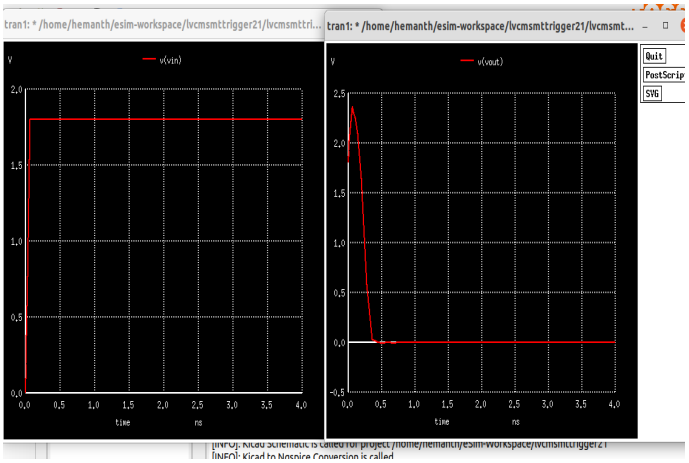

Figure 6.15: Output waveforms

6.6 Design of 8 bit Parity Generator using Pseudo NMOS logic

6.6.1 Circuit details

A 2 bit even and odd parity generator is constructed by cascading 2 Exclusive OR or XOR gates. XOR is a gate which gets 2 inputs and leaves an output. In XOR gate output will be true or high only when there is an odd number of one is given as input and output will be false or zero when even number of one is given as input. XOR gate is implemented using pseudo NMOS logic. Pseudo NMOS logic is a type of static cmos logic where complementary output is driven between Vdd and ground. This complementary output can be normalized by cascading an inverter to it. In this logic the number of transistors required is N plus 1 where N is the number of inputs. A complete logical expression is implemented using NMOS transistors with one PMOS transistor which is grounded . vdd is given to the source terminal in pmos. In this design we have taken two inputs A and B with one output PARITY BIT. T he type of parity generator is choosen by baising Dc source at pin 5 and pin 7. If DCunderscoreB is high odd parity is generated. If DCunderscoreB is low then even parity is generated. Odd parity denotes ODD PARITY BIT and even parity denotes EVEN PARITY BIT. Expression for ODD PARITY BIT is equal to A XNOR B. Expression for EVEN PARITY BIT is equal to A XOR B. Pin 1 is A Pin 2 is D which is B bar pin 3 is C which is Abar pin 4 is B pin 5 is DCunderscoreD pin 6 is vdd pin 7 is DCunderscoreB and pin 8 is PARITY BIT. We can get output plot from 8th pin.

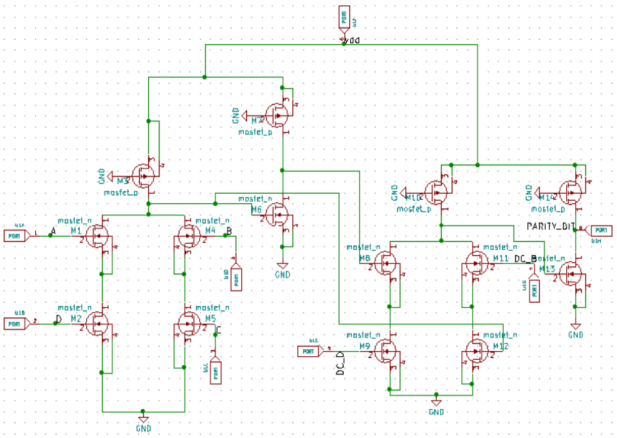

Figure 6.16: Circuit diagram

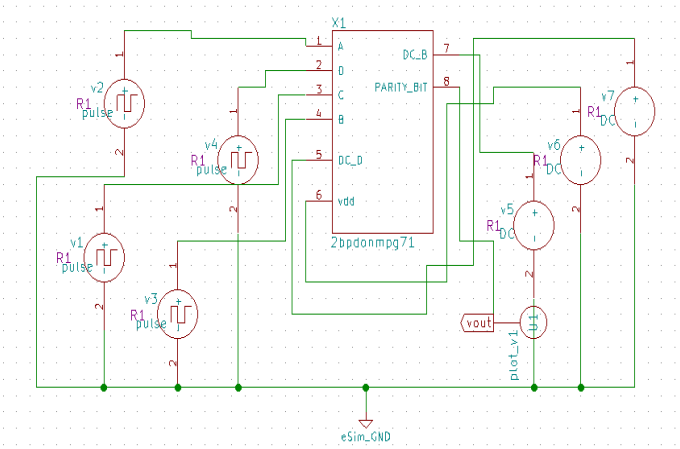

Figure 6.17: Sub-circuit

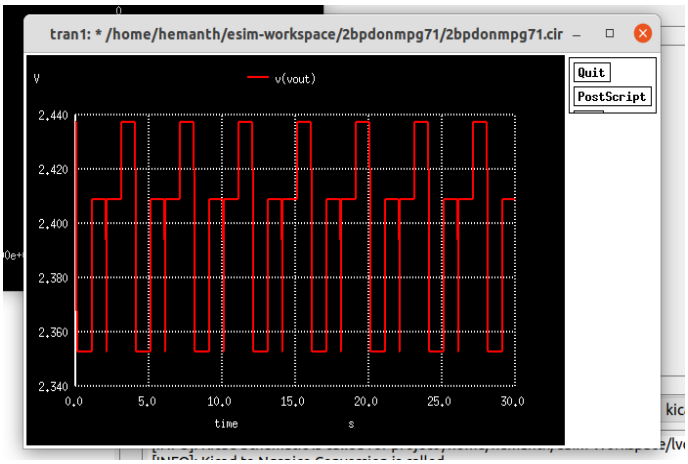

Figure 6.18: Output waveforms

6.7 A Low Power 7T SRAM cell using Supply Feedback Technique CMOS

6.7.1 Circuit details

This project proposes a novel 7T SRAM cell. In the proposed design the read and write operation have been performed separately using read and write port to enhance the data stability. Furthermore, the supply feedback transistor has been used between data storing node and cell power supply in order to increase the write ability of the SRAM cell. .The main aim of this 7T SRAM cell is to reduce the consumption of leakage power and improve the stability of the memory cell in normal region of operation. Some design architecture used CMOS transistor operation in subthreshold region for reducing power. A modified 8-T design architecture is proposed for low power and low voltage circuits. The proposed 7T SRAM cell using supply feedback concept, which comprises of 4 NMOS transistors and three PMOS transistors. Transistor PM1, PM2, NM1, and NM2 forms the latch of SRAM cell where the data has been stored, whereas NM3 acts as an access transistor during the write operation which is activated by word line (WL) signal and NM4 acts as an access transistor during read mode which basically used to separate the RBL from storing nodes Qb and Q of SRAM cell for providing disturb free read operation. The transistor PM3 acts as a feedback transistor which is connected between the power supply and storing node Q. When feedback transistor PM3 is ON state, the voltage at the drain of PM3 is slightly lower than the supply voltage. The bitline (BL) is an input line of a cell during write operation whereas RBL is input or output line during the read operation.

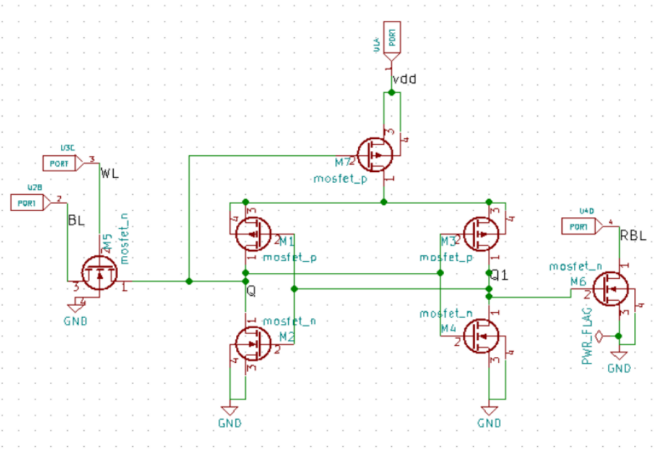

Figure 6.19: Circuit diagram

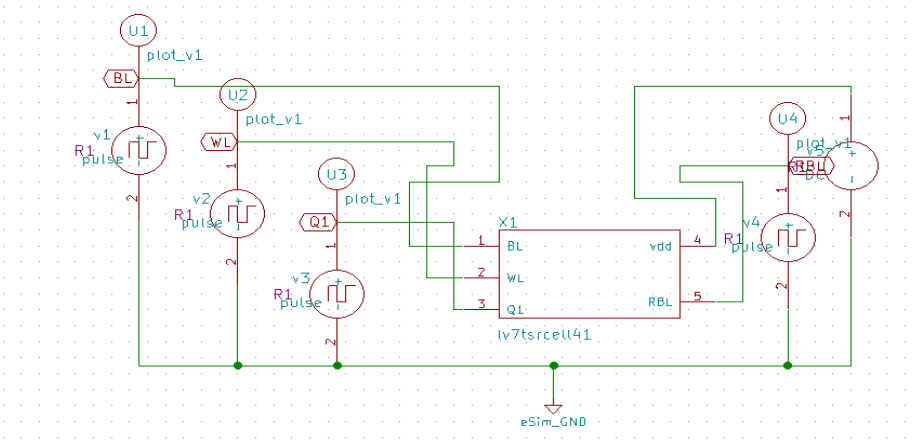

Figure 6.20: Sub-circuit

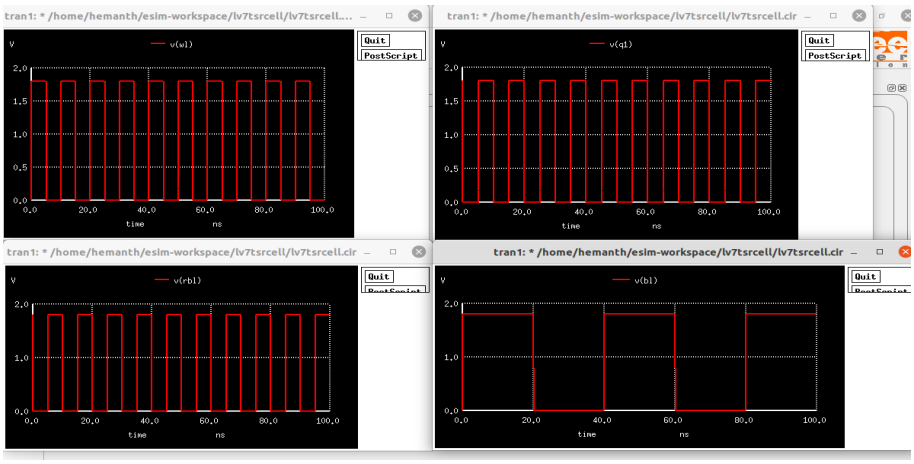

Figure 6.21: Output waveforms

6.8 Dynamic charge sharing comparator

6.8.1 Circuit details

The circuit has been designed using the practical power supply rating of 3.3 V, and the 1.8 V condition is also taken care of by providing inputs which are higher than and equal to 1.8 V. The only addition it required from the reference circuit is addition of a power flag, after ERC on eSim. The circuit is a CMOS transistor-based implementation and has two stages. The first stage being the dynamic charge sharing comparator, and the other one is the output buffer stage. The dynamic charge sharing comparator uses the circuit in the regenerative mode. In regenerative mode, the transistors operate in triode region here. The output buffer stage is self biasing differential amplifier which has differential inputs and does not have any slew rate limitations. An additional inverter is added to the output of the amplifier with the purpose of providing additional gain and to isolate the load capacitance from the amplifier. The MOSFET sizing was done heuristically by arriving at the appropriate size while keeping in mind the 0.13 um limit. The 21 MOSFET configuration consists of 7 input ports and 3 output ports, providing for a range of combinations to be fed into it, to get the required waveform. The same can be further explored but after a successful run was not pursued in this activity. The sizing is done uniformly same for PMOSFETs and for NMOSFETs. The aspect ratio is 6 to 1, with channel length capped at 0.5 um in the SPICE netlist.

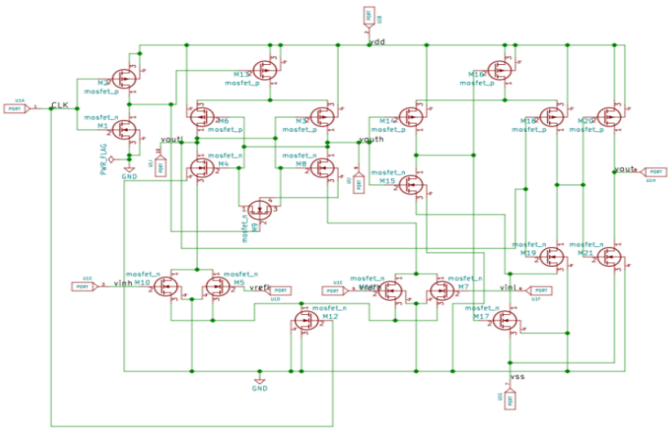

Figure 6.22: Circuit diagram

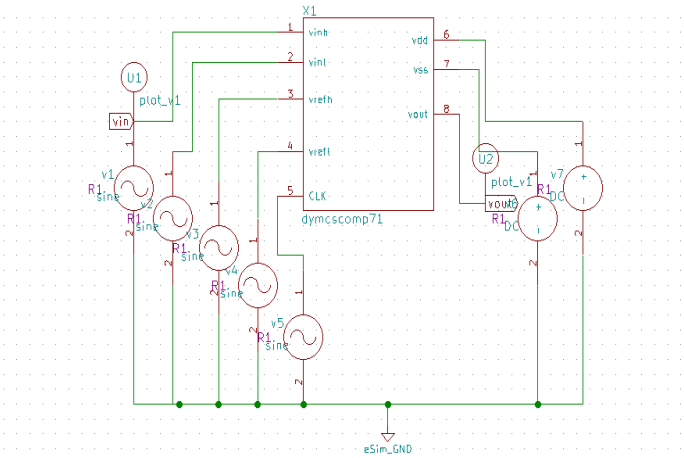

Figure 6.23: Sub-circuit

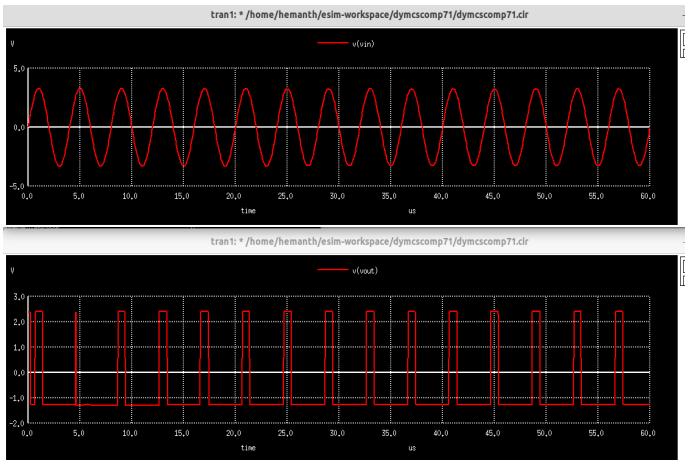

Figure 6.24: Output waveforms

6.9 1-bit NP-CMOS Dynamic Full Adder

6.9.1 Circuit details

Full adder is an inevitable element in almost all digital system designs. So one of the major steps in improving the performance of a system is to develop a better performing adder model. Generally a full adder cell is a 3 input, 2 output block, where the inputs are ith bits of the operands and carry in from the previous block. Considering the research objective, the major drawbacks to tackle were to decrease the total number of transistors as standard CMOS logic required 2N transistors to implement an N input logic, to reduce power consumption as pseudo NMOS logic had static power loss due to its constant switched on pull up network, and to ensure rail to rail swing with high noise tolerance since pass transistor logic suffered from poor voltage levels and reduced noise margins. Dynamic logic, specifically NP CMOS offered the best alternative. Dynamic logic involves two phases, namely precharge and evaluation. Initially a single PMOS precharges the output node to Vdd at CLK = 0. A pull down network receiving inputs using NMOS implements the circuit logic during the evaluation phase, that is, when CLK = 1. In the first stage, (Cout)' is computed using bridge style. This output is used in the second stage to evaluate (Sum)' using, Sum = (Cout)' . (A + B + Cin) + A.B.Cin In total, 16 transistors are needed for the implementation. The inputs should be changed in precharge phase and the results are obtained during evaluation phase.

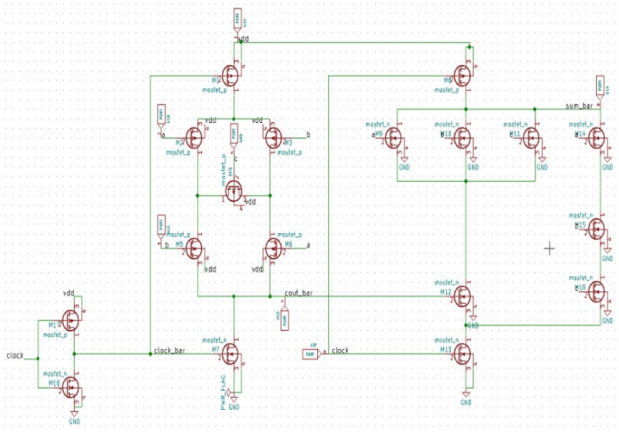

Figure 6.25: Circuit diagram

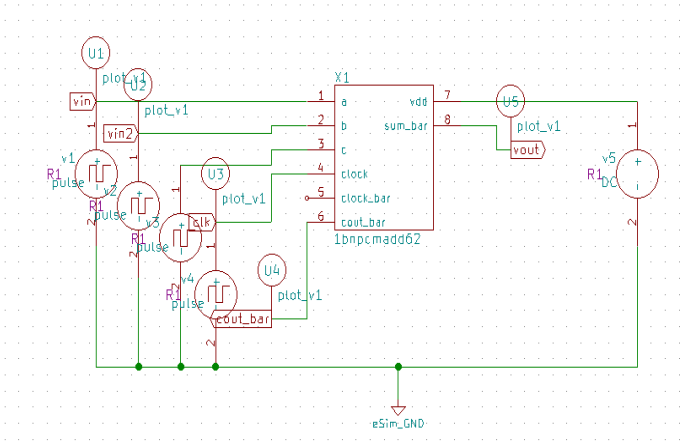

Figure 6.26: Sub-circuit

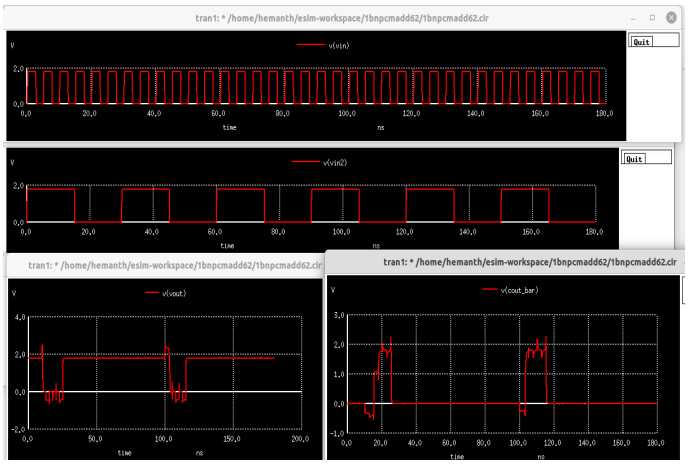

Figure 6.27: Output waveforms

6.10 FULL ADDER USING CMOS

6.10.1 Circuit details

The implementation of the FULL ADDER is done by using a sum of 28 MOSFETs of which 14 are NMOS and the other 14 are PMOS. The circuit takes in 3 inputs (A,B,C) and performs logical operations and gives out two outputs (SUM, CARRY).The dimensions of the mosfets are based on skywater 130nm pdk. The mosfet generally consist of three terminals namely source , gate and drain. For the transistor to conduct the applied gate to source voltage, Vgs must be greater than the threshold voltage, Vt. Only then a channel is formed and there will be a flow of charge in the transistor (electrons or holes) from source to drain. The gate terminal must be at positive potential with the source terminal for an NMOS to conduct and the gate must be at lower potential with source terminal in case of an PMOS . The circuit is provided with a Vdd of 3.3V and the digital inputs are of value 2.2V each (say A,B,C). The mosfets here acts like a switch whenever the digital input goes high at the gate, PMOS goes OFF and NMOS turns ON and vice versa. The inputs are delayed accordingly to match with the output waveform of the submitted file (literature survey) . Through this transistor operation the developed circuit performs logical operation of a full adder. The relations between the inputs and the outputs are expressed as: SUM = C(A+B+C)+ABC ,CARRY =AB+BC+CA.

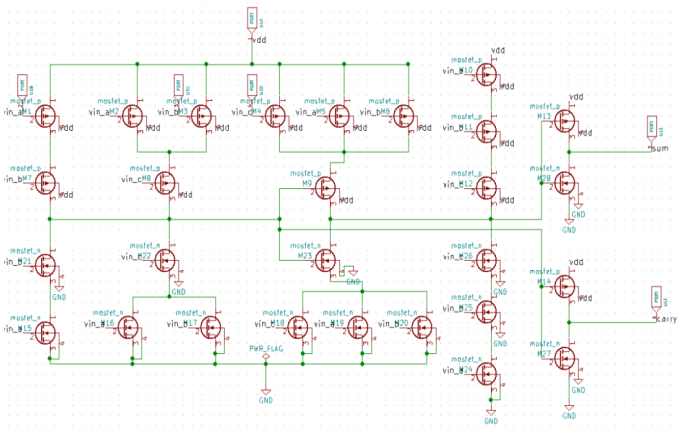

Figure 6.28: Circuit diagram

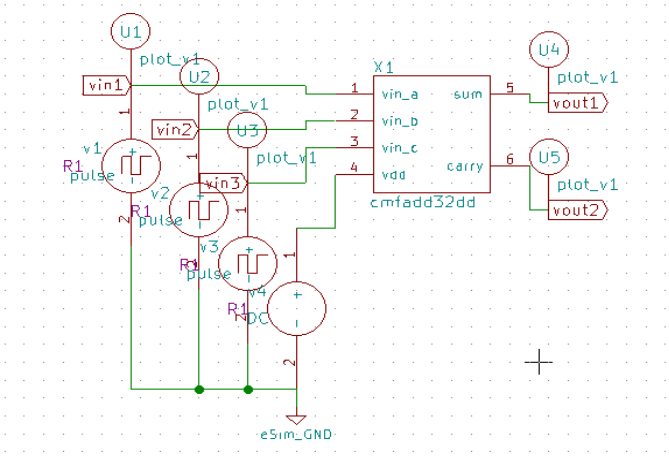

Figure 6.29: Sub-circuit

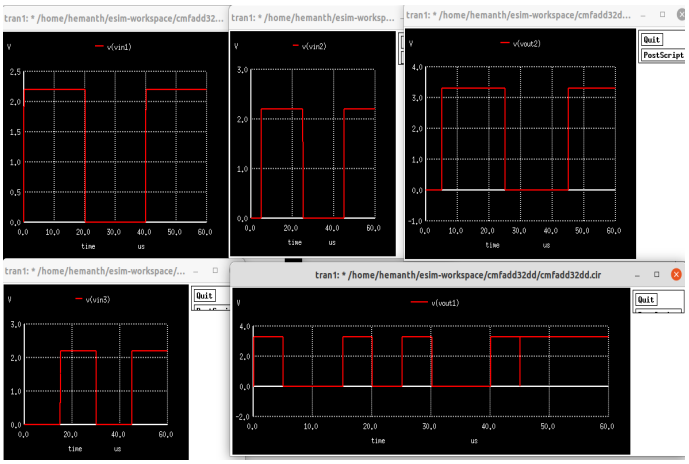

Figure 6.30: Output waveforms

6.11 Portable Mobile Charger for outdoor trips

6.11.1 Circuit details

There are 2 parts of the circuit 1) The rectification and 2) The voltage regulation. The circuit consists of a AC input source of already stepped down voltage as the step down transformer in Spice can't be modelled. The Transformer turns ratio should be calculated via the given below formula equation Np/Ns equals to Ep/Es where the Ns is the number if turns in the primary coil and the Ns is the number of turns in the secondary coil . The Ep is the voltage across the primary node and the Es is the voltage across the secondary node and the capacitance values to reduce the ripple must be calculated by the C=1/2xfxVripple , where C is the capacitor filter and the V ripple is the ripple we want to attain or desire . The output then rectified via a full wave bridge rectifier as the sub circuit where I have used Mosfet as switches instead of diodes .In this final report circuit I have not been able to implement a LM7805 as the spice net list was not included in the ESIM software, instead I used a DC 5 V to just simulate the circuit. Actually the output of the rectifier will be passed through a LM7805 voltage regulator whose output is always 5V. LM7805 is a voltage regulator which will regulate any input voltage across it input to 5 voltage but up to a certain limit so we need to absolutely sure that there is not much voltage drop across the input components of the LM7805. A Zener of 5V voltage rating will be used to protect the LM7805 and the output from getting distorted. Isolation diode is used in between rectifier and voltage regulator , here 5 V DC supply.

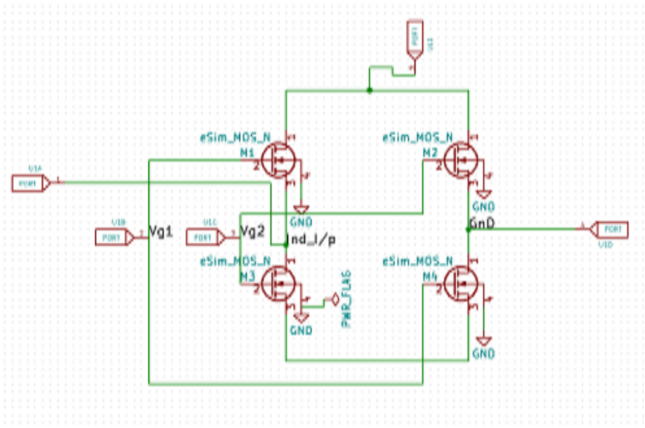

Figure 6.31: Circuit diagram

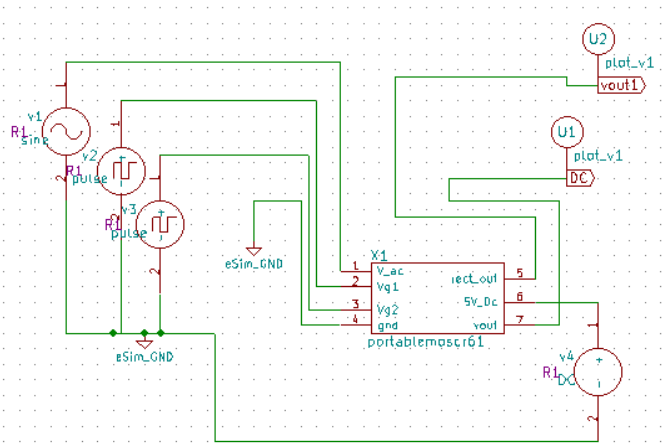

Figure 6.32: Sub-circuit

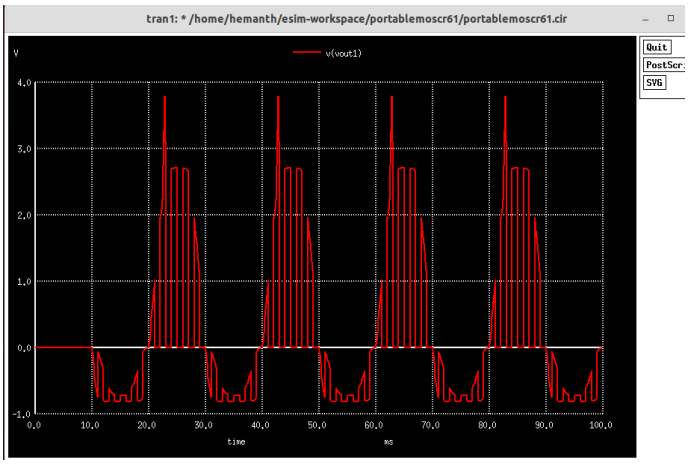

Figure 6.33: Output waveforms

6.12 NMOS Schmitt trigger SRAM

6.12.1 Circuit details

SRAM stores charge as long as it is powered. Unlike DRAM, it does not require refresh cycles, is faster albeit costlier due to higher gate density. The traditional 6T SRAM consisting of PMOS, poses critical performance degradation threat NBTI. It is observed in PMOS due crystal mismatches at the interface of metal and metal oxide interface and increases Vth (Threshold Voltage) of PMOS and reduces SNM resulting in reduced temporal performance, and potential device failure. The invertor proposed in the circuit has only NMOS. The VB boosts output of invertor from Vdd to Vdd1=Vdd+Vth (NMOS threshold voltage) to compensate the Vgs-Vth for M1 and M4 and pulls up Q and Q to Vdd during LH (Low to High) transition thus enhancing the swing of output voltage. The hysteresis VTC of ST reduces lower and raises higher threshold value for invertors, manifested as rise in SNM and faster transition as compared to 6T configuration. The circuit has 2 access transistors M9 and M10 controlled by WL (Word Line). There are 2 ST invertors who drive each other indefinitely as long as powered thus string the data. The invertors are connected to BL and BL (Bit Lines) for READ and WRITE operations through M9 and M10. The stored value is present at Q and complemented Q. To enable READ mode BL and BL are HIGH. After read destruction both BL and BL follow stored data Q and Q respectively and data stored is available at BL line. For WRITE mode, BL and BL are complementary. If new WRITE value is different to stored value, both invertors oppose the change initially and gradually change their states.

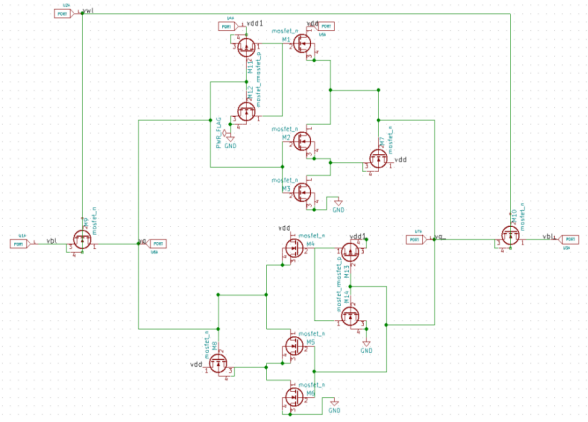

Figure 6.34: Circuit diagram

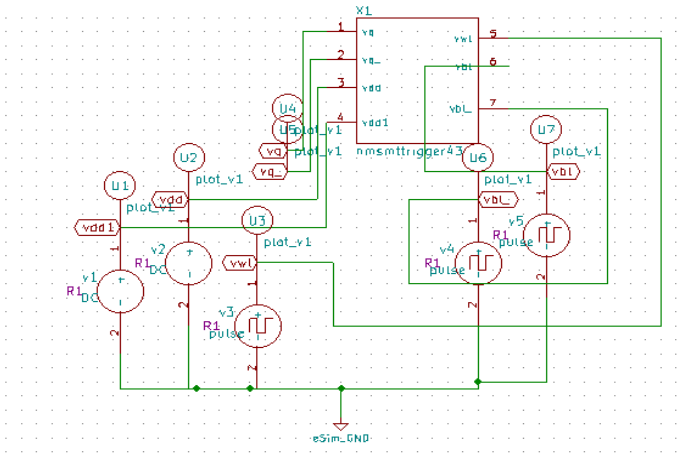

Figure 6.35: Sub-circuit

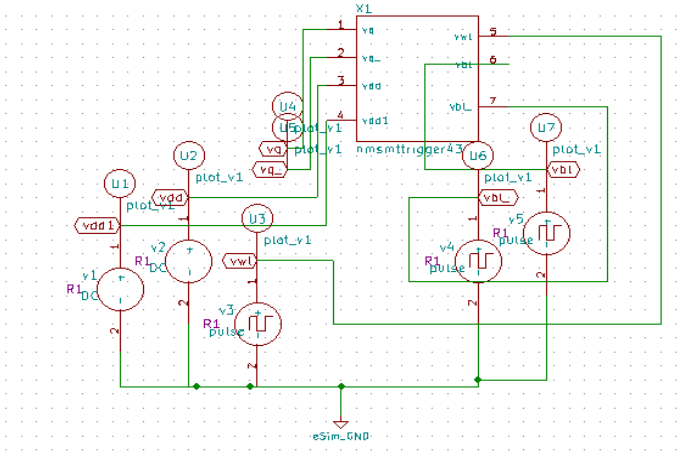

Figure 6.36: Output waveforms

6.13 3 Stage CMOS Ring Oscillator

6.13.1 Circuit details

Ring Oscillator circuit consists of 3 stages, with the presence of a feedback from the last stage to the first stage. The circuit consists of 3 CMOS inverters connected in a cascaded fashion, with the output of one connected to the next inverter. Each inverter consists of nMOS and pMOS transistor. In its basic form, the oscillation frequency mainly limited by the transit response of the pMOS transistor as the mobility of hole is two to three times lower than electron mobility in nMOS transistor. The MOSFETS used in the circuit are using the 130nm technology node. The required 130nm technology MOSFETS are acquired using the sky130-fd-pr, which consists of several models of MOSFETS, Diodes, Capacitors, Resistors etc. The circuit also has 3 capacitors which act as stray capacitance to filter out distortions in the Oscillations. Capacitor of 1 pico Farad is used. The dc source of 1.8V is used as the source voltage for the PMOS and NMOS. The plot generator is connected in the output of every stage. Transient analysis is performed from a time of 10us to 10.5us with a step of 10ns. The oscillations are achieved when the ring provides a phase shift of 2pi radians, thus each stage must provide pi/N delay, since N is equal to 3 in the circuit designed each stage provides a delay of pi/3 radians. The rest of the phase shift/delay of pi is provided by the dc inversion.

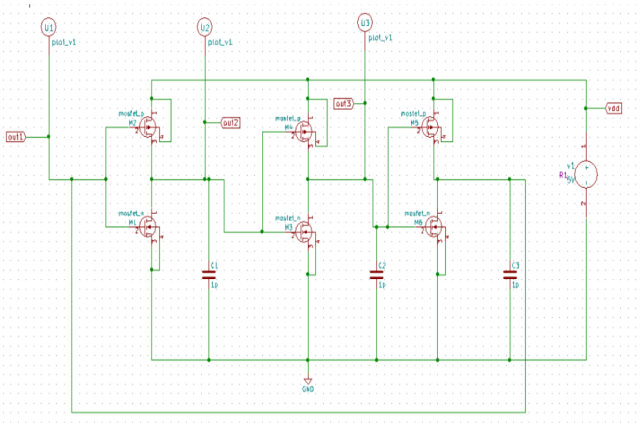

Figure 6.37: Circuit diagram

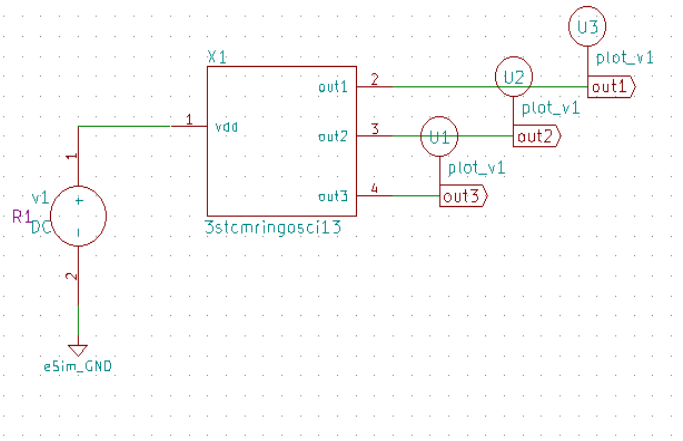

Figure 6.38: Sub-circuit

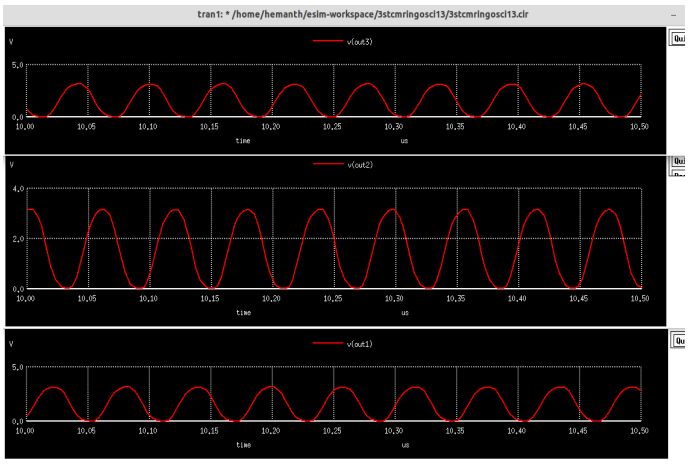

Figure 6.39: Output waveforms

6.14 CURRENT STARVED VCO TARGETING

6.14.1 Circuit details

The Current-mode analogue signal processing has led to the development of many systems based on the current-mode approach. The current mirrors are particularly useful for the distribution of bias currents in larger circuits. It is wellknown that the Wilson current mirrors have better high frequency behavior than other current mirrors. Wilson current mirror balances the two branches to avoid systematic error introduced by differences in Vds voltages is the main advantage of using it. Negative feedback is included in this circuit and will give stable output currents for wide voltage swings and enhanced output impedance. It consists of four NMOS M1, M2, M3, M4. M1 and M4 are diode connected transistor. A diode connected transistor always remains in saturation region. So, no need to provide external biasing. Negative feedback is due to negative feedback drain current and series sampling is used at output to increase output impedance. M4 is in saturation and senses the current at output side. As M2 and M4 are identical MOS with same Vgs, Same current flows in both input and output side due to feedback action. Input branch and output branch currents are taken as Iref and Iout respectively. Keeping Vdd as 1.8V and resistance as 1.123k ohms, current of 6.23uA flows at input branch. From transient analysis which was performed for 1ms, it is observed that Iref current of 6.23uA is perfectly mirrored at output branch. This Implementation of NMOS Wilson Current Mirror for 6.23uA of current was done using eSim, ngspice and SKY130 PDK.

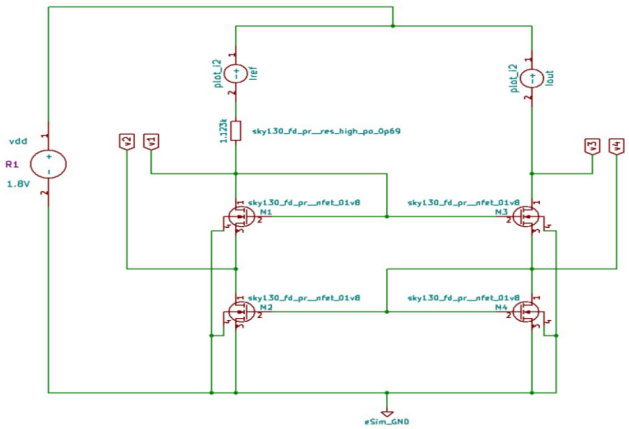

Figure 6.40: Circuit diagram

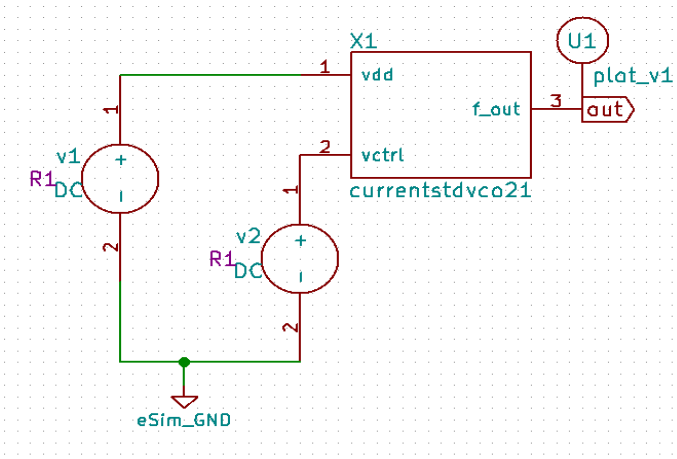

Figure 6.41: Sub-circuit

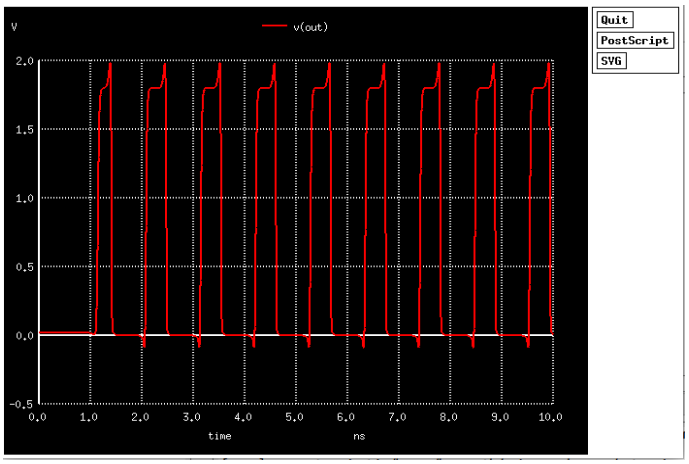

Figure 6.42: Output waveforms

6.15 4-bit Carry Lookahead Adder

6.15.1 Circuit details

Here we are designing 4-bit CLA process by using conventional static cmos. The power supply is varied from 1.0 Volts to 2.8 Volts for proposed and basic design. The proposed circuit will be implemented in eSim EDA tool and will be done using SKYWater's 130nm PDK. In circuit, basic element is NMOS and PMOS is used to made every block. Two intermediate terms, called propagate and generate bits are used to calculate sum (S) and carry out (Cout) bits. If we define two variables as carry generate Gi and carry propagate Pi then, Pi = Ai xor Bi; Gi = Ai and Bi; The sum output and carry output can be expressed as Si = Pi xor Ci; Ci + 1 = Gi or (Pi and Ci); Where Gi is a carry generate which produces the carry when both Ai, Bi are one regardless of the input carry. Pi is a carry propagate and it is associate with the propagation of carry from C1 to Ci +1 (Because input carry is already is given with Ai and Bi). I was able to reach a 4-bit ripple carry adder that has delay of 1.22 ns with 0.6 uW power consumption (measured at 10 MHz), with 200 mosfets. Every carry bit can be found from the generate and propagate terms. Once the carry-out bits have been calculated, the sums are found using the simple XOR operation. Carry Look Ahead Adder (CLA) uses direct parallel-prefix scheme for carry computation. Its time delay(T) and area complexity(A) are as follows for an n-bit CLA adder: T = (2log(n) + 4); A = ((3/2)nlog(n) + 4n + 5). And also n bit cla cost will be = 7n +(1/6)n(n+1)(n+5).

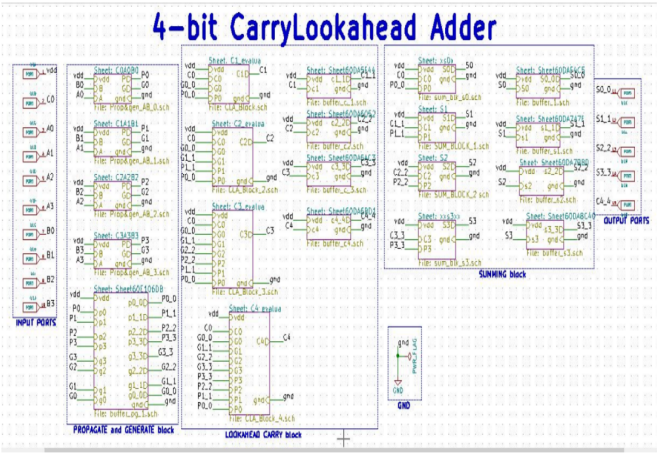

Figure 6.43: Circuit diagram

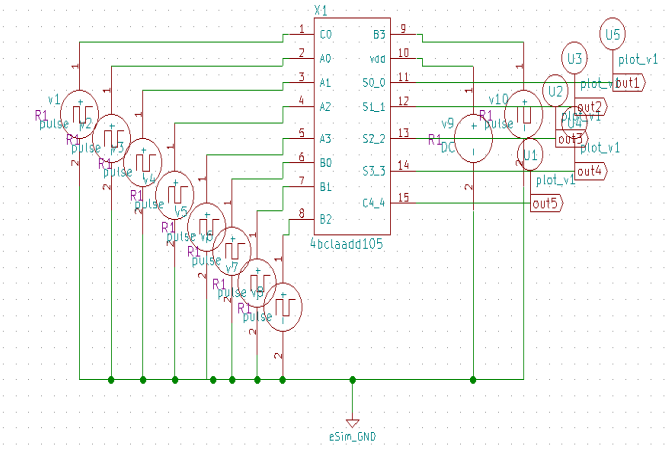

Figure 6.44: Sub-circuit

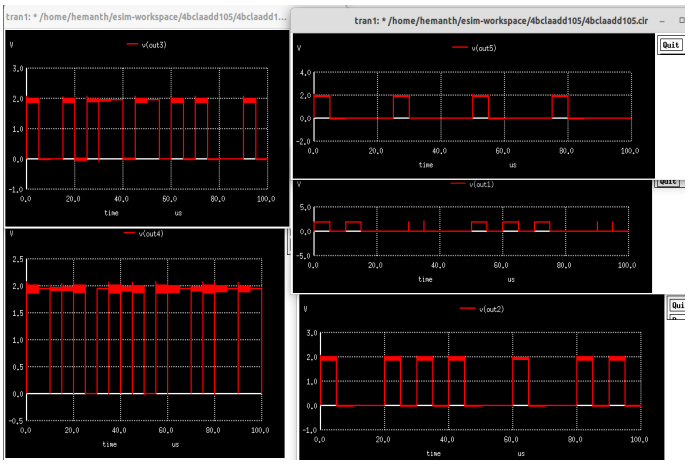

Figure 6.45: Output waveforms

6.16 Schmitt Trigger

6.16.1 Circuit details

CMOS Schmitt Trigger circuit has the switching thresholds are extensively dependent on the ratio of NMOS and PMOS. This circuit will exhibit racing phenomena after the transition starts. The three NMOS is loaded by the top PMOS circuit, the instant when output voltage Vout, is LOW, Third NMOS i.e., M5 will be OFF, hence the other two M1 and M2 NMOS run in triode mode of operation meaning the drain current is controlled by three terminals instead of two as in the saturation mode. When input voltage Vin to the terminal M1 and M2 is LOW, both the transistors operate in cut off mode. Hence both are in OFF condition. Transistors M3 and M4 are in ON condition that raise the output voltage to logic high level. When the input reaches the threshold voltage of the transistor M1, the M1 is turned on, while M2 is closed, then the high output turns on M5. Current starts to flow through M5. The node between M1and M2 is pull down by transistor M1. The on transistor M5 tries to pull up this node voltage. The transistor M2 is maintained at a high logic level output. When the input voltage exceeds the threshold M2, the output is switched to a low logic level. As a result the switching point is switched to a higher voltage, called VIH. When Vin falls from HIGH to LOW, PMOS shifts the switching point to VIL. The difference between the VIH and VIL is referred to as HYSTERESIS voltage.

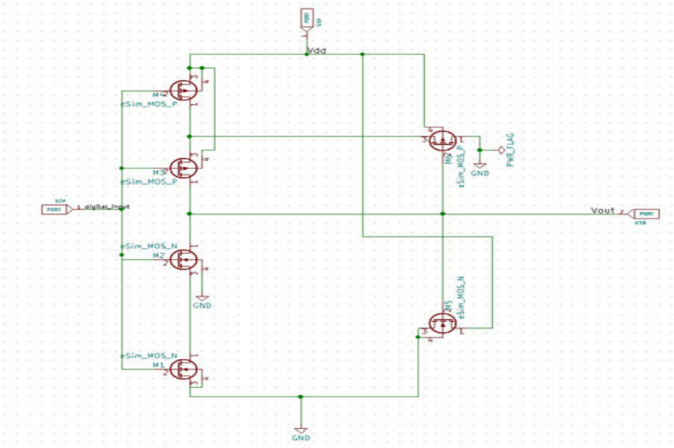

Figure 6.46: Circuit diagram

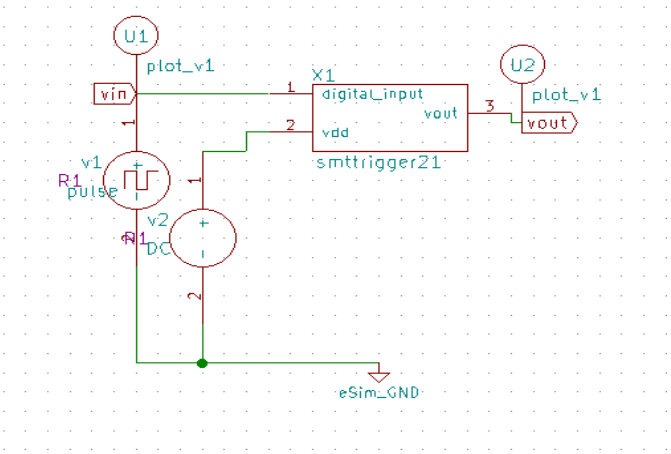

Figure 6.47: Sub-circuit

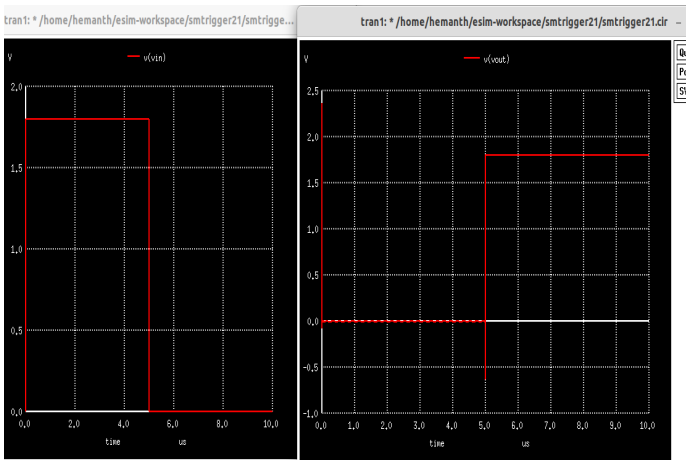

Figure 6.48: Output waveforms

6.17 8x4 right Barrel Shifter using NMOS pass transistor logic

6.17.1 Circuit details

An 8x4 right barrel shifter using NMOS pass transistors with skywater 130nm technology is designed using an integrated tool, 'eSim' with circuit schematics on KiCAD. The transistors are positioned to give right shift operation. The 8 inputs bits of shifter are In0, In1, In2, In3, In4, In5, In6, In7, the five control shift bits are S0, S1, S2, S3, S4 and output bits are Out0, Out1, Out2, Out3 respectively. The gate terminal of each NMOS transistor in a column is connected to one control shift signal as input. At a time only one control signals (from S0-S4) are enabled high while others are low. When control shift bit S0 is enabled, then the output bits are at Out0 = In0, Out1 = In1, Out2 = In2, Out3 = In3. For the next clock cycle, when S1 is enabled then the inputs bits are shifted right by one bit position. For the input bit pattern In0 = 0, In1 =1, In2 = 1, In3 = 0, In4 = 0, In5 = 0, In6 = 1, In7 = 1 and control bits as S0 = 0, S1 = 0, S2 = 1, S3 = 0, S4 = 0, output becomes Out0 = 1, Out1 = 0, Out2 = 0, Out3 = 0. For simulation purpose, the control bit S4 is enabled, the inputs bits are shifted right by 4 bit position and the output bits are at Out0 = In4, Out1 = In5, Out2 = In6, Out3 = In7. From the NgSpice output plots, the output shifted bits are observed and these are cross-validated to confirm the functionality of the circuit. The output bits suffer from threshold voltage (VTn) drop i.e. maximum output voltage level is limited to VDD - VTn which can be overcome by using transmission gates instead of pass transistors.

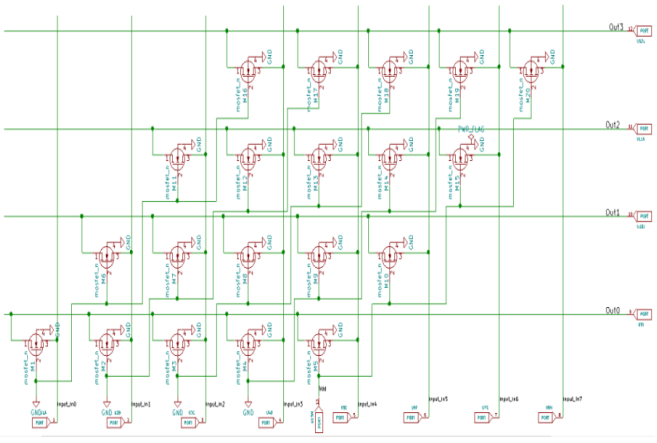

Figure 6.49: Circuit diagram

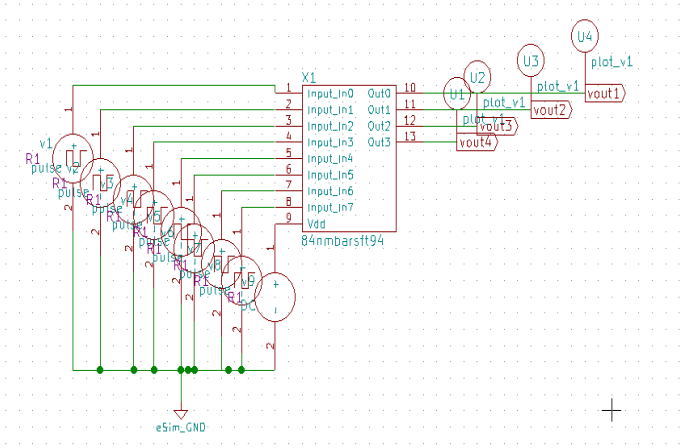

Figure 6.50: Sub-circuit

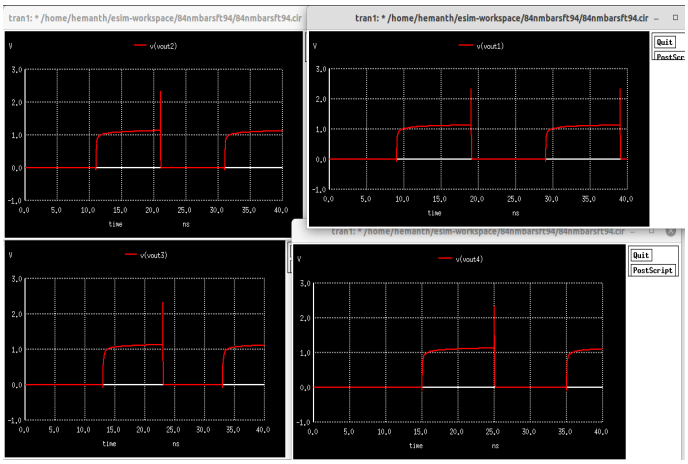

Figure 6.51: Output waveforms

6.18 Two Stage CMOS Operational Amplifier

6.18.1 Circuit details

Operational Amplifiers, Op Amps for short are play a very crucial role in the Linear Integrated Circuit Design. It can perform mathematical operations which make it "operational" amplifier, amplifier, comparators, PLLs, Integrators, Filters are few notable circuits that use Op Amp. They play a vital role in biomedical field for amplifying weak biomedical signals, which is important for gaining insights into the signal. The Operational Amplifier design is achieved through skywater 130nm technology. This circuit employs a NMOS differential amplifier M1 and M2 with two input terminals, with a PMOS load M3 and M4. This circuit is provided bias with the help of a current mirror circuit M5 and M6 provided with a constant current source. The output is taken as a single ended output and the gain of the differential amplifier thus obtained is further increased with the help of a Common Source Amplifier M7 which is also biased with the current mirror circuit of M5 and M8. The capacitors provide a stability against the poor phase margin of the circuit by trading off the fast response of the amplifier. Hence for better phase margin an external compensation is a must. The circuit employs different aspect ratio for different MOSFETs for the correct bias and operation of the circuit. The circuit provides a gain of nearly 40dB with a gain bandwidth product of 4.7MHz and about 3KHz 3dB cut off, which makes the operational amplifier circuit to amplifier a 1mV peak to peak to about 2V peak to peak thus weak signals can easily be amplified.

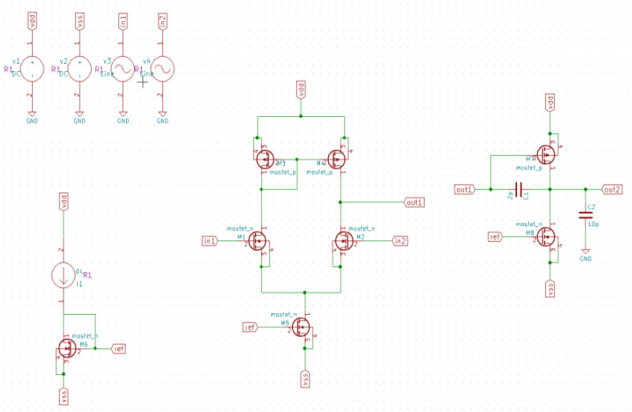

Figure 6.52: Circuit diagram

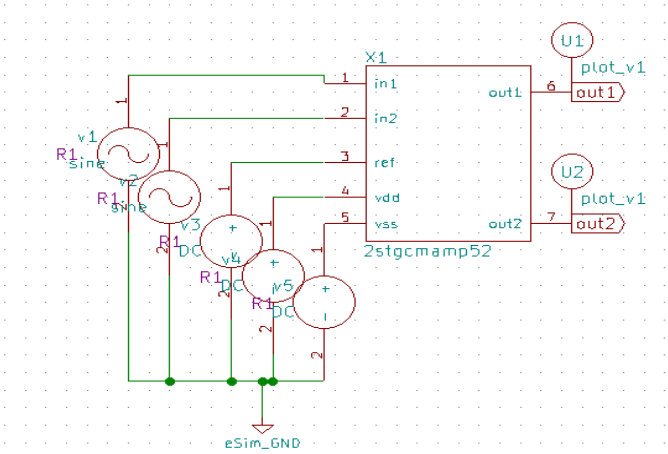

Figure 6.53: Sub-circuit

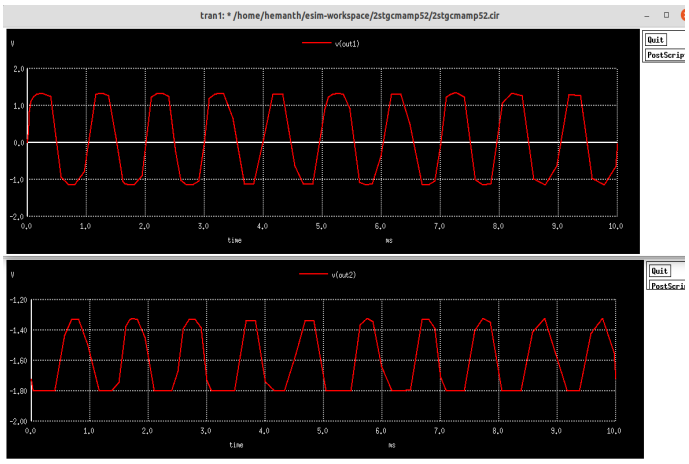

Figure 6.54: Output waveforms

6.19 Bandgap reference circuit using simple current mirror architecture

6.19.1 Circuit details

A bandgap voltage reference is a circuit which produces a constant voltage of 1.1V to 1.3V with respect to any change in temperature, supply changes of plus or minus 10 percent and process variations. A constant current is pumped into a diode, the voltage across the diode decreases with respect to increase in temperature. This is called complementary to absolute temperature, CTAT. This is obtained using pumping a constant current through a diode connected pnp or npn transistor. The slope of the CTAT voltage is around 26mV per C When the voltage difference between the two CTAT voltages is taken we get Proportional to absolute temperature, PTAT voltage. PTAT voltages varies linearly with the increase in the temperature. The slope of the PTAT is around 86uV per C. This PTAT voltage is obtained by taking the difference of the CTAT voltages produced by two independent diodes. The current from the first diode is copied using a current mirror or an operational amplifier used in negative feedback. The op amp in the negative feedback makes the voltages of non inverting terminal and inverting terminal equal and the potential difference between the two CTAT voltages is taken using a designed resistor. The CTAT and PTAT currents are being added and are being dumped into a resistor to obtain constant reference voltage. To avoid the zero biased conditions at the transient a start up circuit is designed to keep the mosfets in saturation region.

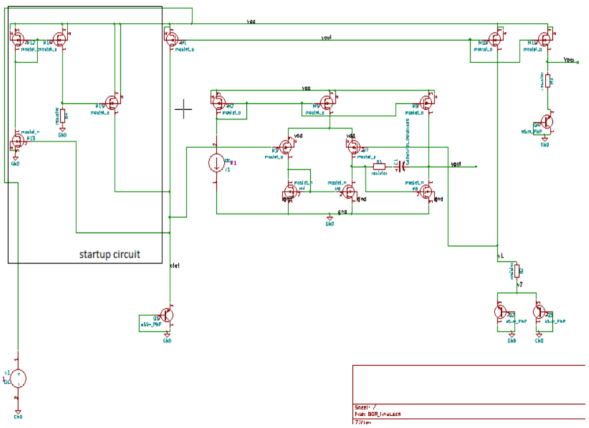

Figure 6.55: Circuit diagram

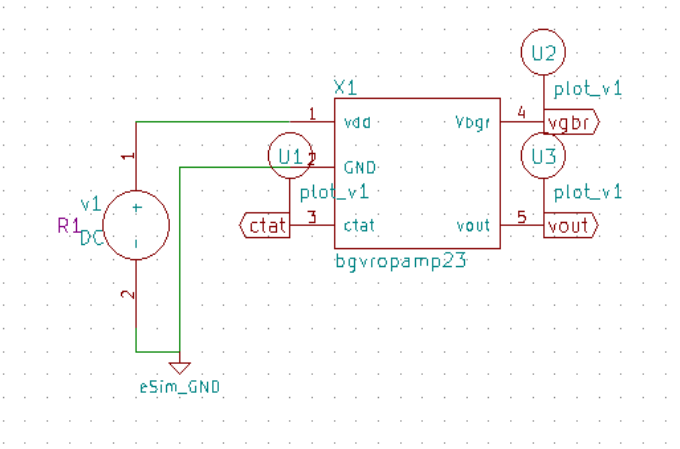

Figure 6.56: Sub-circuit

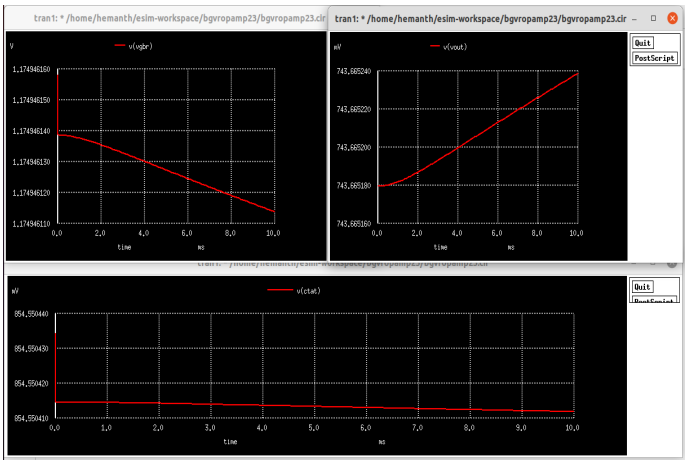

Figure 6.57: Output waveforms

6.20 Design and Analysis of DIBO Differential Amplifier

6.20.1 Circuit details

The differential amplifier is a commonly used circuit in analog design. The Differential amplifies the difference of the two input voltages by the constant differential gain Ad. If a part of the input is common to both the inputs, the differential amplifier rejects the difference. This common difference is called as common mode rejection. The design uses two input signals and hence called as dual input. It is balanced output because the output taken at both the drains are at same potential with respect to ground. Figure 1 shows the design of differential amplifier. Inputs Vin1 and Vin2 are applied to the gate of M1 and M2. These two inputs are same in magnitude and opposite in phase. The differential output is measured between the two drain of M1 and M2. Two identical registers Rd1 and Rd2 are connected to drain of MOSFETs used as load puts the transistor in saturation. The design is simulated in esim using 130nm skywater technology. This technology is developed by Cypress semiconductor. It is open source a foundry technology. Design: The design of MOSFET differential amplifier is as shown in below equations Given Rd1=Rd2=25Kohms, VDD=5V, VSS=-5V, VTN1=VTN2=1V, kn1=kn2=50uA/Vsquare. By DC Analysis VGSQ=VSS-2IdqRs Idq=kn(VGSQVTN) square Substituting and Solving the above two equation VGSQ=2.186v=VGSQ1=VGSQ2 ID=70.33uA gm=2kn(VGSVTN)=0.1186uA Differential gain Ad=gm RD =2.965 Figure 2 shows the differential amplifier designed for gain of 2.965 is achieved.

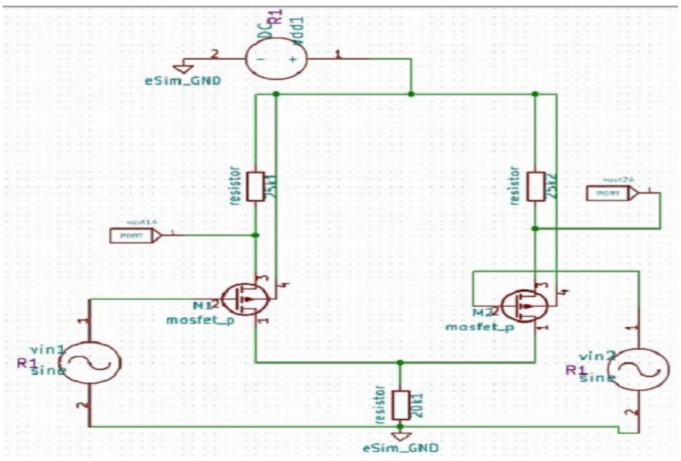

Figure 6.58: Circuit diagram

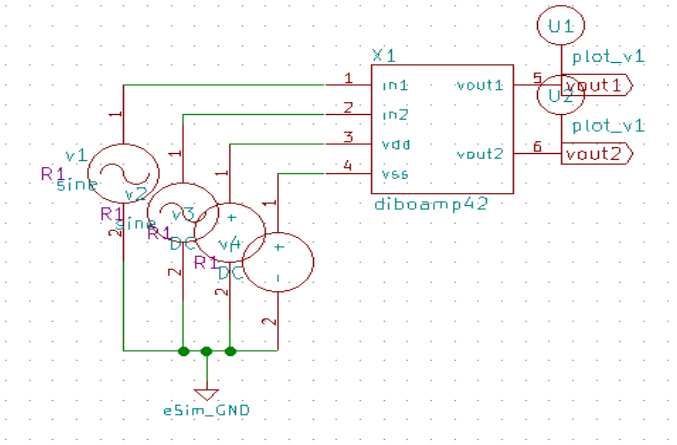

Figure 6.59: Sub-circuit

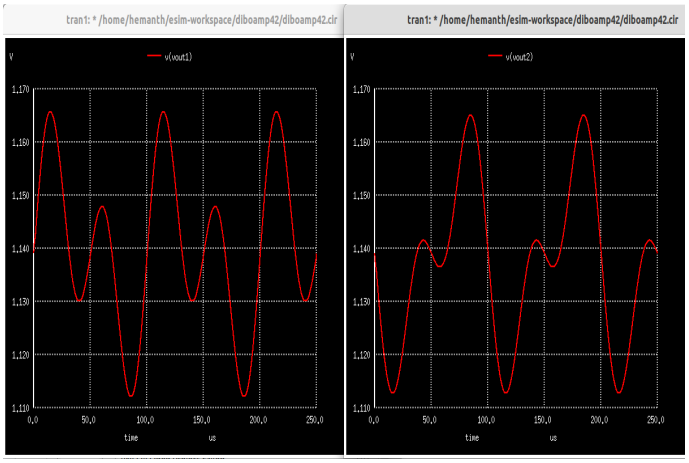

Figure 6.60: Output waveforms

6.21 Phase Frequency Detector for Phase locked loops

6.21.1 Circuit details

A phase locked loop or PLL in short, is a negative feedback system containing a voltage controlled oscillator and a phase comparator connected such that the oscillator maintains a constant phase angle relative to a reference input signal. PLL can be used to generate stable high frequency signals as output from a fixed low frequency input signal. Such circuits are used in many SoC based systems and are used to clock the microcontrollers and microprocessors by generating a clock signal with precise frequency. A typical PLL uses a phase frequency detector circuit to get a measure of error between the input signal and required signal i.e. it is used to compare the signal from the feedback loop with the input signal. The circuit is idealized when the inputs are frequency locked and phase locked. Two inputs are given to the circuit. Consider a case when an input is higher in frequency than the other. The flip flops are set and reset accordingly. This causes one of the two outputs to spend more of its time in high state than the other. Such behaviour will be carried forward in the PLL to correct the output and to minimize the variation in frequencies. The corresponding reference circuit features a phase frequency detector. Each of the two D flip flops and the AND gate will be implemented using CMOS logic in SkyWater 130nm PDK technology.

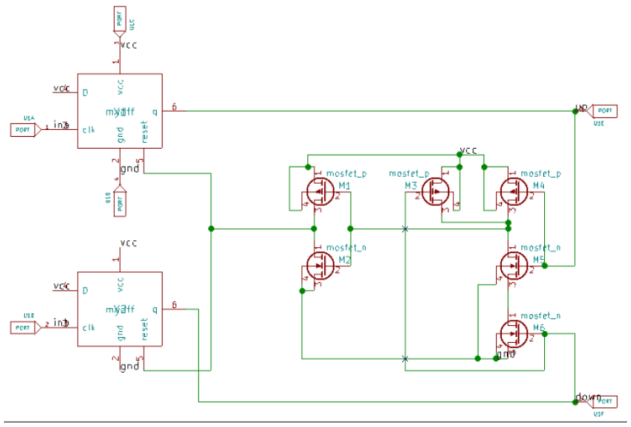

Figure 6.61: Circuit diagram

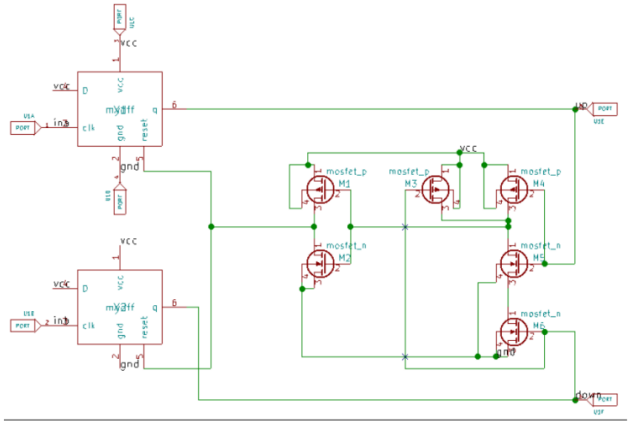

Figure 6.62: Sub-circuit

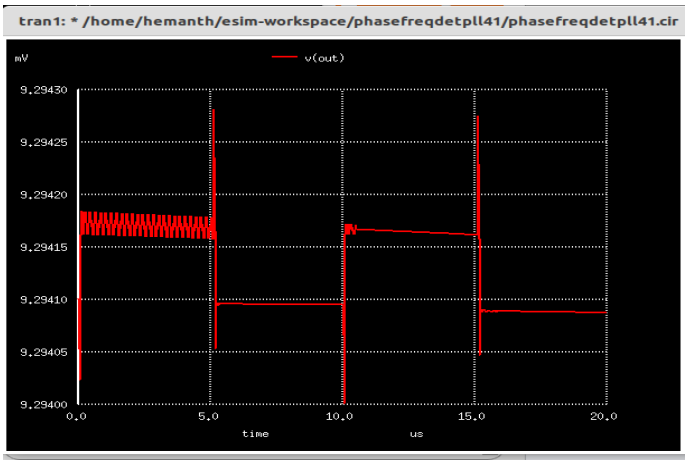

Figure 6.63: Output waveforms

6.22 3-bit resistor string DAC

6.22.1 Circuit details

The 3 bit Digital to Analog converter was implemented in three blocks: a resistor string network, an 8 to 1 multiplexer and a control signals generator block. The resistor string had 8, which is 2 raised to the power 3, equal resistors between Vrefh and Vrefl. The control signals generator block was there to pass the three input bits and their complements to act as select lines for the multiplexer. D Flip Flops which contain CMOS inverters and Transmission gates within them were built for this purpose, and three of them, one for each digital input bit were used. DFFs need both a clock signal and its complement. To obtain the complement, the clock signal was passed through a CMOS inverter. Since this causes an additional delay, the regular clock was sent through a Transmission gate to equalise the delays. Instead of the traditional method of implementing a network of switches in a digital to analog converter, an 8 to 1 multiplexer was used, which was built by using 7 units of 2 to 1 multiplexers. 2 to 1 multiplexers were built using the transmission gates design. The inputs to the 8 to 1 multiplexer were the intermediate voltages from the resistor string and the select lines were the three digital input bits from DFFs in the control signals generator block. The output generated by the 8 to 1 multiplexer is the final analog output.

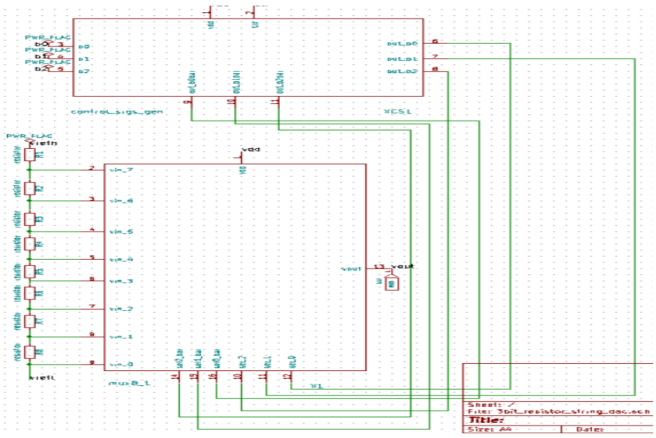

Figure 6.64: Circuit diagram

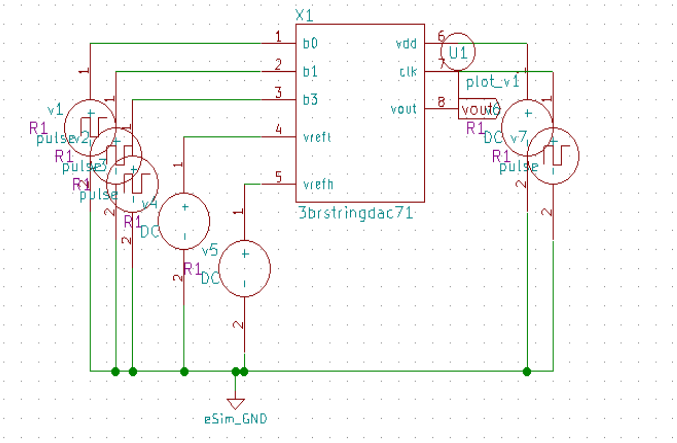

Figure 6.65: Sub-circuit

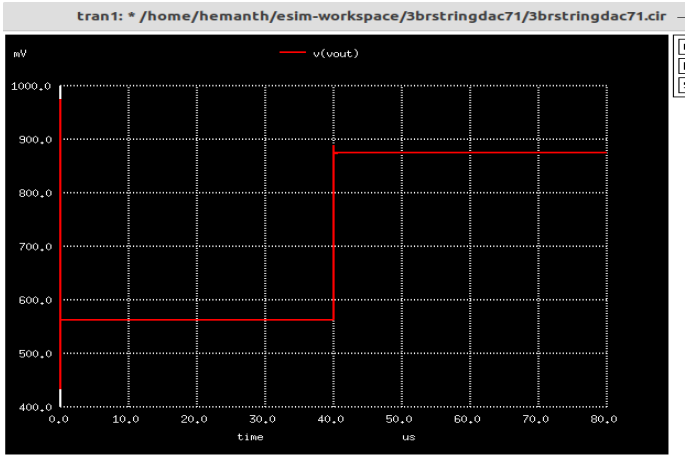

Figure 6.66: Output waveforms

6.23 Single Stage Operational Amplifier Using CMOS

6.23.1 Circuit details

To design a CMOS single stage op-amp there is a need to consider the following specifications. 1.It should produce an output signal with high gain (in db) 2.And also operational bandwidth for circuit with respect to gain(Gain Bandwidth product). 3.High Slew rate that is how fast output changes with respect to input. 4.Input Common Mode Range(ICMR) the range of common mode signal for which the amplifier's operation remains linear. 5.Common Mode Rejection Ratio(CMRR) is the ratio of the differential voltage amplification to the common-mode voltage amplification. ideally the ratio is infinite. —-¿ Designed single stage op-amp have following design specifications 1.Process specifications(V(Threshold),K' etc.) 2.Load Capacitance of 3E-19 3.differential Gain of 40db 4.Gain bandwidth 80000 Hz 5.Slew Rate greater than equal to 5 V/usec 6.ICMR (+) of 1.6v and ICMR(-) of 0.8v 7.CMRR 80db 7.Process using 130nm —-¿ From circuit 1.Current mirrors are used in design process 2.All mosfets are working in saturation mode 3.dc current from current source is found using slew rate. 4.dimensions i.e w/l ratios of mosfets m3 and m5 are same and are found using ICMR(+) 5.dimensions of mosfets m2 and m6 are same and found using Gain Bandwidth 6.dimension of mosfet m1 is found using ICMR(-) 7. all w/l ratios ,w and l are found, L should be less than twice of 130nm and in all ratios w is greater than L.

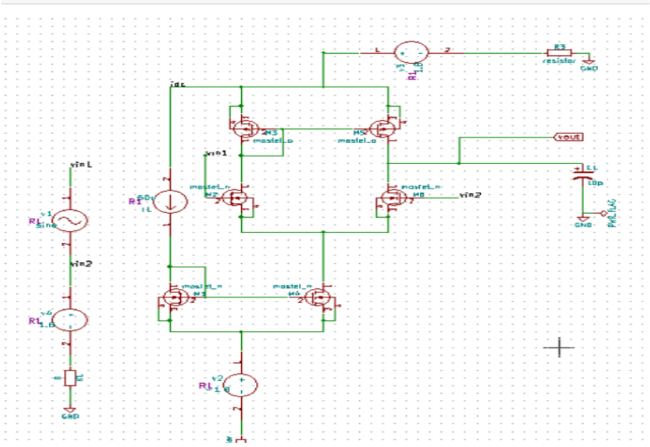

Figure 6.67: Circuit diagram

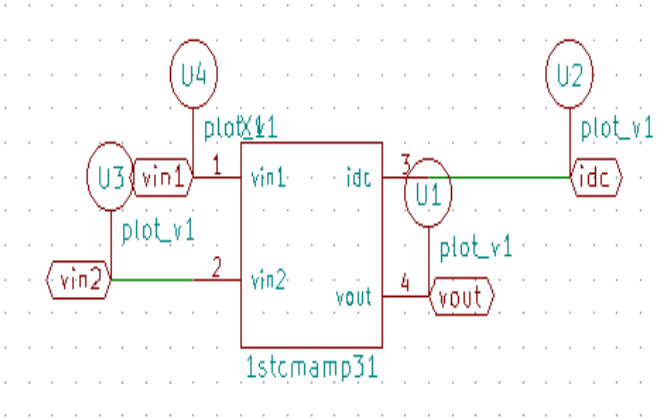

Figure 6.68: Sub-circuit

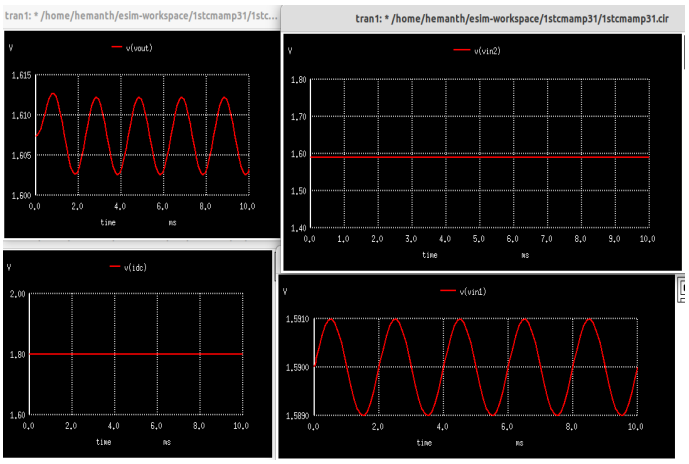

Figure 6.69: Output waveforms

6.24 Low Power SRAM Cell

6.24.1 Circuit details

The MTCMOS SRAM circuit consists of a conventional 6T SRAM cell along with two sleep transistors which have a higher threshold voltage. These sleep transistors are controlled by two signals, CLK, and nCLK, which is the complement of CLK. A subcircuit for CMOS inverter is constructed using a PMOS and an NMOS. This subcircuit is used to invert the CLK signal to form nCLK. When CLK is high, the transistors are on, connecting the virtual power rails to the physical power rails. In this mode, any read or write operation can be done. But when CLK is low, the sleep transistors are turned off. Now the virtual rails are powered by the data present in the SRAM cell through the pass transistors of the corresponding inverters. In this mode no operation can be performed to the SRAM cell, and it only retains the data. For read and write operations the signals, word line WL, bit line BL and complement of bit line nBL are used. When CLK and WL are high the read and write operations can be performed. To prevent loss of data, it has been made sure that WL is never high when CLK is low. In the sleep state, the charge in the SRAM cell can leak out slowly since it is not connected to the power supply. So the sleep transistors have to be turned back on before the charge can leak and change the state of the SRAM. Hence the frequency of CLK has been chosen accordingly. The sleep transistors are given a higher threshold voltage so that the leakage would be less and more power would be conserved. The threshold voltage is increased by applying a substrate bias voltage to the sleep transistors.

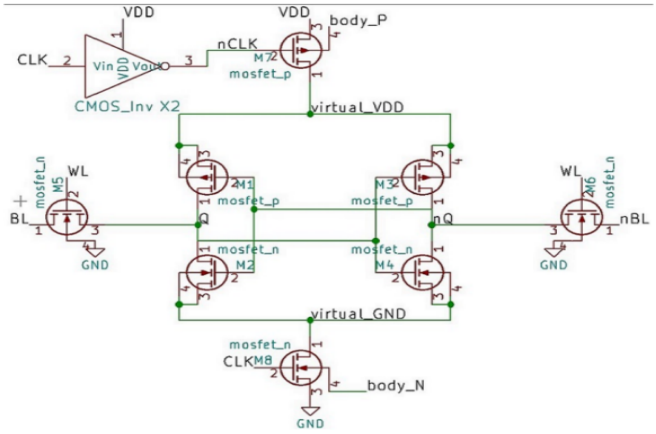

Figure 6.70: Circuit diagram

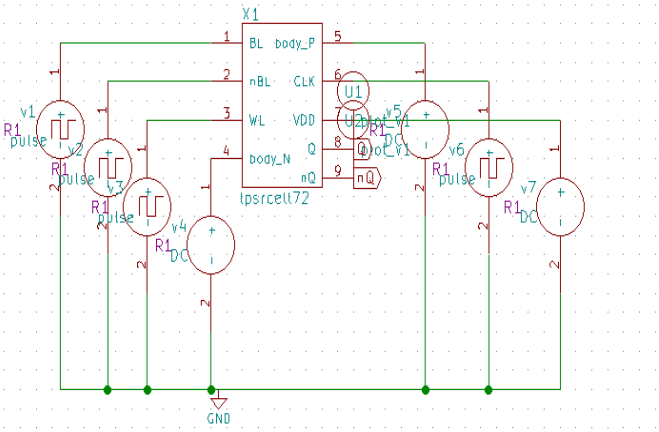

Figure 6.71: Sub-circuit

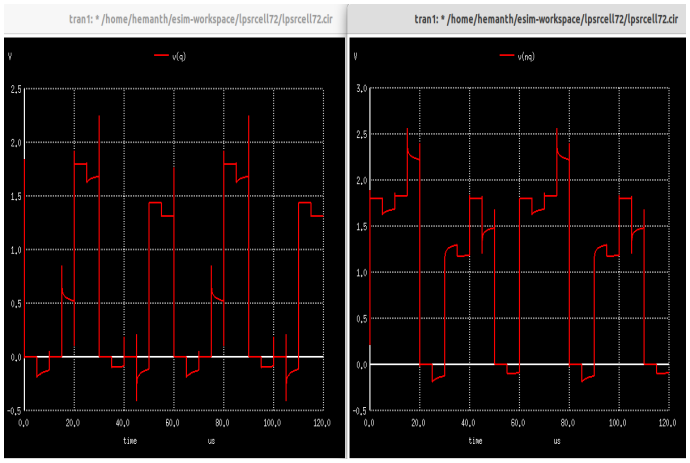

Figure 6.72: Output waveforms

Bibliography

[1] eSim Official website. 2021.
URL: https://esim.fossee.in/

[2] Ngspice Manual
URL: https://ngspice.sourceforge.net/docs/ngspice-31-manual.pdf

[3] eSim Marathon Completed circuits URL: https://esim.fossee.in/mixed-signal-design marathon/download/completed-circuit

[4] eSim User Manual
URL: https://esim.fossee.in/resource/book/esimusermanual.pdf

[5] eSim Spoken Tutorials
URL: https://spoken-tutorial.org/tutorial-search/?search_foss=eSim&search_language=English