FSM in ASIC with RF transmitter using eSim

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***Abstract*—Finite State Machine (FSM) in Application Specific Integrated Circuit (ASIC) is highly efficient in terms of computation and power. In this project I want to implement Smart Garden using FSM written in Verilog with wireless interface for remote monitoring. The circuit will be composed of System on a chip, opto-relay, sensors, flash, timer and display. The emphasis of the project is to design a mixed signal circuit. That is the FSM for design a digital circuit written in Verilog and Rf transmitter for the analog circuit.**

Keywords—FSM, ASIC, SOC, Rf transmitter, mixed

I. Circuit Details

SoC will be composed of FSM, ADC, DAC, I2C, SPI, CAN, RAM, UART and the RF block. I2C, SPI, CAN and ADC will be connected to sensors. DAC will be connected to LED light to control its power. Sensors reading will be recorded every minute and send to remote PC wirelessly via UART every hour. Digital output will be connected to opto-relay to control valves for irrigation.

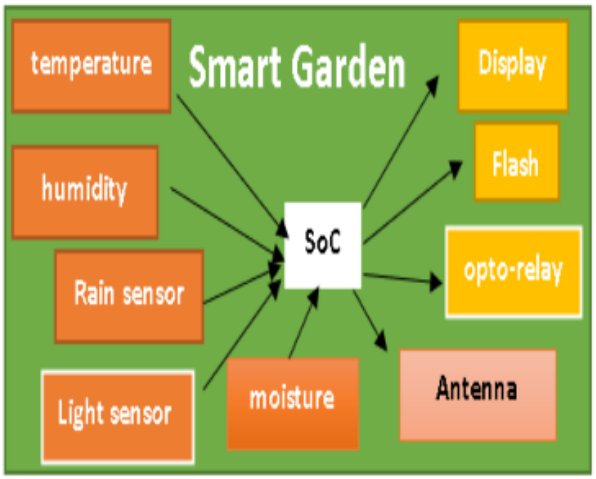

Figure 1: Smart Garden Circuit

The sensors are the temperature sensor, humidity sensor, rain sensor, light sensor, and moisture sensor. Each of which has its own interface like CAN, SPI, I2C and some are analog. RF block will be connected to antenna. Opto-relay will be connected to digital output of SoC. The LED display will be connected to DAC block..

II. Reference Circuit

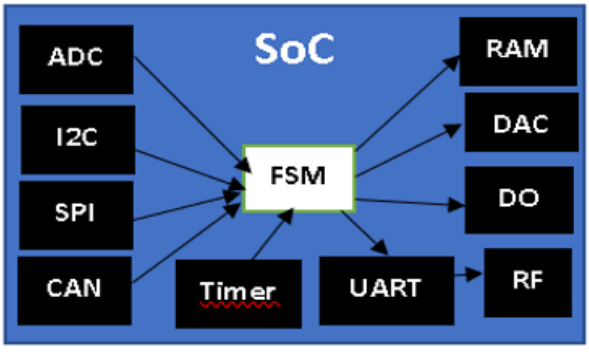

Figure 2: System on a Chip

The circuit shown in Figure 2 is composed of digital block that is premade in eSim except for FSM block which will be design using Verilog and the RF block the analog block.

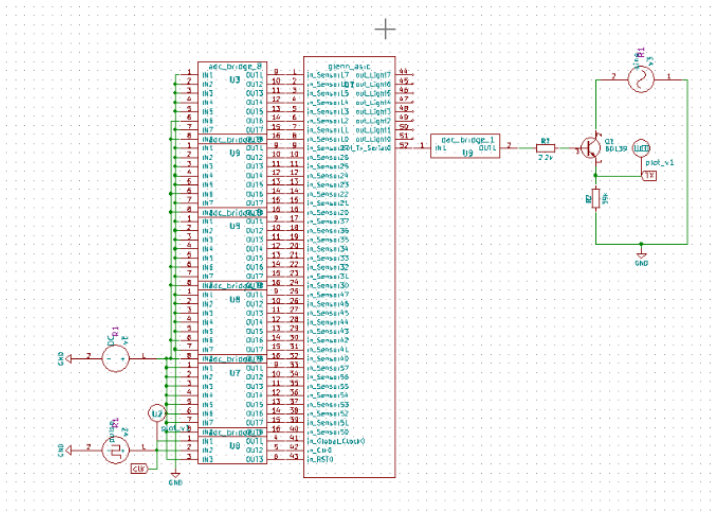

Figure 3: ASK transmitter circuit

The circuit above is the implementation of rf transmitter using amplitude shift keying modulation.

III. Reference Waveform

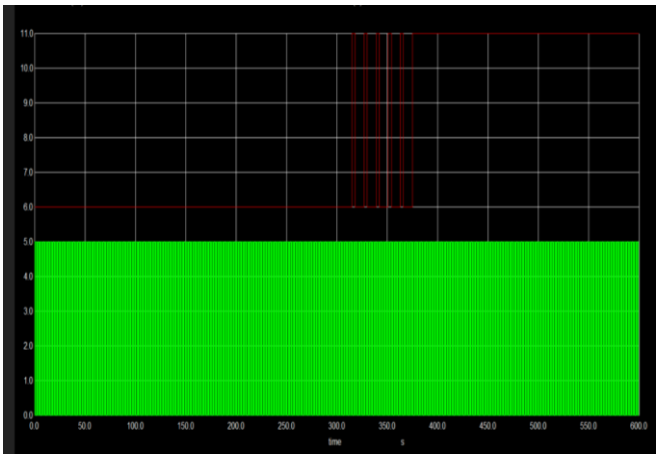

Figure 4: Reference waveform simulation using Multisi.

References

[1] Generation of ASK signal using multisim software | Amplitude shift keying | Acts of Facts..
https://www.youtube.com/watch?v=TrqzPw1Ad5s.

[1] How to write FSM in Verilog?
https://www.asic-world.com/tidbits/verilog_fsm.html