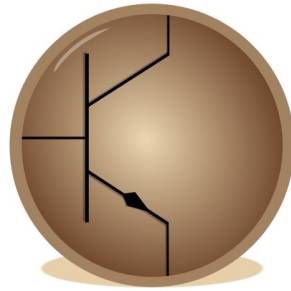


eSim

An open source EDA tool for circuit design,
simulation, analysis and PCB design



eSim User Manual

version 1.1.3

Prepared By:

eSim Team

FOSSEE at IIT, Bombay



Indian Institute of Technology Bombay



Dec 2019

Contents

1	Introduction	1
2	Architecture of eSim	3
2.1	Modules used in eSim	3
2.1.1	Eeschema	3
2.1.2	CvPcb	4
2.1.3	Pcbnew	4
2.1.4	KiCad to Ngspice converter	5
2.1.5	Model Builder	6
2.1.6	Subcircuit Builder	6
2.1.7	Ngspice	6
2.1.8	NGHDL	6
2.1.9	OpenModelica	6
2.2	Work flow of eSim	6
3	Installing eSim	9
3.1	eSim installation in Ubuntu	9
3.2	eSim installation in Windows	9
4	Getting Started	10
4.1	How to launch eSim in Ubuntu?	10
4.2	eSim User Interface	11
4.2.1	Toolbar	11
4.2.2	Menubar	15
4.2.3	Project Explorer	15
4.2.4	Dockarea	15
4.2.5	Console Area	16
5	Schematic Creation	17
5.1	Familiarizing the Schematic Editor interface	17
5.1.1	Top menu bar	17

5.1.2	Top toolbar	19
5.1.3	Toolbar on the right	20
5.1.4	Toolbar on the left	21
5.1.5	Hotkeys	21
5.2	eSim component libraries	22
5.3	Schematic creation for simulation	23
5.3.1	Selection and placement of components	23
5.3.2	Wiring the circuit	25
5.3.3	Assigning values to components	26
5.3.4	Annotation and ERC	26
5.3.5	Netlist generation	26
5.4	Tools for creating the PCB layout	27
5.4.1	FootPrint Editor	28
5.4.2	PCB Layout	28
6	Simulation	29
6.1	Kicad to Ngspice Conversion	29
6.1.1	Analysis	29
6.1.2	Source Details	30
6.1.3	Ngspice Model	30
6.1.4	Device Modelling	31
6.1.5	Sub Circuit	32
6.2	Simulating the schematic	33
6.2.1	Simulation	33
6.2.2	Multimeter	34
7	Model Editor	36
7.1	Creating New Model Library	36
7.2	Editing Current Model Library	38
7.3	Uploading external .lib file to eSim repository	39
8	SubCircuit Builder	40
8.1	Creating a SubCircuit	40
8.2	Edit a Subcircuit	45
9	NGHDL-Mixed mode simulation	46
9.1	Introduction	46
9.2	Digital Model creation using NGHDL	47
9.3	Schematic Creation	49

10	OpenModelica	57
10.1	Introduction	57
10.1.1	OMEdit	57
10.1.2	OMOptim	57
10.2	OpenModelica in eSim	58
10.2.1	OM Optimisation	59
11	Solved Examples	65
11.1	Solved Examples	65
11.1.1	Basic RC Circuit	65
11.1.2	Half Wave Rectifier	72
11.1.3	Inverting Amplifier	75
11.1.4	Half Adder	79
11.1.5	Full Wave Rectifier using SCR	82
11.1.6	Oscillator Circuit	86
11.1.7	Characteristics of BJT in Common Base Configuration	89
12	PCB Design	93
12.1	Schematic creation for PCB design	93
12.1.1	Removing components required for simulation from the schematic	93
12.1.2	Mapping of components using Cvpcb	94
12.1.3	Familiarising with Cvpcb Window	94
12.1.4	Viewing footprints in 2D and 3D	96
12.1.5	Mapping of components in the circuit	96
12.1.6	Netlist generation for PCB	98
12.2	Creation of PCB layout	99
12.2.1	Launching Pcbnew	99
12.2.2	Familiarizing the Layout Editor tool	99
12.2.3	Hotkeys	100
12.2.4	Designing PCB layout for 7805VoltageRegulator circuit	101
13	Appendix	110
13.1	Appendix A	110
13.1.1	A.1: Pin types in KiCad	110
13.1.2	A.2: ERC Table	111
13.2	Appendix B	112
13.2.1	B.1: Shortcut keys in Schematic editor	112
13.2.2	B.2: Shortcut keys in PCB editor	112
13.3	Appendix C: ERC errors	113
13.4	Appendix D: Checks to be done before Simulation in NGHDL	114
13.5	Appendix E: Common Errors in NGHDL	116

13.5.1	NGHDL Upload Errors	116
13.5.2	Simulation Related Errors	116
13.5.3	Model Deletion	118

Chapter 1

Introduction

Electronic systems are an integral part of human life. They have simplified our lives to a great extent. Starting from small systems made of a few discrete components to the present day integrated circuits (ICs) with millions of logic gates, electronic systems have undergone a sea change. As a result, design of electronic systems too have become extremely difficult and time consuming. Thanks to a host of computer aided design tools, we have been able to come up with quick and efficient designs. These are called **Electronic Design Automation** or EDA tools.

Let us see the steps involved in EDA. In the first stage, the specifications of the system are laid out. These specifications are then converted to a design. The design could be in the form of a circuit schematic, logical description using an HDL language, etc. The design is then simulated and re-designed, if needed, to achieve the desired results. Once simulation achieves the specifications, the design is either converted to a PCB, a chip layout, or ported to an FPGA. The final product is again tested for specifications. The whole cycle is repeated until desired results are obtained

A person who builds an electronic system has to first design the circuit, produce a virtual representation of it through a schematic for easy comprehension, simulate it and finally convert it into a Printed Circuit Board (PCB). There are various tools available that will help us do this. Some of the popular EDA tools are those of **Cadence**, **Synopsys**, **Mentor Graphics** and **Xilinx**. Although these are fairly comprehensive and high end, their licenses are expensive, being proprietary.

There are some free and open source EDA tools like **gEDA**, **KiCad** and **Ngspice**. The main drawback of these open source tools is that they are not comprehensive. Some of them are capable of PCB design (e.g. **KiCad**) while some of them are capable of performing simulations (e.g. **gEDA**). To the best of our knowledge, there is no open source software that can perform circuit design, simulation and layout design together. **eSim** is capable of doing all of the above.

eSim is a free and open source EDA tool. It is an acronym for **Electronics Simulation**. **eSim** is created using open source software packages, such as **KiCad**, **Ngspice** and

Python. Using eSim, one can create circuit schematics, perform simulations and design PCB layouts. It can create or edit new device models, and create or edit subcircuits for simulation.

Because of these reasons, eSim is expected to be useful for students, teachers and other professionals who would want to study and/or design electronic systems. eSim is also useful for entrepreneurs and small scale enterprises who do not have the capability to invest in heavily priced proprietary tools.

This book introduces eSim to the reader and illustrates all the features of eSim with examples. The software architecture of eSim is presented in Chapter 2 while Chapter 3 gives the user step by step instructions to install eSim on a typical computer system. Chapter 4 gets the user started with eSim. It takes them through a tour of eSim with the help of a simple RC circuit example. Chapter 5 illustrates how to create the circuit schematic in esim and Chapter 6 explains simulating the circuit schematic. The advanced features of eSim such as Model Builder and Sub circuit Builder are covered in Chapter 7 and Chapter 8 respectively. Additional features in eSim like mixed mode simulation and OpenModelica are covered in Chapter 9 and Chapter 10 respectively. Chapter 11 illustrates how to use eSim for solving circuit simulation problems. The last chapter, Chapter 12 explains how eSim can be used to do PCB layout.

The following convention has been adopted throughout this manual. All the menu names, options under each menu item, tool names, certain points to be noted, etc., are given in *italics*. Some keywords, names of certain windows/dialog boxes, names of some files/projects/folders, messages displayed during an activity, names of websites, component references, etc., are given in **typewriter** font. Some key presses, e.g. **Enter** key, **F1** key, **y** for yes, etc., are also mentioned in **typewriter** font.

Chapter 2

Architecture of eSim

eSim is a CAD tool that helps electronic system designers to design, test and analyse their circuits. But the important feature of this tool is that it is open source and hence the user can modify the source as per his/her need. The software provides a generic, modular and extensible platform for experiment with electronic circuits. This software runs on Ubuntu Linux distributions 14.04-16.04 and some flavours of Windows. It uses Python 2.7, KiCad 4.0.7, Ghdl and Ngspice.

The objective behind the development of eSim is to provide an open source EDA solution for electronics and electrical engineers. The software should be capable of performing schematic creation, PCB design and circuit simulation (analog, digital and mixed signal). It should provide facilities to create new models and components. The architecture of eSim has been designed by keeping these objectives in mind.

2.1 Modules used in eSim

Various open-source tools have been used for the underlying build-up of eSim. In this section we will give a brief idea about all the modules used in eSim.

2.1.1 Eeschema

Eeschema is an integrated software where all functions of circuit drawing, control, layout, library management and access to the PCB design software are carried out. It is the schematic editor tool used in KiCad. Eeschema is intended to work with PCB layout software such as Pcbnew. It provides netlist that describes the electrical connections of the PCB. Eeschema also integrates a component editor which allows the creation, editing and visualization of components. It also allows the user to effectively handle the symbol libraries i.e; import, export, addition and deletion of library components. Eeschema also integrates the following additional but essential functions needed for a modern schematic capture software:

1. Design rules check (DRC) for the automatic control of incorrect connections and inputs of components left unconnected. 2. Generation of layout files in POSTSCRIPT or HPGL format. 3. Generation of layout files printable via printer. 4. Bill of materials generation. 5. Netlist generation for PCB layout or for simulation.

This module is indicated by the label 1 in Fig. 2.1.

As Eeschema is originally intended for PCB Design, there are no fictitious components¹ such as voltage or current sources. Thus, we have added a new library for different types of voltage and current sources such as sine, pulse and square wave. We have also built a library which gives printing and plotting solutions. This extension, developed by us for eSim, is indicated by the label 2 in Fig. 2.1.

2.1.2 CvPcb

CvPcb is a tool that allows the user to associate components in the schematic to component footprints when designing the printed circuit board. CvPcb is the footprint editor tool in KiCad. Typically the netlist file generated by Eeschema does not specify which printed circuit board footprint is associated with each component in the schematic. However, this is not always the case as component footprints can be associated during schematic capture by setting the component's footprint field. CvPcb provides a convenient method of associating footprints to components. It provides footprint list filtering, footprint viewing, and 3D component model viewing to help ensure that the correct footprint is associated with each component. Components can be assigned to their corresponding footprints manually or automatically by creating equivalence files. Equivalence files are look up tables associating each component with its footprint. This interactive approach is simpler and less error prone than directly associating footprints in the schematic editor. This is because CvPcb not only allows automatic association, but also allows to see the list of available footprints and displays them on the screen to ensure the correct footprint is being associated. This module is indicated by the label 3 in Fig. 2.1.

2.1.3 Pcbnew

Pcbnew is a powerful printed circuit board software tool. It is the layout editor tool used in KiCad. It is used in association with the schematic capture software Eeschema, which provides the netlist. Netlist describes the electrical connections of the circuit. CvPcb is used to assign each component, in the netlist produced by Eeschema, to a module that is used by Pcbnew. The features of Pcbnew are given below:

¹Signal generator or power supply is not a single component but in circuit simulation, we consider them as a component. While working with actual circuit, signal generator or power supply gives input to the circuit externally thus, doesn't require for PCB design.

- It manages libraries of modules. Each module is a drawing of the physical component including its footprint - the layout of pads providing connections to the component. The required modules are automatically loaded during the reading of the netlist produced by CvPcb.
- Pcbnew integrates automatically and immediately any circuit modification by removal of any erroneous tracks, addition of new components, or by modifying any value (and under certain conditions any reference) of old or new modules, according to the electrical connections appearing in the schematic.
- This tool provides a rats nest display, a hairline connecting the pads of modules connected on the schematic. These connections move dynamically as track and module movements are made.
- It has an active Design Rules Check (DRC) which automatically indicates any error of track layout in real time.
- It automatically generates a copper plane, with or without thermal breaks on the pads.
- It has a simple but effective auto router to assist in the production of the circuit. An export/import in SPECCTRA dsn format allows to use more advanced auto-routers.
- It provides options specifically for the production of ultra high frequency circuits (such as pads of trapezoidal and complex form, automatic layout of coils on the printed circuit).
- Pcbnew displays the elements (tracks, pads, texts, drawings and more) as actual size and according to personal preferences such as:
 - display in full or outline.
 - display the track/pad clearance.

This module is indicated by the label 4 in Fig. 2.1.

2.1.4 KiCad to Ngspice converter

Analysis parameters, and the source details are provided through this module. It also allows us to add and edit the device models and subcircuits, included in the circuit schematic. Finally, this module facilitates the conversion of KiCad netlist to Ngspice compatible ones.

It is developed by us for eSim and it is indicated by the label 7 in Fig. 2.1. The use of this module is explained in detail in section (yet to be put).

2.1.5 Model Builder

This tool provides the facility to define a new model for devices such as, 1. Diode 2. Bipolar Junction Transistor (BJT) 3. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) 4. Junction Field Effect Transistor (JFET) 5. IGBT and 6. Magnetic core. This module also helps edit existing models. It is developed by us for eSim and it is indicated by the label 5 in Fig. 2.1.

2.1.6 Subcircuit Builder

This module allows the user to create a subcircuit for a component. Once the subcircuit for a component is created, the user can use it in other circuits. It has the facility to define new components such as, Op-amps, IC-555, UJT and so on. This component also helps edit existing subcircuits. This module is developed by us for eSim and it is indicated by the label 6 in Fig. 2.1.

2.1.7 Ngspice

Ngspice is a general purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analysis. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, lossless and lossy transmission lines (two separate implementations), switches, uniform distributed RC lines, and the five most common semiconductor devices: diodes, BJTs, JFETs, MESFETs, and MOSFET. This module is indicated by the label 9 in Fig. 2.1.

2.1.8 NGHDL

NGHDL, a module for mixed mode circuit simulation is also integrated with eSim. It uses ghdl for digital simulation and the mixed mode simulation happens through NgSpice.

2.1.9 OpenModelica

OpenModelica (OM) is an open source modeling and simulation tool based on Modelica language. Two modules of OpenModelica, OMEdit, an IDE for modeling and simulation and OMOptim, an IDE for optimisation are integrated with eSim.

2.2 Work flow of eSim

Fig. 2.1 shows the work flow in eSim. The block diagram consists of mainly three parts:

- Schematic Editor

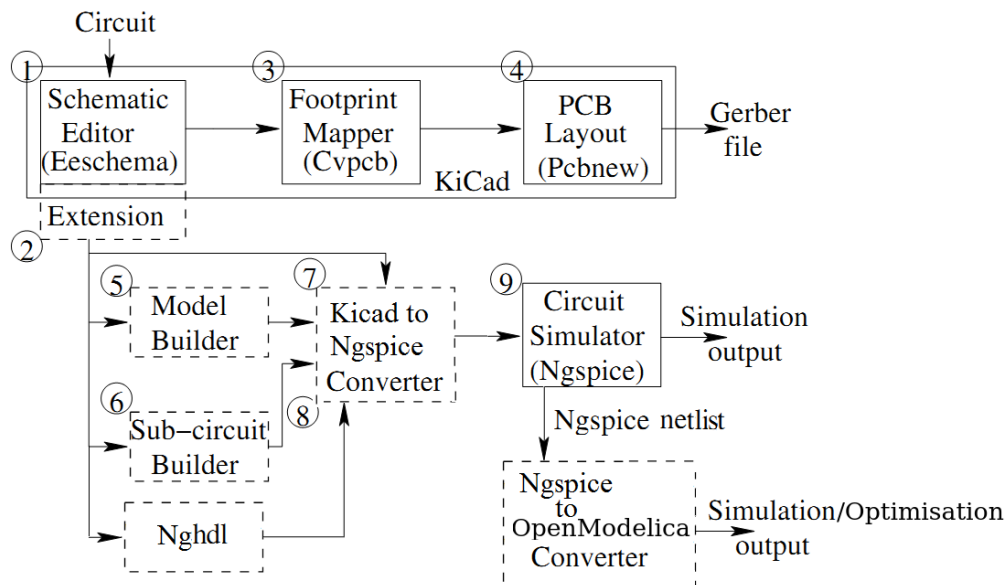


Figure 2.1: Work flow in eSim. (Boxes with dotted lines denote the modules developed in this work).

- PCB Layout Editor
- Circuit Simulators

Here we explain the role of each block in designing electronic systems. Circuit design is the first step in the design of an electronic circuit. Generally a circuit diagram is drawn on a paper, and then entered into a computer using a schematic editor. Eeschema is the schematic editor for eSim. Thus all the functionalities of Eeschema are naturally available in eSim.

Libraries for components, explicitly or implicitly supported by Ngspice, have been created using the features of Eeschema. As Eeschema is originally intended for PCB design, there are no fictitious components such as voltage or current sources. Thus, a new library for different types of voltage and current sources such as sine, pulse and square wave, has been added in eSim. A library which gives the functionality of printing and plotting has also been created.

The schematic editor provides a netlist file, which describes the electrical connections of the design. In order to create a PCB layout, physical components are required to be mapped into their footprints. To perform component to footprint mapping, CvPcb is used. Footprints have been created for the components in the newly created libraries. Pcbnew is used to draw a PCB layout.

After designing a circuit, it is essential to check the integrity of the circuit design. In the case of large electronic circuits, breadboard testing is impractical. In such cases, electronic system designers rely heavily on simulation. The accuracy of the simulation results can be increased by accurate modeling of the circuit elements. Model Builder provides the facility to define a new model for devices and edit existing models. Complex circuit elements can be created by hierarchical modeling. Subcircuit Builder provides an easy way to create a subcircuit.

The netlist generated by Schematic Editor cannot be directly used for simulation due to compatibility issues. Netlist Converter converts it into Ngspice compatible format. The type of simulation to be performed and the corresponding options are provided through a graphical user interface (GUI). This is called KiCad to Ngspice Converter in eSim.

eSim uses Ngspice for analog, digital, mixed-level/mixed-signal circuit simulation. Ngspice is based on three open source software packages

- Spice3f5 (analog circuit simulator)
- Cider1b1 (couples Spice3f5 circuit simulator to DSIM device simulator)
- Xspice (code modeling support and simulation of digital components through an event driven algorithm)

It is a part of gEDA project. Ngspice is capable of simulating devices with BSIM, EKV, HICUM, HiSim, PSP, and PTM models. It is widely used due to its accuracy even for the latest technology devices.

Chapter 3

Installing eSim

3.1 eSim installation in Ubuntu

1. Download eSim installer for Linux from <http://esim.fossee.in/downloads> to a local directory and unpack it.

You can also unpack the installer through the terminal. Open the terminal and navigate to the directory where this INSTALL file is located. Use the following command to unpack:

```
$ unzip eSim-1.1.3.zip
```

2. To install eSim and other dependencies run the following command.

```
$ ./install-eSim.sh --install
```

Above script will install eSim along with the dependencies.

3. To run eSim from the terminal, type:

```
$ esim
```

or you can double click on eSim icon created on the Desktop after installation.

3.2 eSim installation in Windows

1. Download eSim from website <http://esim.fossee.in/downloads>

`eSim-Windows-Installer.zip` file.

2. By default the installer file will install in Program Files of C drive and since there is space, it will give an error. Create a folder name fossee and copy the installer folder. Open eSim-Windows-Installer folder, right click on **Setup** file and select **run as administrator**. Click **Yes** and **Next** to complete the installation.

3. **eSim** icon will be created on desktop. You can double click on the eSim icon created on the Desktop after installation.

Chapter 4

Getting Started

In this chapter we will get started with eSim. Referring to this chapter will make one familiar with eSim and will help plan the project before actually designing a circuit. Lets get started.

4.1 How to launch eSim in Ubuntu?

After the installation of eSim, a shortcut to eSim is created on the Desktop. To launch eSim double click on the shortcut.

Alternately, you can also launch esim from the terminal.

1. Go to terminal.
2. Type **esim** and press **Enter**.

The first window that appears is workspace dialog as shown in Fig. 4.1.

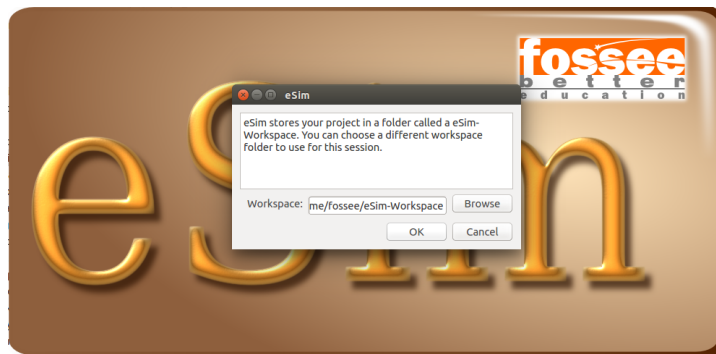


Figure 4.1: eSim-Workspace

The default workspace is eSim-Workspace under home directory. To create new workspace use **browse** option.

4.2 eSim User Interface

The main graphic window of eSim is as shown in Fig. 4.2.

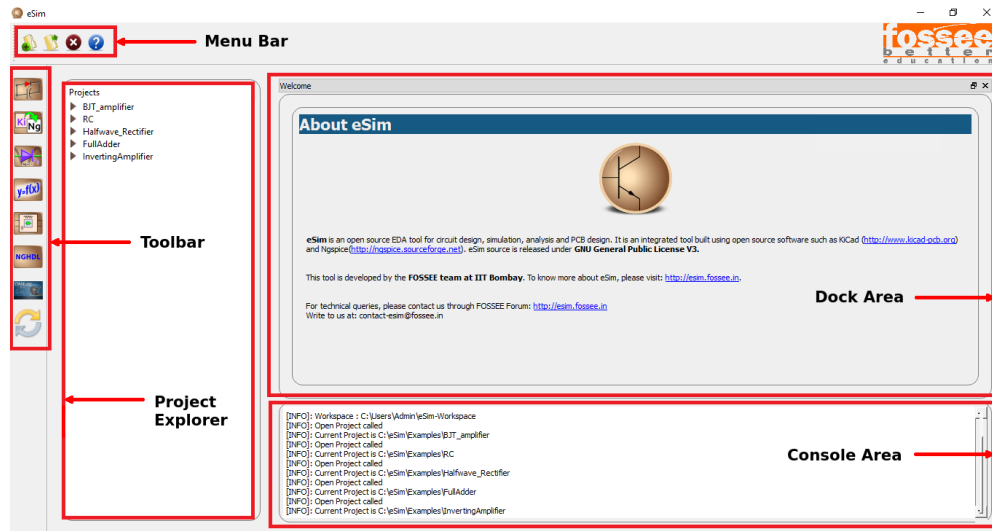


Figure 4.2: eSim Main GUI

The eSim window consists of the following sections.

1. Toolbar
2. Menubar
3. Project explorer
4. Dockarea
5. Console area

4.2.1 Toolbar

The toolbar consists of the following buttons. See Fig. 4.3.

Open Schematic

The first button on the toolbar is the *Schematic Editor*. Clicking on this button will open Eeschema, the KiCad schematic editor. If a new project is being created, one will get a dialog box confirming the creation of a schematic. This is illustrated in See Fig. 4.4. However, if an already existing project is opened, the schematic editor window is opened. To know how to use the schematic editor to create circuit schematics, refer to Chapter 5.

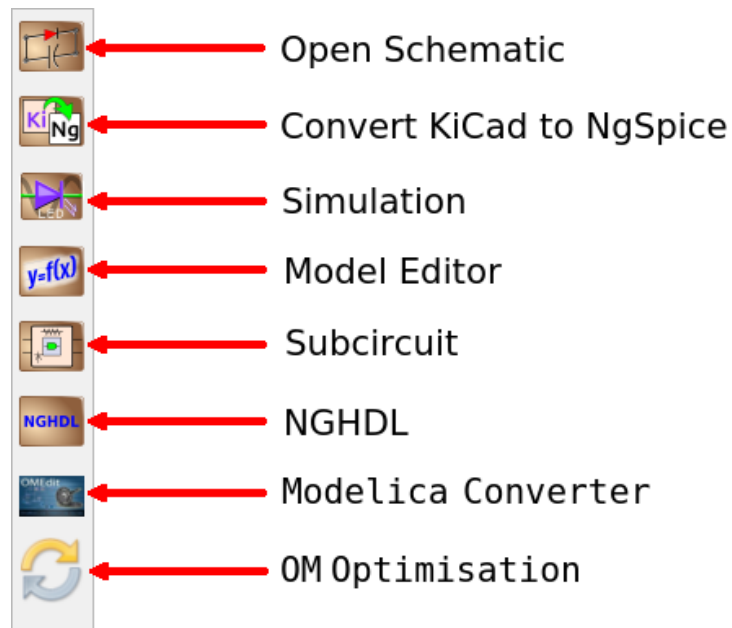


Figure 4.3: Toolbar

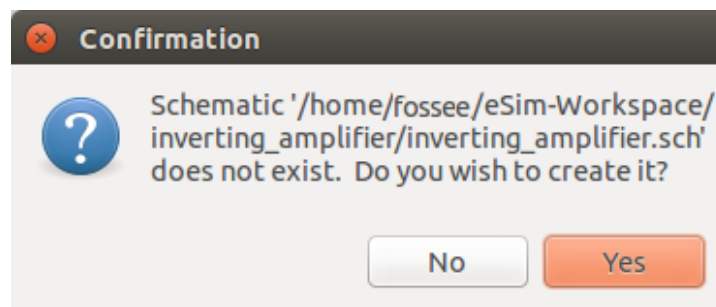


Figure 4.4: Confirmation for schematic creation

Convert KiCad to Ngspice

In the Eeschema window, after creating the schematic the netlist is generated. This tool converts the generated KiCad spice netlist into Ngspice compatible netlist. The KiCad to Ngspice window consists of five tabs namely *Analysis*, *Source Details*, *Ngspice Model*, *Device Modeling* and *Subcircuits*.

The details of these tabs are as follows.

- *Analysis*: This feature helps the user to insert the parameters for performing different types of analysis such as Operating point analysis, DC analysis, AC

analysis, transient analysis, DC Sweep Analysis.

It has the facility to insert

- Type of analysis such as AC or DC or Transient
- Values for analysis
- *Source Details:* eSim sources are added from `eSim_Sources` library. Source such as *SINE, AC, DC, PULSE* are in this library. The parameter values to all the sources added in the schematic can be given through 'Source Details'.
- *Ngspice Model:* Ngspice has in-built model such as *flipflop(D,SR,JK,T), gain, summer* etc. which can be utilised while building a circuit. eSim allows to add and modify Ngspice model parameter through Ngspice Model tab.
- *Device Modeling:* Devices like *Diode, JFET, MOSFET, IGBT, MOS* etc used in the circuit can be modeled using device model libraries. eSim also provides editing and adding new model libraries. While converting KiCad to Ngspice, these library files are added to the corresponding devices used in the circuit.
- *Subcircuits:* eSim allows you to build subcircuits. The subcircuits can again have components having subcircuits and so on. This enables users to build commonly used circuits as subcircuits and then use it across circuits. The subcircuits are added to the main circuits using this facility. We can also edit already existing subcircuits.

Once the values have been entered, press the **Convert** button. This will generate the `.cir.out` file in the same project directory. Note that *KiCad to Ngspice Converter* can only be used if the KiCad spice netlist `.cir` file is already generated.

Simulation

The netlist generated using the *KiCad to Ngspice* converter is simulated using *Simulation* button on the eSim left toolbar. This will run the Ngspice simulation for current project. eSim have two options to see the simulation output. The first one is the Python plotting window which opens up in the dock area, as shown in Fig. 4.5. The second is the Ngspice window with the simulation data. The user can type in Ngspice commands to view the plots.

Note: If the user has used the plot components (available under `eSim_Plot` library) at various nodes in the circuit schematic the Ngspice plots are displayed automatically.

Model Editor

eSim also gives an option to re-configure the model library of a device. It facilitates the user to change model library of devices such as diode, transistor, MOSFET, etc. It

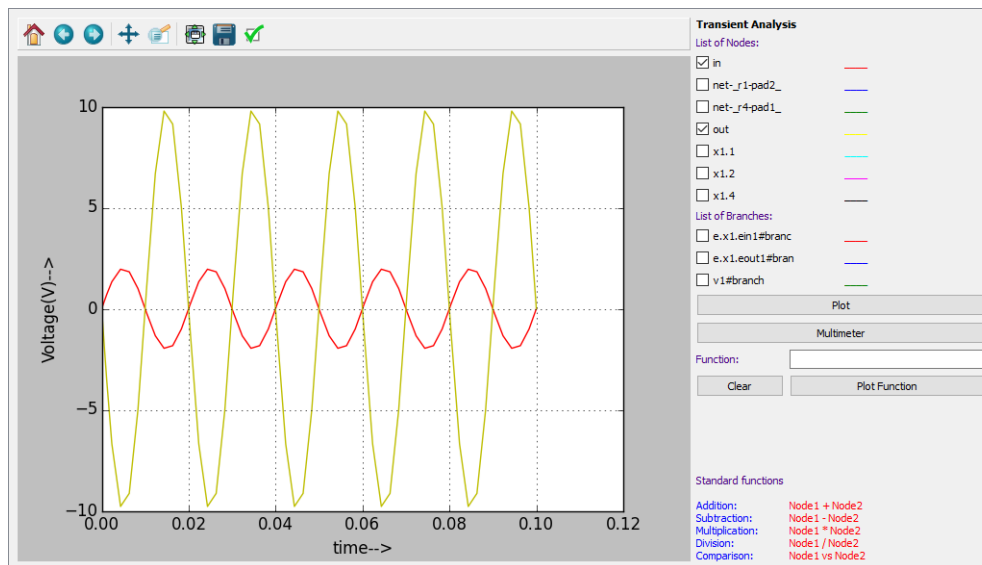


Figure 4.5: Simulation Output in Python Plotting Window

also facilitates the user to load the spice library externally and use it for the existing or newly added models. To know more about Model Editor, refer to Chapter 7.

Subcircuit

eSim also allows the user to build subcircuits. The subcircuits can again have components having subcircuits and so on. This enable users to build commonly used circuits as subcircuits and then use it across circuits. For example, one can build a 12 Volt power supply as a subcircuit and then use it as just a single component across circuits without having to recreate it. Clicking on *Subcircuit Builder* tool will allow one to edit or create a subcircuit. To know how to make a subcircuit, refer to Chapter 8.

Nghdl

Nghdl is an add on to eSim for mixed mode circuit simulation. It uses Ghdl for digital simulation and the mixed mode simulation is done through the Ngspice. It takes digital values from Ghdl using socket programming.

Modelica Converter

OpenModelica (OM) is an open source modeling and simulation tool based on Modelica language. Modelica is an object oriented language. The Modelica Converter in eSim interface, converts the ngspice netlist to Modelica format. This facility will be only

available if you have OpenModelica already installed in the system. More details on how to use this module is available in Chapter 10.

OM Optimisation

OMOptimisation (OMOptim) is a powerful and interactive tool for performing design optimisation. It has a good library of electrical components called Modelica Standard Library (MSL). OMOptim is stable and robust. It is very easy to add objective functions to the OMOptim interface.

4.2.2 Menubar

- **New Project:** New projects are created in the eSim-Workspace. When this menu is selected, a new window opens up with **Enter Project name** field. Type the name of the new project and click on **OK**. A project directory will be created in eSim-Workspace. The name of this folder will be the same as that of the project created. *Make sure that the project name does not have any spaces in between.* This project is also added to the project explorer.
- **Open Project:** This opens the file dialog of default eSim-Workspace where the projects are stored. Select the required project and click on **Open**. The selected project is added to the project explorer.
- **Exit:** This button closes the opened project.
- **Help:** It opens user manual in the browser.

4.2.3 Project Explorer

Project explorer contains the list of all the projects previously added to it. Select a project and double click on it, this will display all the files under this project. Right click on any displayed file to open it. To remove or refresh any project file from the project explorer, right click on the main project file.

4.2.4 Dockarea

This area is used to open the following windows.

1. KiCad to Ngspice converter
2. Ngspice plotting
3. Python plotting
4. Model builder

5. Subcircuit builder

Modules/Windows will appear here as per your selection.

4.2.5 Console Area

Console area provides the log information about the activity done during the current session.

Chapter 5

Schematic Creation

The first step in the design of an electronic system is the design of its circuit. This circuit is usually created using a **Schematic Editor** and is called a **Schematic**. eSim uses **Eeschema** as its schematic editor. Eeschema is the schematic editor of KiCad. It is a powerful schematic editor software. It allows the creation and modification of components and symbol libraries and supports multiple hierarchical layers of printed circuit design.

5.1 Familiarizing the Schematic Editor interface

Fig. 5.1 shows the schematic editor and the various menu and toolbars. We will explain them briefly in this section.

5.1.1 Top menu bar

The top menu bar will be available at the top left corner. Some of the important menu options in the top menu bar are:

1. File - The file menu items are given below:
 - (a) New - Clear current schematic and start a new one
 - (b) Open - Open a schematic
 - (c) Open Recent - A list of recently opened files for loading
 - (d) Save Schematic project - Save current sheet and all its hierarchy.
 - (e) Save Current Sheet Only - Save current sheet, but not others in a hierarchy.
 - (f) Save Current sheet as - Save current sheet with a new name.
 - (g) Page Settings - Set preferences for printing the page.
 - (h) Print - Access to print menu (See Fig. 5.2).
 - (i) Plot - Plot the schematic in Postscript, HPGL, SVF or DXF format
 - (j) Close - Close the schematic editor.

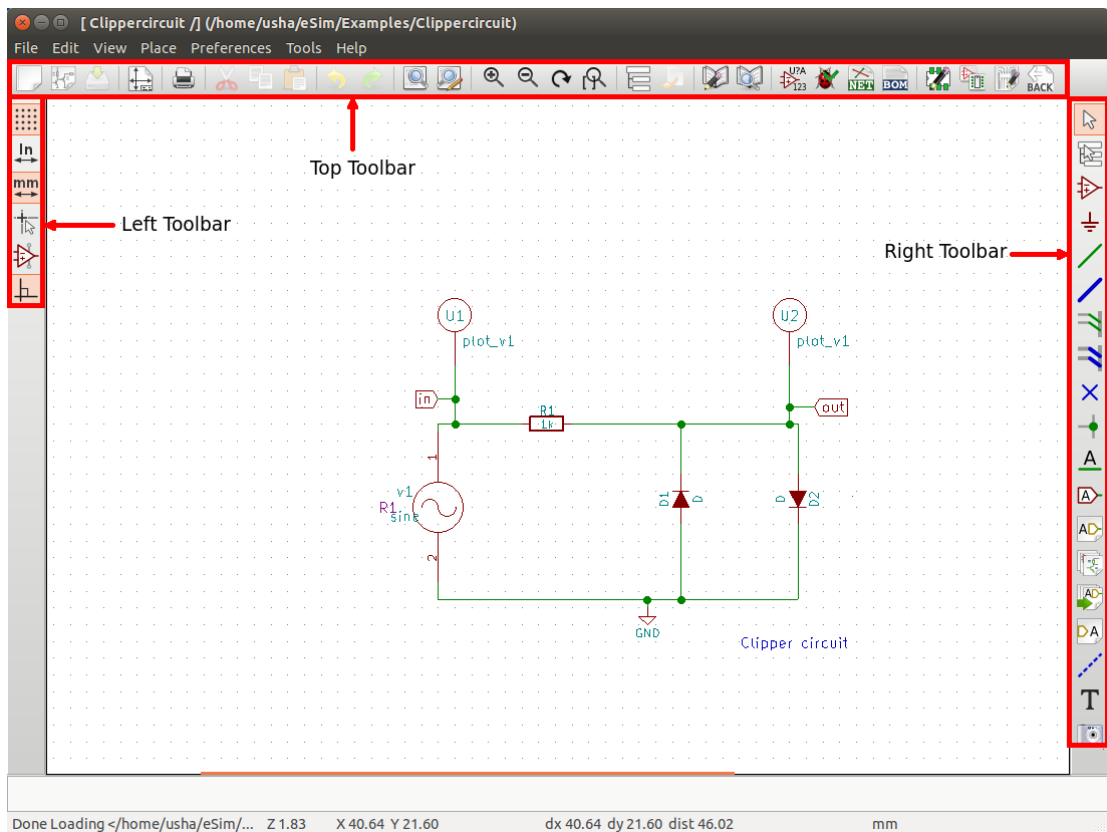


Figure 5.1: Schematic editor with the menu bar and toolbars marked

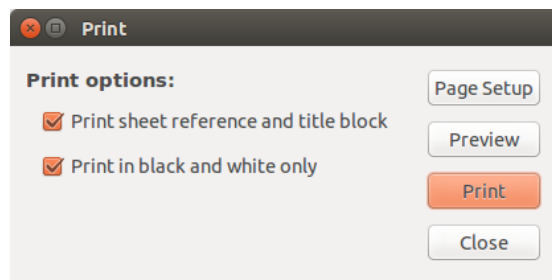


Figure 5.2: Print options

2. Place - The place menu has shortcuts for placing various items like components, wire and junction, on to the schematic editor window. See Sec. 5.1.5 to know more about various shortcut keys (hotkeys).
3. Preferences - The preferences menu has the following options:

- (a) Component Libraries - Select component libraries and library paths. This enables the user to add the libraries, if the libraries are not loaded in the Eeschema.
- (b) Schematic Editor Options - Select colors for various items, display options and set hot keys.
- (c) Language - Shows the current list of available languages. Use default.
- (d) Import and Export - Contain options to load and save preferences and import/ export hot key configuration files. See Sec. 5.1.5 to know about various hotkeys.

5.1.2 Top toolbar

Some of the important tools in the top toolbar are discussed below. They are marked in Fig. 5.3.

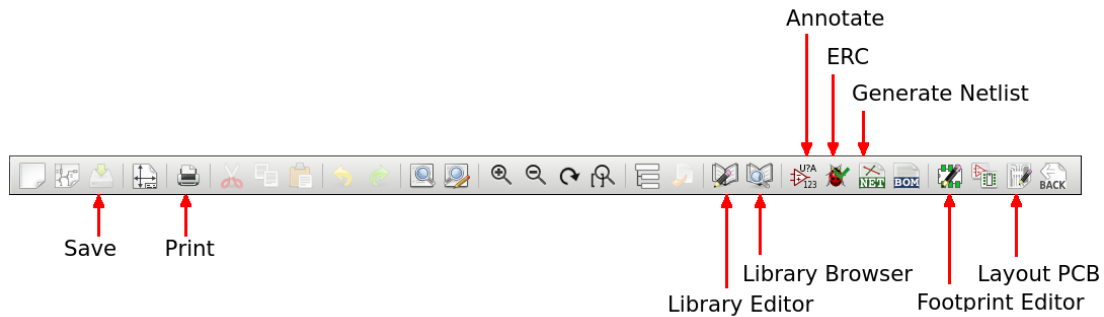


Figure 5.3: Toolbar on top with important tools marked

1. Save - Save the current schematic
2. Print - Print the schematic
3. Navigate schematic hierarchy - Navigate among the root and sub-sheets in the hierarchy
4. Library Editor - Create or edit components.
5. Library Browser - Browse through the various component libraries available
6. Annotate - Annotate the schematic
7. Check ERC - Do Electric Rules Check for the schematic
8. Generate Netlist - Generate a netlist for PCB design(`.net`) or for simulation(`.cir`).
9. Create BOM - Create a Bill of Materials of the schematic
10. Footprint editor - Map each component in the PCB netlist to a footprint
11. Layout PCB - Lay tracks between the footprints to get the PCB layout

5.1.3 Toolbar on the right

The toolbar on the right side of the schematic editor window has many important tools. Some of them are marked in Fig. 5.4. Let us now look at each of these tools and their

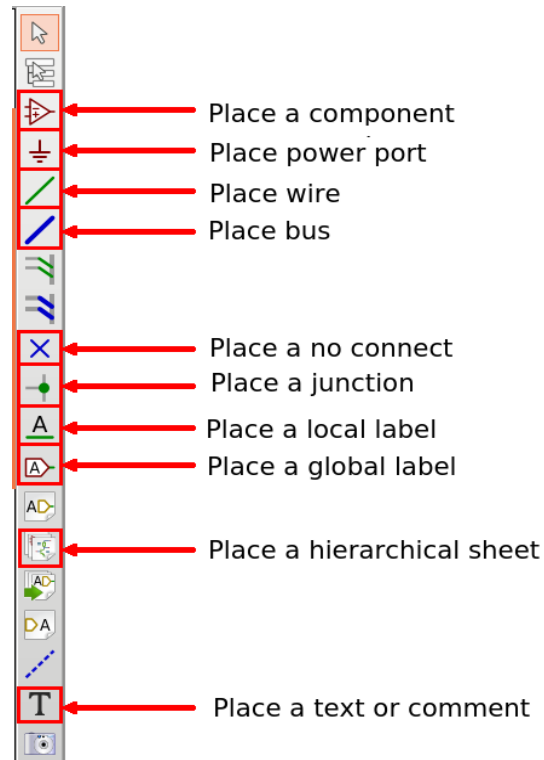


Figure 5.4: Toolbar on right with important tools marked

uses.

1. Place a component - Load a component to the schematic. See Sec. 5.3.1 for more details.
2. Place a power port - Load a power port (Vcc, ground) to the schematic.
3. Place wire - Draw wires to connect components in schematic.
4. Place bus - Place a bus on the schematic.
5. Place a no connect - Place a no connect flag, particularly useful in ICs.
6. Place a local label - Place a label or node name which is local to the schematic.
7. Place a global label - Place a global label (these are connected across all schematic diagrams in the hierarchy).
8. Create a hierarchical sheet - Create a sub-sheet within the root sheet in the hierarchy. Hierarchical schematics is a good solution for big projects.
9. Place a text or comment - Place a text or comment in the schematic.

5.1.4 Toolbar on the left

Some of the important tools in the toolbar on the left are discussed below. They are marked in Fig. 5.5.

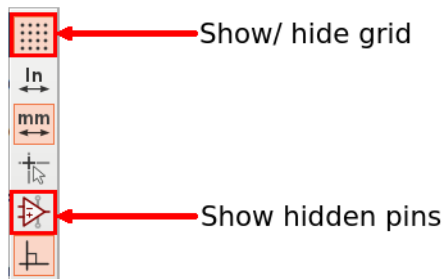


Figure 5.5: Toolbar on left with important tools marked

1. Show/Hide grid - Show or Hide the grid in the schematic editor. Pressing the tool again hides (shows) the grid if it was shown (hidden) earlier.
2. Show hidden pins - Show hidden pins of certain components, for example, power pins of certain ICs.

5.1.5 Hotkeys

A set of keyboard keys are associated with various operations in the schematic editor. These keys save time and make it easy to switch from one operation to another. The list of hotkeys can be viewed by going to Preferences in the top menu bar. Choose *Schematic Editor Options* and select *Controls* tab. The hotkeys can also be edited here. Some frequently used hotkeys, along with their functions, are given below:

- F1 - Zoom in
- F2 - Zoom out
- Ctrl + Z - Undo
- Delete - Delete item
- M - Move item
- C - Copy item
- A - Add/place component
- P - Place power component
- R - Rotate item
- X - Mirror component about X axis
- Y - Mirror component about Y axis
- E - Edit schematic component
- W - Place wire
- T - Add text
- S - Add sheet

Note: Both lower and upper-case keys will work as hotkeys.

5.2 eSim component libraries

eSim schematic editor has a huge collection of components. As Eeschema is meant to be a schematic editor to create circuits for PCB, Eeschema lacks some components that are necessary for simulation (e.g. probes(plot_v and current sources). A set of component libraries has been created with such components under the label *eSim_**. These libraries are Ngspice compatible. If one is using eSim only for designing a PCB, then one might not need these libraries. However, these libraries are essential if one needs to simulate one's circuit. Hereafter, we will refer to these libraries as eSim libraries to distinguish them from libraries already present in Eeschema (Eeschema libraries) as shown in Fig. 5.6.

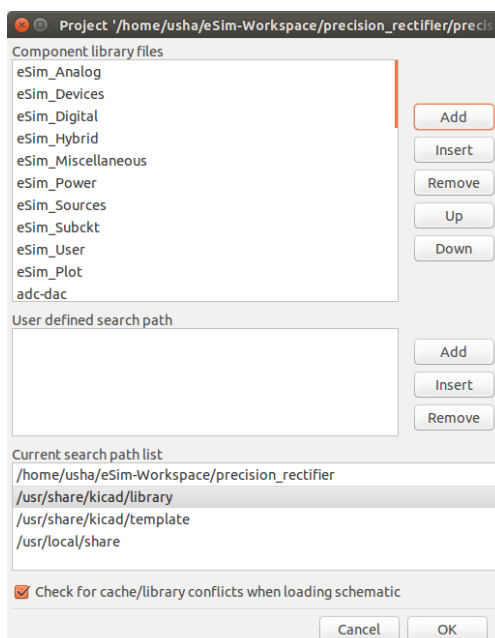


Figure 5.6: eSim-Components Libraries

The following list shows the various eSim component libraries.

- *eSim_Analog* - Contains Ngspice analog models such as aswitch(analog switch), summer(adder model), Transfo(Transformer), zener.
- *eSim_Devices* - Includes elementary components like resistor, capacitor, transistor, MosFet.
- *eSim_Digital* - Includes Ngspice digital models such as basic gates (AND, OR, NOR,NAND,XOR), filpflops (SR, D, JK), buffer, inverter.

- *eSim_Hybrid* - Includes components like ADC and DAC.
- *eSim_Miscellaneous* - Contains components like ic(used for giving initial conditions in circuit) and port(used in creating subcircuits).
- *eSim_Plot* - Contains plotting components like plot_v1 (plot voltage at a node), plot_v2 (plot voltage between 2 nodes), plot_i2 (plot current through branch), plot_log (plot logarithmic voltage at a node).
- *eSim_Power* - Includes power components like DIAC, TRIAC and SCR.
- *eSim_Sources* - Contains sources for the circuits like AC voltage source, DC voltage source, sine source and pulse source.
- *eSim_Subckt* - Contains subcircuit components like Op-Amp(UA 741), IC 555, Half adder and full adder.
- *eSim_User* - A repository for all user created components

5.3 Schematic creation for simulation

There are certain differences between the schematic created for simulation and that created for PCB design. We need certain components like plots and current sources for simulation whereas these are not needed for PCB design. For PCB design, we would require connectors (e.g. DB15 and 2 pin connector) for taking signals in and out of the PCB whereas these have no meaning in simulation. This section covers schematic creation for simulation. Refer to Chapter 12 to know how to create schematic for PCB design.

The first step in the creation of circuit schematic is the selection and placement of required components. Let us see this using an example. Let us create the circuit schematic of an RC filter given in Fig. 5.10c and do a transient simulation.

5.3.1 Selection and placement of components

We would need a resistor, a capacitor, a voltage source, ground terminal and some plot components. To place a resistor on the schematic editor window, select the *Place a component* tool from the toolbar on the right side and click anywhere on the schematic editor. This opens up the component selection window. This action can also be performed by pressing the key A. Choose the *eSim_Devices* library and click on the arrow near it. This will open the *eSim_Devices* library and the resistor component can be found here. Fig. 5.7 shows the selection of resistor component. Click on OK. A resistor will be tied to the cursor. Place the resistor on the schematic editor by a single click. To place the next component, i.e., capacitor, click again on the schematic editor. The capacitor component is also found under *eSim_Devices* library. Select it and then click on OK. Place the capacitor on the schematic editor by a single click.

Let us now place a sinusoidal voltage source. This is required for performing transient analysis. On the component selection window, choose the library *eSim_source*. Select

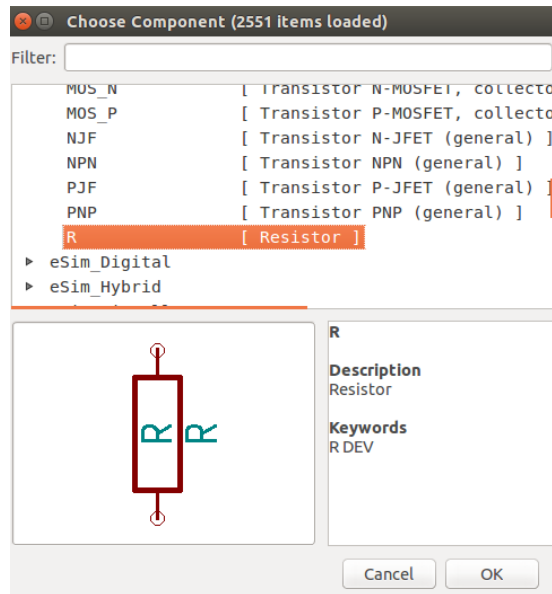


Figure 5.7: Placing a resistor using the Place a Component tool

the component **SINE** and click on **OK**. Place the sine source on the schematic editor by a single click. Similarly select and place **gnd**, a ground terminal from the **power** library.

The plot components can be found under the **eSim.Plot** library. Select the **plot.v1** component and place the component. Once all the components are placed, the schematic editor would look like as in Fig. 5.8.

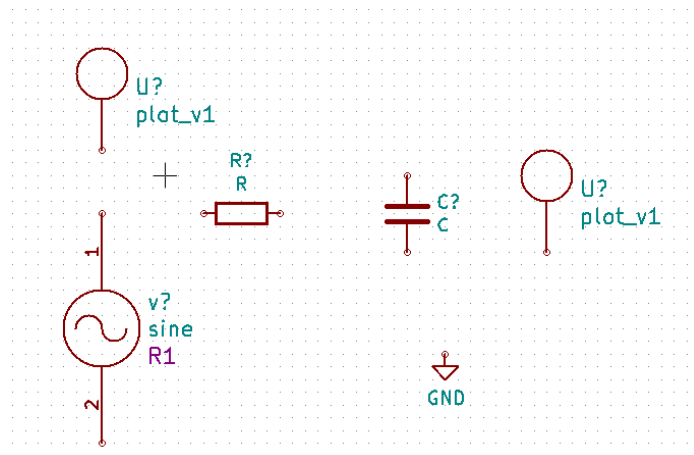


Figure 5.8: All RC circuit components placed

Let us rotate the resistor to complete the circuit. To rotate the resistor, place the

cursor on the resistor as shown in Fig. 5.9 and press the key R. This applies to all components.

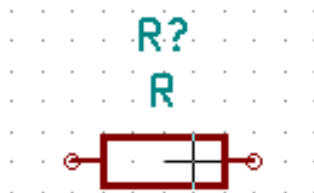


Figure 5.9: Placing the cursor (cross mark) on the resistor component

If one wants to move a component, place the cursor on top of the component and press the key M. The component will be tied to the cursor and can be moved in any direction.

5.3.2 Wiring the circuit

The next step is to wire the connections. Let us connect the resistor to the capacitor. To do so, point the cursor to the terminal of resistor to be connected and press the key W. It has now changed to the wiring mode. Alternately, this can also be done by selecting the *Place wire* tool on the right side toolbar. Move the cursor towards the terminal of the capacitor and click on it. A wire is formed as shown in Fig. 5.10a. Similarly connect

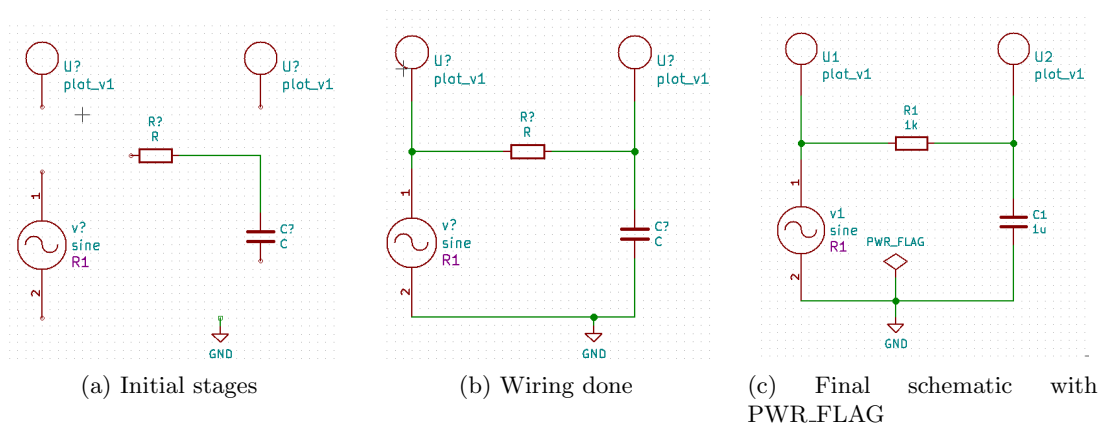


Figure 5.10: Various stages of wiring

the wires between all terminals and the final schematic would look like Fig. 5.10b.

5.3.3 Assigning values to components

We need to assign values to the components in our circuit i.e., resistor and capacitor. Note that the sine voltage source has been placed for simulation. The specifications of sine source will be given during simulation. To assign value to the resistor, place the cursor above the letter R (not R?) and press the key E. Choose *Field value*. Type 1k in the *Edit value field* box as shown in Fig. 5.11. 1k means $1k\Omega$. Similarly give the value 1u for the capacitor. 1u means $1\mu F$.

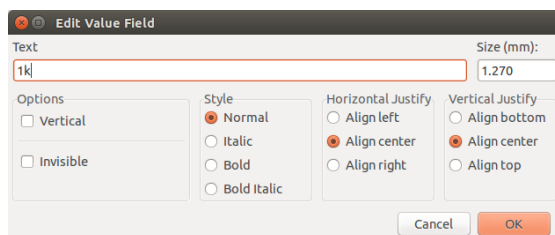


Figure 5.11: Editing value of resistor

5.3.4 Annotation and ERC

The next step is to annotate the schematic. Annotation gives unique references to the components. To annotate the schematic, click on *Annotate Schematic Components* tool from the top toolbar. Click on **Annotate**, then click on **OK** and finally click on **Close** as shown in Fig. 5.12. The schematic is now annotated. The question marks next to component references have been replaced by unique numbers. If there are more than one instance of a component (say resistor), the annotation will be done as R1, R2, etc.

Let us now do ERC or **E**lectric **R**ules **C**heck. To do so, click on *Perform electric rules check* tool from the top toolbar. Click on **Run** button. The error as shown in Fig. 5.13 may be displayed. Click on close in the test erc window.

There will be a green arrow pointing to the source of error in the schematic. Here it points to the ground terminal. This is shown in Fig. 5.14.

This error is due to the GND pin. The GND pin is a power input pin and Eeschema gives this error as there is no power line connected. To correct this error, a flag has to be placed indicating that there will be an external power line connected to it. Place a **PWR_FLAG** from the Eeschema library *power*. Connect the power flag to the ground terminal as shown in Fig. 5.10c. Repeat the ERC. Now there are no errors. With this we have created the schematic for simulation.

5.3.5 Netlist generation

To simulate the circuit that has been created in the previous section, we need to generate its netlist. **Netlist** is a list of components in the schematic along with their connection

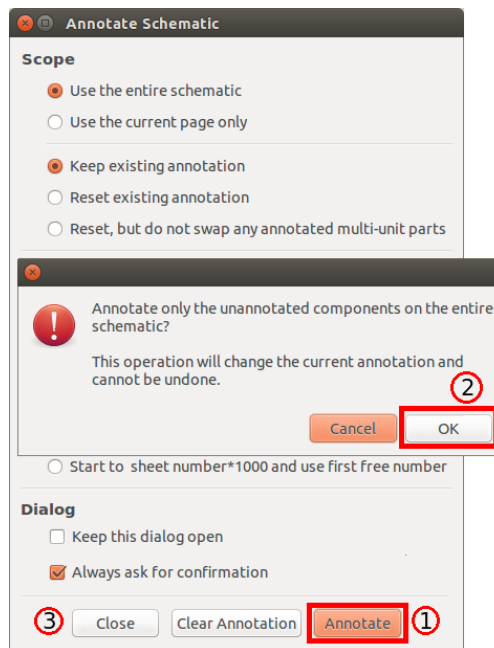


Figure 5.12: Steps in annotating a schematic: 1. First click on Annotation then 2. Click on OK then 3. Click on close



Figure 5.13: ERC error

information. To do so, click on the *Generate netlist* tool from the top toolbar. Click on Spice from the window that opens up. Check the option **Default Format**. Then click on *Generate*. This is shown in Fig. 5.15. Save the netlist. This will be a .cir file. Do not change the directory while saving. Now the netlist is ready to be simulated. Refer to [?] or [?] to know more about Eeschema.

5.4 Tools for creating the PCB layout

The Eeschema top toolbar also has two important tools which can help the user to generate the PCB layout of the created schematic.



Figure 5.14: Green arrow pointing to Ground terminal indicating an ERC error

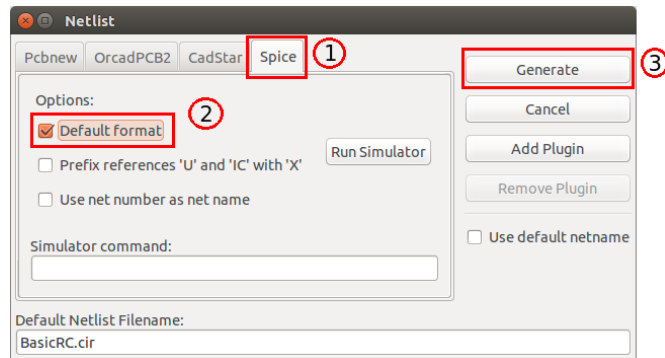


Figure 5.15: Steps in generating a Netlist for simulation: 1. Click on Spice then 2. Check the option Default Format then 3. Click on Generate

5.4.1 FootPrint Editor

Clicking on the *Footprint Editor* tool will open the *CvPcb* window. This window will ideally open the .net file for the current project. So, before using this tool, one should have the netlist for PCB design (a .net file). To know more about how to assign footprints to components, see Chapter 12.

5.4.2 PCB Layout

Clicking on the *Layout Editor* tool will open *Pcbnew*, the layout editor used in eSim. In this window, one will create the PCB. It involves laying tracks and vias, performing optimum routing of tracks, creating one or more copper layers for PCB, etc. It will be saved as a .brd file in the current project directory. Chapter 12 explains how to use the *Layout Editor* to design a PCB.

Chapter 6

Simulation

Circuit simulation uses mathematical models to replicate the behaviour of an actual device or circuit. Simulation software allows to model circuit operations. Simulating a circuit's behaviour before actually building it can greatly improve design efficiency. eSim uses Ngspice for analog, digital and mixed-level/mixed-signal circuit simulation. The various steps involved in simulating a circuit schematic in eSim are explained in the sections below:

6.1 Kicad to Ngspice Conversion

In the chapter on schematic creation, we have learnt to generate the netlist from circuit schematic. The generated netlist is not compatible with Ngspice. eSim uses Ngspice to simulate the circuit schematic. Hence the netlist i.e. `.cir` file generated should be converted in to a Ngspice compatible file. The *Convert KiCad to Ngspice* tool on eSim left toolbar is used to do this. Let us now see the various tabs and their functions available under this.

6.1.1 Analysis

In order to simulate a circuit, the user must define the type of analysis to be done on the circuit. This tab is used to insert the type of analysis and value of the analysis parameters to the netlist. eSim supports three types of analyses: 1. *DC Analysis* (Operating Point and DC Sweep) 2. *AC Small-signal Analysis* 3. *Transient Analysis* These are explained below.

In the current example for simulating an RC circuit, select the analysis type as **transient** analysis and enter the values as shown in the Fig. 6.1.

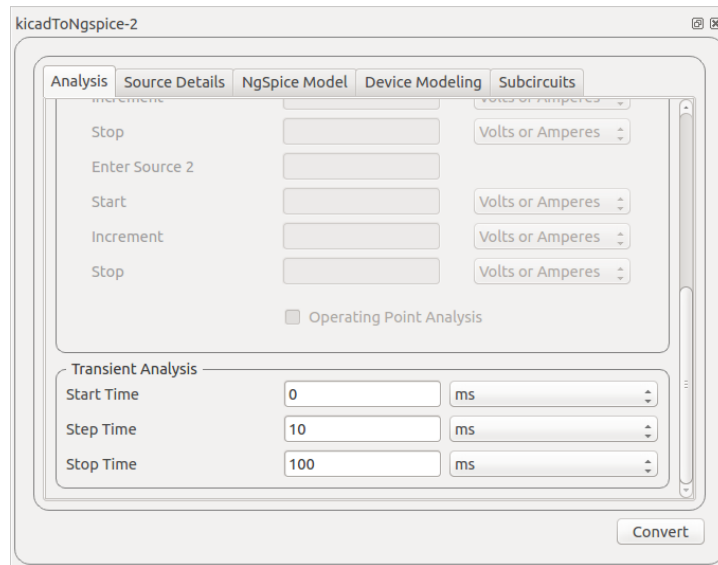


Figure 6.1: KiCad to Ngspice Window

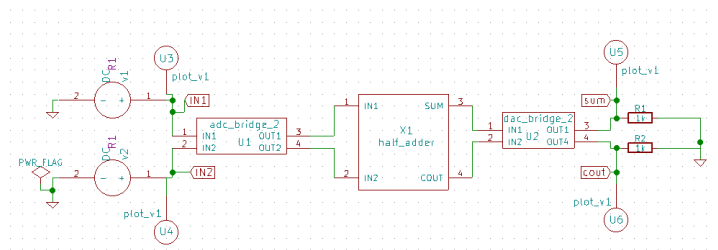


Figure 6.2: Half Adder Schematic

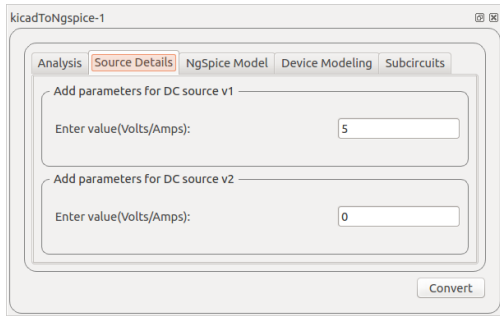
6.1.2 Source Details

The various parameter values of the sources added in the schematic can be added using this tool. *Source details* is a dynamic tab, i.e. the fields are added as per the number of sources in the circuit. For example, consider a Half-Adder circuit as shown in Fig. 6.2. Here, we have used two DC input sources and hence the source detail GUI would be having two input fields as shown in Fig. 6.3a.

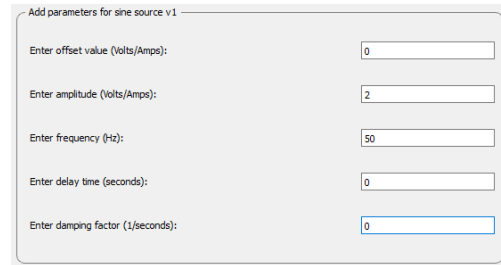
In the current example of the RC circuit, we have a single AC source. Fill in the details as shown in Fig. 6.3b.

6.1.3 Ngspice Model

The component libraries for components like DAC, ADC, transformer etc. which are used in the schematic are directly linked with the corresponding Ngspice models. The



(a) Source Details of Half-Adder



(b) Source Details of RC circuit

Figure 6.3: Source details interface

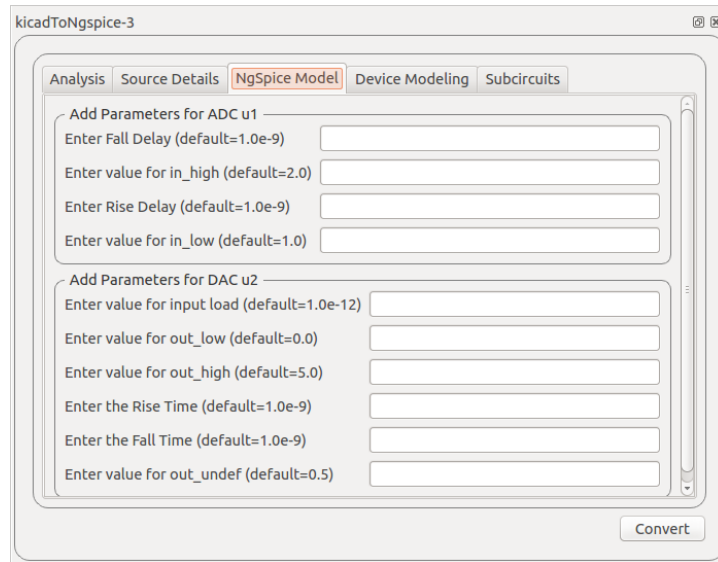


Figure 6.4: Half adder: Ngspice model

user can modify the parameter values using this tab, as shown in Fig. 6.4. If there are no modifications the default values are taken.

6.1.4 Device Modelling

Spice based simulators include a feature which allows accurate modeling of semiconductor devices such as diodes, transistors etc. Model libraries holds these features to define models for devices such as diodes, MOSFET, BJT, JFET, IGBT, Magnetic core etc.

The fields in this tab are added for each such device in the circuit and the corresponding model library is added. In the example of bridge rectifier as shown in Fig. 6.5a

for four diodes library files are added as in Fig. 6.5b. If you do not add any library it will take default Ngspice model for diode.

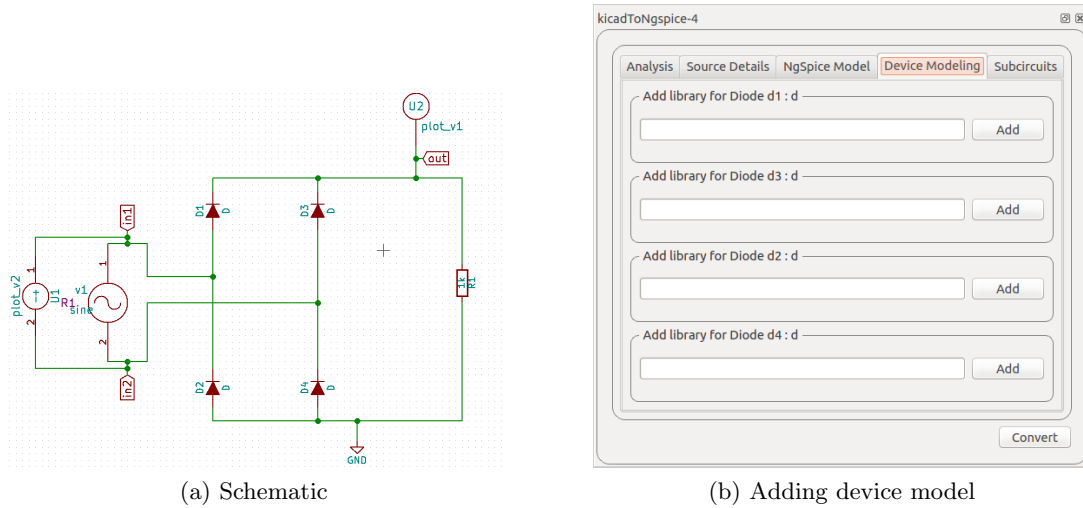


Figure 6.5: Bridge Rectifier

6.1.5 Sub Circuit

Subcircuit is a way to implement hierarchical modeling. Once a subcircuit for a component is created, it can be used in other circuits.

After Filling up the values in all the above mentioned fields the convert button is pressed. The Ngspice netlist, `.cir.out` file is generated. A message box pops up, as shown in Fig. 6.6. Click on OK.

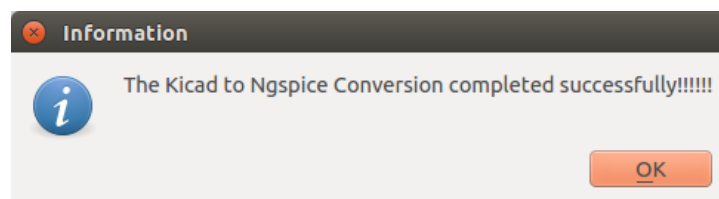


Figure 6.6: Message after successful Ngspice netlist generation

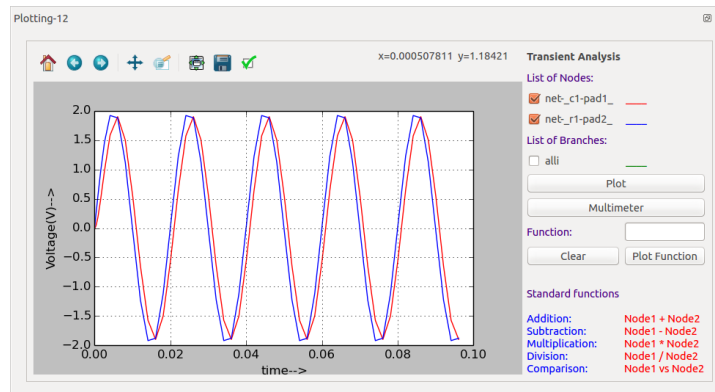


Figure 6.7: Pythonplot for RC circuit

6.2 Simulating the schematic

6.2.1 Simulation

Once the Kicad to Ngspice conversion is successfully completed, press the *Simulation* button on the leftside toolbar on eSim interface. This will display the Python plot window along with the node names. Select the required nodes and click on **Plot**. The simulations are displayed. In the present example of the RC circuit, the plot will be displayed as shown in Fig. 6.7. By changing the values of capacitor and resistor, the output can be varied. We can also use the option **Function** from the right side of the python plot window to plot combination of waveforms for example `plot V1+V2`.

Pressing the *Simulation* button also opens up the Ngspice terminal and plot windows. The Ngspice plots for all the nodes (where we have used the plot components in the schematic) will be displayed. In the current example, we have used two plot components and the Ngspice simulations for these two nodes are displayed as in Fig. 6.8.

If the *Plot components* are not used in the schematic, the simulations are not displayed automatically. To see the Ngspice simulations, type the following commands in the Ngspice terminal window.

- `plot allv` - Plots all the voltage waveforms.
- `plot v(node-name)` - Plot a waveform of the node-name voltage source.
- `plot alli` - Plots all the current waveforms.

You can refer the ngspice commands from <https://esim.fossee.in/ngspiccmd>

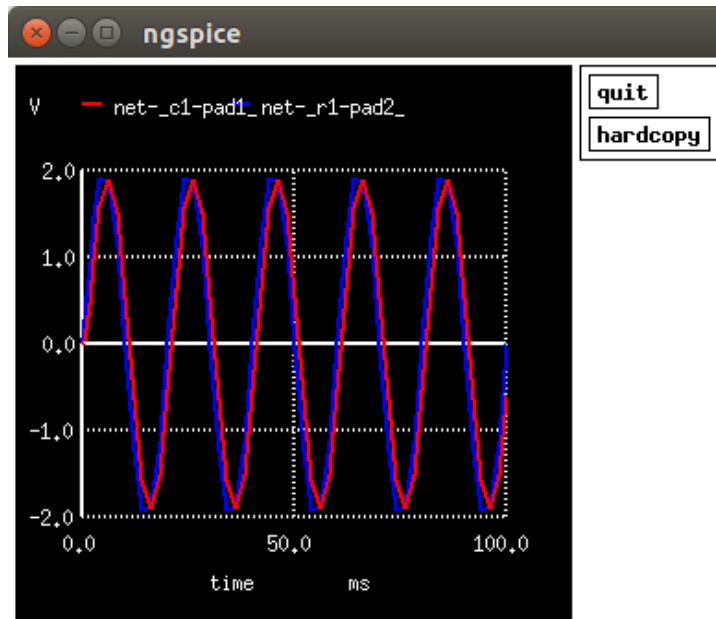


Figure 6.8: Ngspice voltage simulation for RC circuit

6.2.2 Multimeter

Multimeter is another feature that is available in eSim. Using this facility the user can view the voltage and current values in various nodes and branches respectively. To use the multimeter select the required nodes from the plot window and press **Multimeter** button, shown in Fig. 6.9. Windows equal to the number of selected nodes will open. Now open the schematic window and place these pop up windows near the appropriate nodes on the schematic to get the voltage of each node. Similarly current through each branches in the schematic can also be found using the multimeter facility.

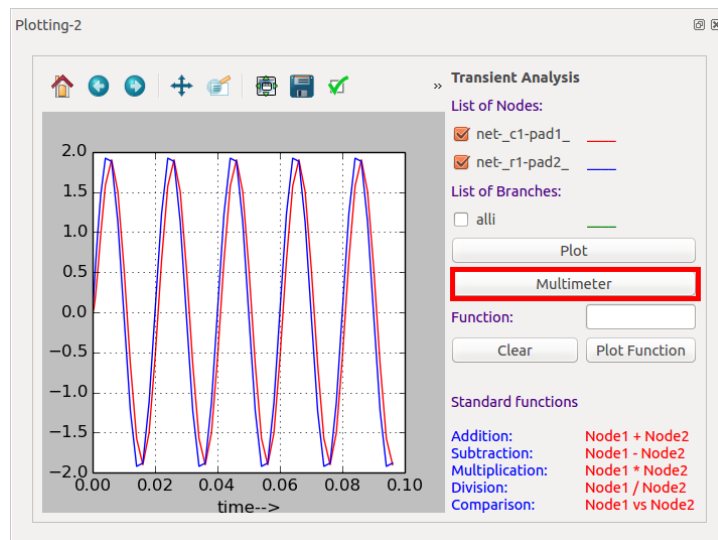


Figure 6.9: Multimeter feature in eSim

Chapter 7

Model Editor

Spice based simulators include a feature which allows accurate modeling of semiconductor devices such as diodes, transistors etc. eSim Model Editor provides a facility to define a new model for devices such as *diodes*, *MOSFET*, *BJT*, *JFET*, *IGBT*, *Magnetic core* etc. Model Editor in eSim lets the user enter the values of parameters depending on the type of device for which a model is required. The parameter values can be obtained from the data-sheet of the device. A newly created model can be exported to the model library and one can import it for different projects, whenever required. Model Editor also provides a facility to edit existing models. The GUI of the model editor is as shown in Fig. 7.1

7.1 Creating New Model Library

eSim lets us create new model libraries based on the template model libraries. On selecting **New** button the window is popped as shown in Fig. 7.2. The name has to be

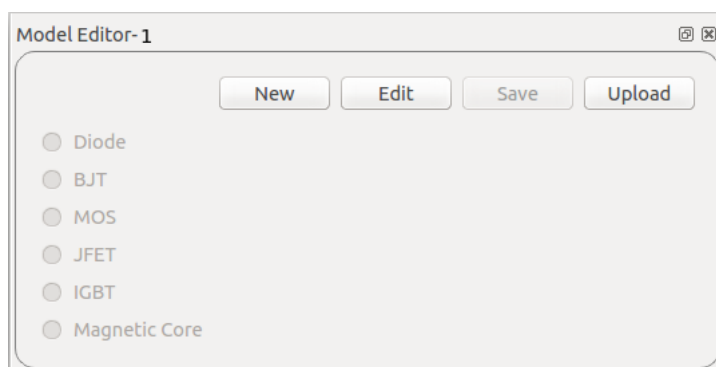


Figure 7.1: Model Editor

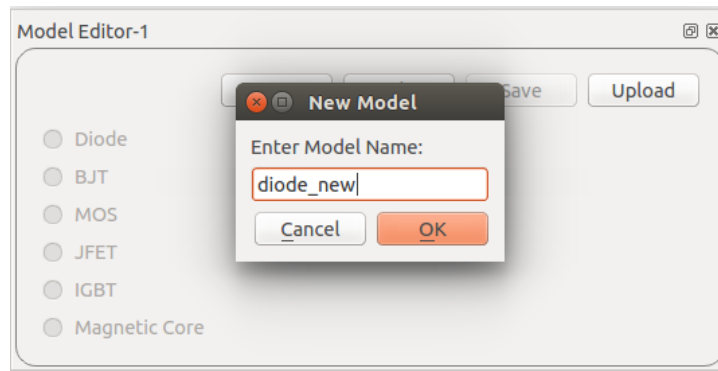


Figure 7.2: Creating New Model Library

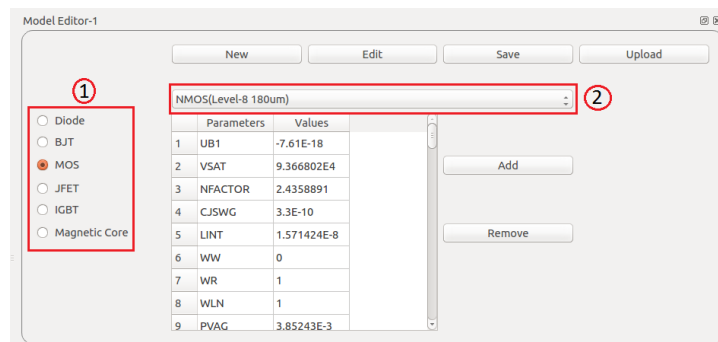


Figure 7.3: Choosing the Template Model Library

unique otherwise the error message appears on the window.

After the OK button is pressed the type of model library to be created is chosen by selecting one of the types on the left hand side i.e. Diode, BJT, MOS, JFET, IGBT, Magnetic Core. The template model library opens up in a tabular form as shown in Fig. 7.3

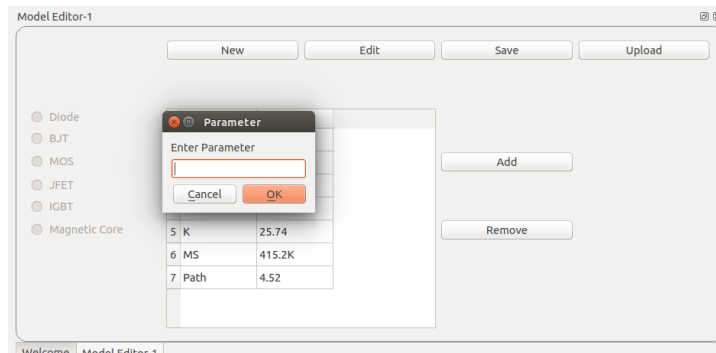


Figure 7.4: Adding the Parameter in a Library

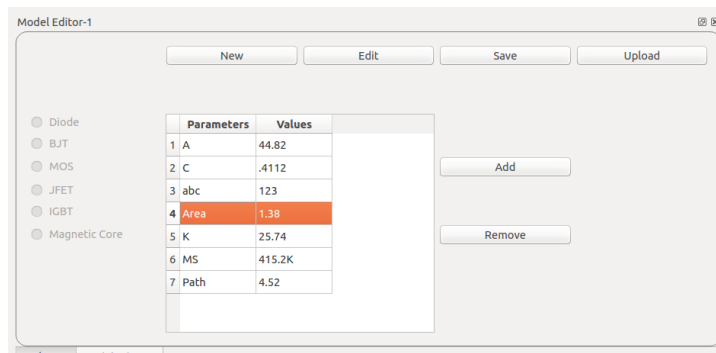


Figure 7.5: Removing a Parameter from a Library

New parameters can be added or current parameters can be removed using **ADD** and **REMOVE** buttons. Also the values of parameters can be changed in the table. Adding and removing the parameters in library files is shown in the Fig. 7.4 and Fig. 7.5

After the editing of the model library is done, the file can be saved by selecting the **SAVE** button. These libraries are saved in the *User Libraries* folder under *deviceModel-Library* directory.

7.2 Editing Current Model Library

The existing model library can be modified using **EDIT** option. On clicking the **EDIT** button the file dialog opens where all the library files are saved as shown in Fig. 7.6. You can select the library you want to edit. Once you are done with the editing, click on **SAVE** button.

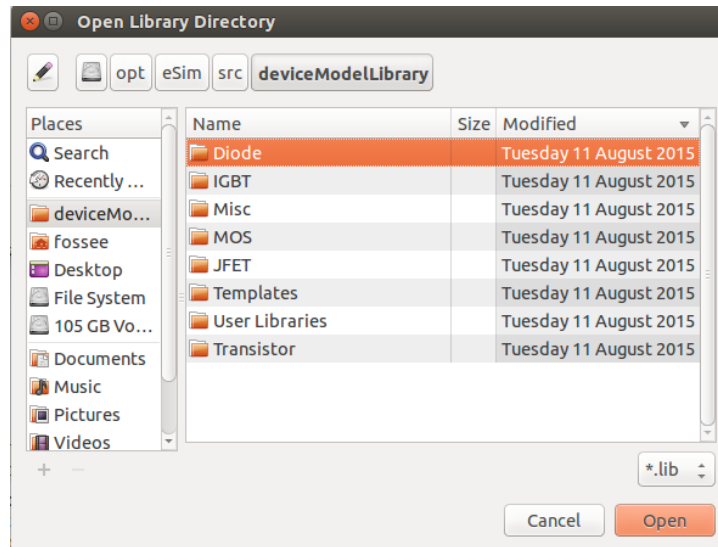


Figure 7.6: Editing Existing Model Library

7.3 Uploading external .lib file to eSim repository

User can also upload external spice **.model** library files. These **.model** libraries can be downloaded online. eSim directly cannot use the external **.lib** file. It has to be uploaded to eSim repository before using it in a circuit. eSim provides the facility to upload library files using the **Upload** option in the *Model Editor*. They are then converted into xml format, which can be easily modified from the eSim interface. On clicking **UPLOAD** button the library can be uploaded from any location. The model library will be saved with the name you have provided, in the *User Libraries* folder of repository *deviceModelLibrary*. Example: You can download any model of Schottky diode from Spice website and save it as **.lib** extension on the system. Click on **UPLOAD** option and give the path. The lib file along with XML file is created in the `eSim-1.1.3/src/deviceModelLibrary/UserLibraries`. The uploaded library can be used for the existing part eSim_Diode or the user can create a new model(part). Refer Chapter 8 on how to create a new part library model in eSim.

Chapter 8

SubCircuit Builder

Subcircuit is a way to implement hierarchical modeling. Once a subcircuit for a component is created, it can be used in other circuits. eSim provides an easy way to create a subcircuit. The following Fig. 8.1 shows the window that is opened when the SubCircuit tool is chosen from the toolbar.

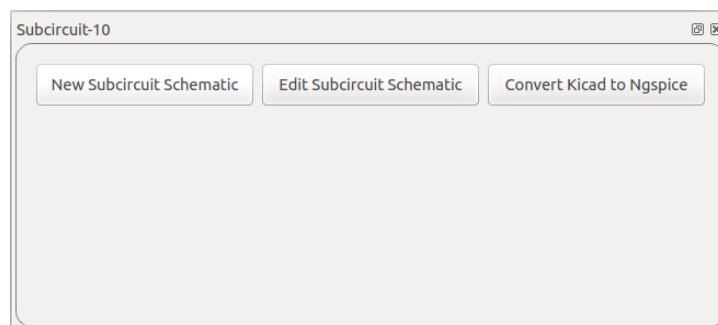


Figure 8.1: Subcircuit Window

8.1 Creating a SubCircuit

The steps to create subcircuit are as follows.

- After opening the Subcircuit tool, click on **New Subcircuit Schematic** button. It will ask the name of the subcircuit. Enter the name of subcircuit (without any spaces) and click **OK** as shown in Fig. 8.2.
- After clicking **OK** button it will open KiCad schematic. Draw your circuit which will be later used as a subcircuit. e.g the Fig. 8.3 shows the half adder circuit.

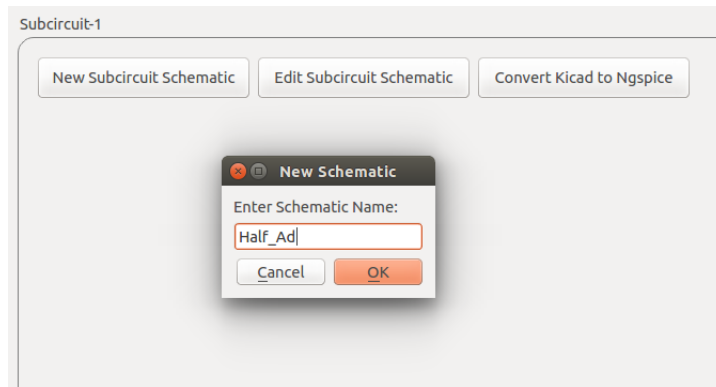


Figure 8.2: New Sub circuit Window

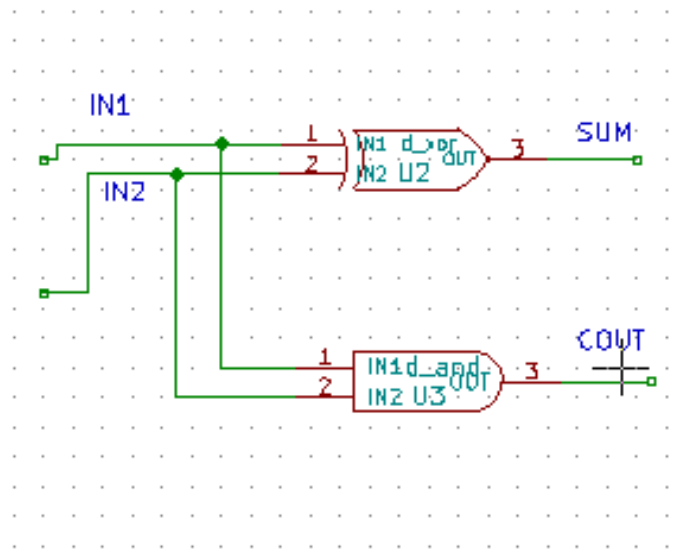


Figure 8.3: New Sub circuit Window

- Once you complete the circuit, assign port to each open node of your circuit which will be used to connect with the main circuit. The port should match with the number of input and output pin. The circuit will look like Fig. 8.4 after adding PORT to it. The PORT symbol can be found in Eeschema as shown in Fig. 8.5.
- Next step is to save the schematic and generate KiCad netlist as explained in Chapter 5.
- To use this as a subcircuit, create a block in KiCad Eeschema by following steps

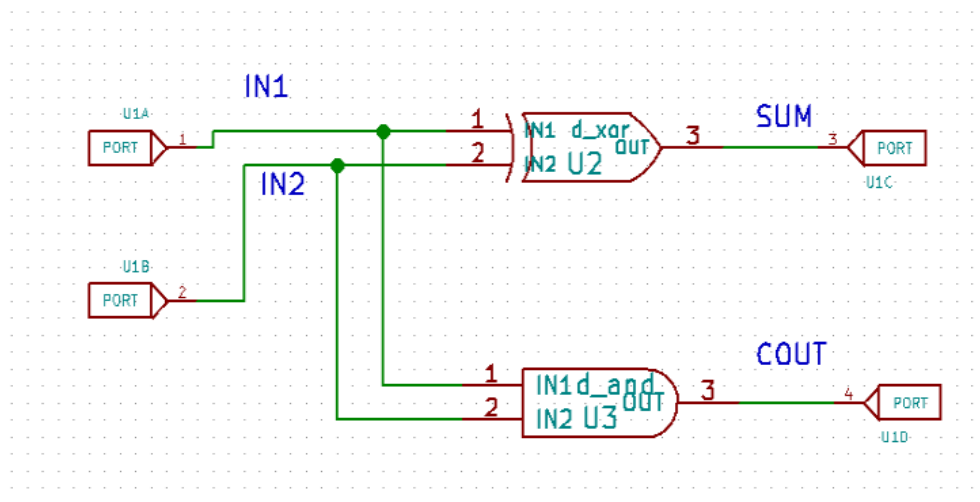


Figure 8.4: Half-Adder Subcircuit

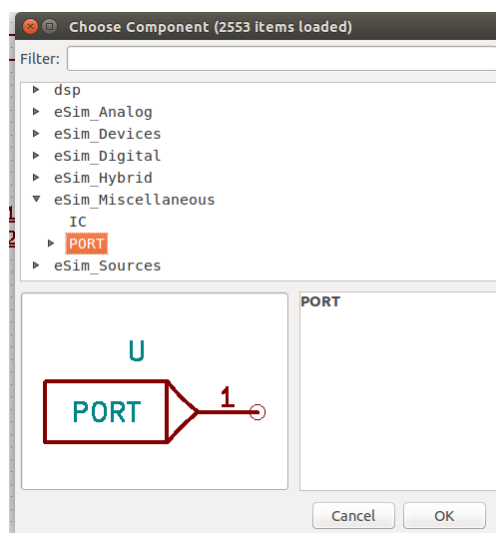


Figure 8.5: Selection of PORT component

given below:

1. Go to library browser of Eeschema. It is an open book icon on the top toolbar.
2. Select the Current Library as eSim_Subckt shown in Fig. 8.6 from the eSim-1.1.3/KicadSchematics. You can also select eSim_Subckt from default path but most of the time the changes are not reflected as it is *read-only* file.

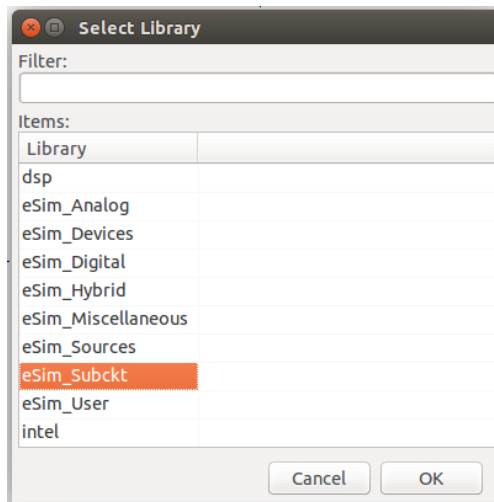


Figure 8.6: Selecting Working Library

3. Click on create a new component from the top toolbar with reference X as shown in Fig. 8.7. The reference X is for subckt, D is for diode, Q is for transistors, J is for FET. The user needs to choose the appropriate reference based on the library in which the model is to be added.

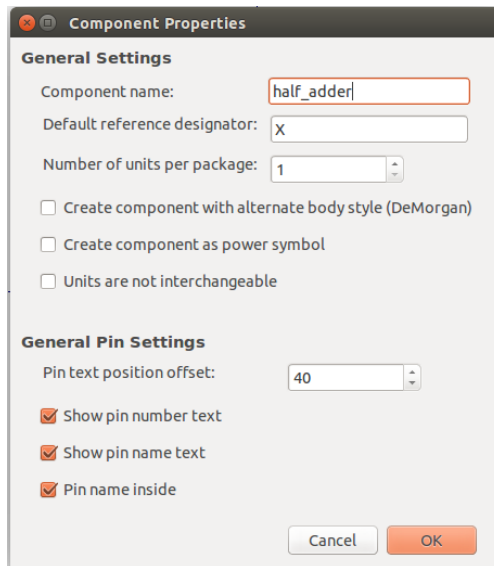


Figure 8.7: Creating New Component

4. Start drawing the subcircuit block by using the drawing tools from the right

taskbar. Here we have used `Add graphic rectangle` to component body. You can start drawing with a point to point click on the editor.

- To add pins select `Add pins to components` from the right taskbar. Give the `Pin Name` as `IN1` and `Pin Number` as `1`. The pin number has to match with the `Port name`. Example `Port A` is mapped to pin `1`. Select the `Orientation` as right or left accordingly. The `Electrical Type` has to be chosen as `Input`. Note here if user wants to build the subcircuit using `Transistor` then the electrical type should be `Open Emitter` and `Open Collector` for emitter and collector pins and the base can be `Passive`. Refer Appendix for further information on `Pin Types`.
- Update and save using `Update Current` component from the top toolbar as shown in Fig. 8.8.

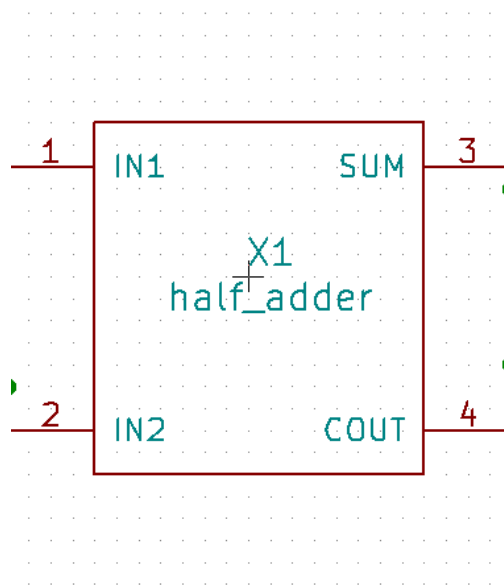


Figure 8.8: Half-Adder Subcircuit Block

- Close the Eeschema window and click on `Convert KiCad to Ngspice` button in `subcircuit builder tool`. You can assign values in the transient analysis or leave it blank. Add the libraries in case, you have used any `Device Models` or `Sub-circuits`. This will convert the KiCad spice netlist to Ngspice netlist. And it will save your subcircuit into eSim repository, which you can add in your main circuit. You can see the subcircuit library is added in the `subcircuit` folder of eSim. The newly added part (model) library is added in the `KicadSchematicLibrary` under `eSim Subckt` of eSim repository.

8.2 Edit a Subcircuit

The steps to edit a subcircuit are as follows.

- After opening the Subcircuit tool, click on **Edit Subcircuit Schematic** button. It will open a dialog box where you can select any subcircuit for editing.
- After selecting the subcircuit it will open it in KiCad Eeschema, where you can edit the subcircuit.
- Next step is to save the schematic and generate KiCad netlist.
- If you have edited the number of ports then you have to change the block in KiCad Eeschema accordingly.
- Close the Eeschema window and click on **Convert KiCad to Ngspice** button in subcircuit builder tool to convert the edited subcircuit KiCad netlist into Ngspice netlist. You can also refer the subcircuit examples at [eSim-1.1.3/src/subcircuitlibrary/](https://github.com/eSim-1.1.3/src/subcircuitlibrary/)

Note:

- User can also import or append the schematic of different projects in the current page using the *Append Schematic Sheet* from the *File* menu. This will import(copy) the schematic that user has defined to the current schematic editor page.
- User can also import the model in the part library editor page using the option *Import Component* from the top toolbar.

Chapter 9

NGHDL-Mixed mode simulation

NGHDL feature facilitates creation of user-defined models for mixed-mode circuit simulation in eSim. By interfacing GHDL and Ngspice, we achieve mixed-mode simulation. Digital models are simulated using GHDL and XSPICE engine of Ngspice.

9.1 Introduction

Ngspice supports mixed mode simulation, i.e. it can simulate both digital and analog component. It defines a `model` which has the functionality of the circuit component, which can be used in the netlist. For example you can create an `adder` model in Ngspice and use it in any circuit netlist of Ngspice.

However, it is not feasible to define complex digital models without a complete understanding of Ngspice and XSPICE architectures and is a time-consuming process. Also, most of the users are familiar with GHDL and can write the models using VHDL code with ease. Hence, NGHDL provides an interface to write VHDL code for a digital model and install it as model in Ngspice. So whenever Ngspice looks for that model, it will actually interface with VHDL code to get the result.

Fig. 9.1 shows the overview of NGHDL indicating its architecture at the abstract level. The values for the digital models present in the netlist are fetched from the GHDL side of the interface whereas the values of the analog part are fetched from Ngspice's spice3f5 engine. Digital and Analog components in Fig. 9.1 are connected to each other with the help of the hybrid ADC and DAC models provided by Ngspice. This helps in the signal level switching when simulation is performed. As analog signals are in continuous time domain and Digital signals are in discrete time domain, hybrid components help bridge the gap. More information on the parameters of ADC and DAC present in Appendix : D.

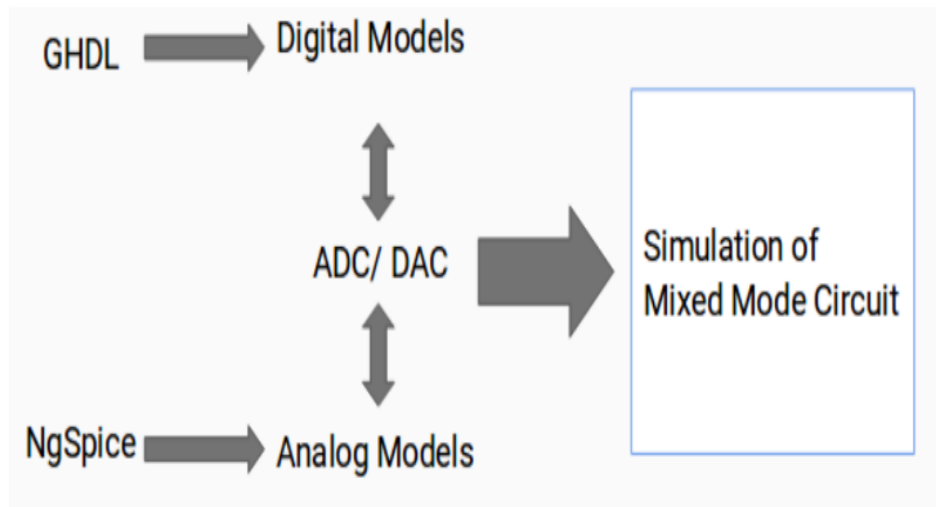


Figure 9.1: Overview of NGHDL

9.2 Digital Model creation using NGHDL

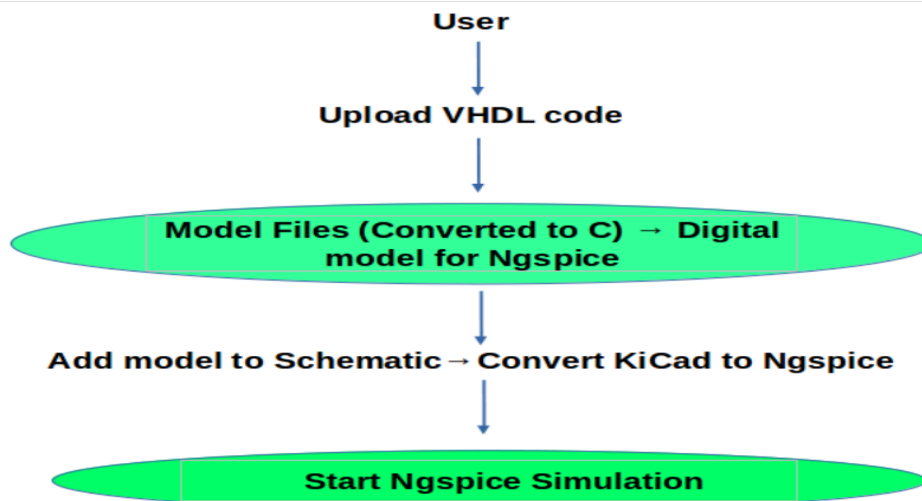


Figure 9.2: User Flow for NGHDL

The steps to create digital models are given below:

1. Click on NGHDL button on left side pane of main window, the Ngspice Digital Model Creator window will appear as shown in Fig. 9.3

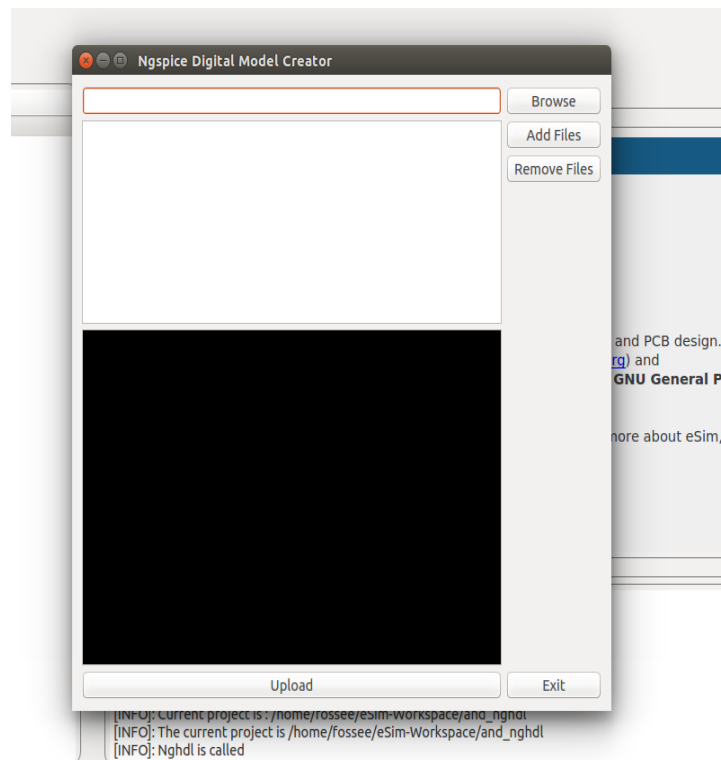


Figure 9.3: NGHDL interface

2. Now browse and locate the VHDL file to upload. Select the VHDL file and click on the Upload button. This process will create Ngspice model and corresponding component drawing inside the KiCad library (eSim_Nghdl.lib) of the VHDL block to be used in mixed-mode simulations. An acknowledgement message will appear upon successful processing of the VHDL code as shown in Fig. 9.4.

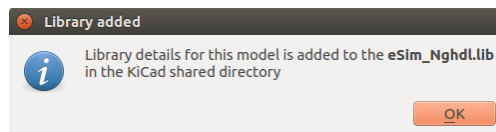


Figure 9.4: Uploading of digital model

Note : "Add files" option allow you to use a smaller entity / subpart / submodule to support the main VHDL file. That is, a digital model will be generated corresponding to that file that has been browsed. The file that has been "added" to Nghdl upload window will only be placed along with the model under model's

DUTghdl folder to support the model.

Hence, "browsing" one file and "adding" several files won't create that many number of models, but only one model will be created corresponding to the browsed file.

9.3 Schematic Creation

Steps for schematic creation are as follows:

1. Click on New Project icon to create a new project as shown in Fig. 9.5, be careful of the naming conventions.



Figure 9.5: Creation of a new project

2. After successful upload of the model using the VHDL code, you can create the schematic of your design by clicking on **Open Schematic** button on the left pane of the eSim window. Then go to **Preferences** option on top of the schematic editor window and click on **Component Libraries** to add the library eSim_Nghdl.lib in KiCad. Following window will appear as shown in Fig. 9.6, where you will have to click on **Add** button and select the eSim.Nghdl library. Refer Fig. 9.6 and Fig. 9.7.

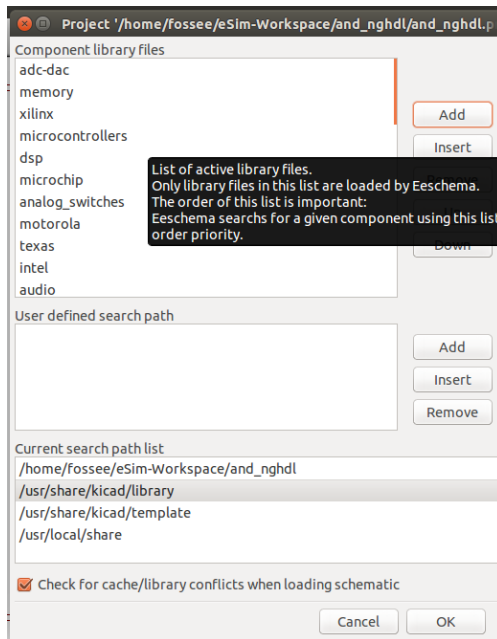


Figure 9.6: Adding the digital model library in KiCad

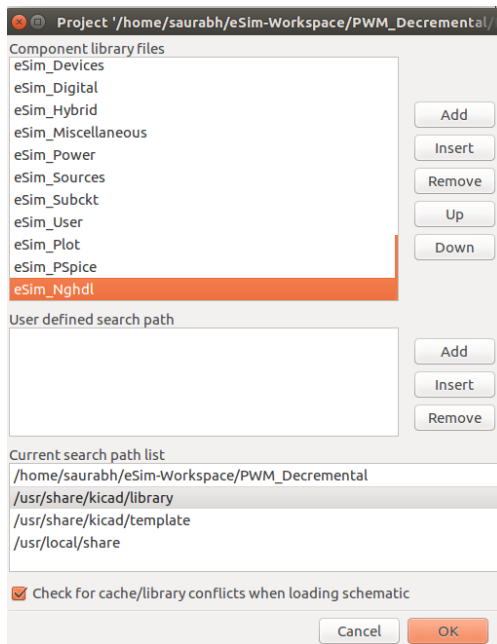


Figure 9.7: Selection of library

3. Next step is to locate the component in eSim_Nghd1 library as shown in Fig. 9.8 and place it on the schematic editor as shown in Fig. 9.9.

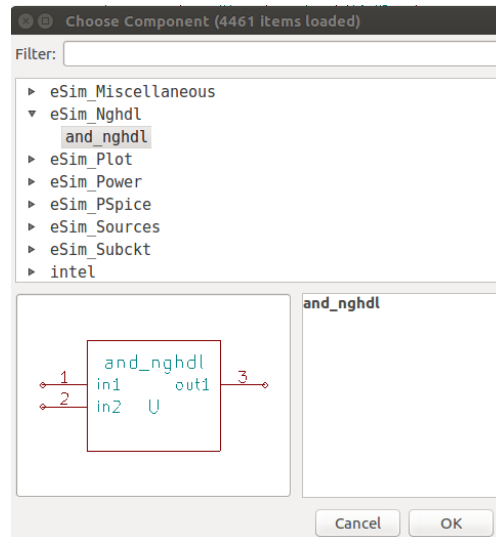


Figure 9.8: Locating the component in library

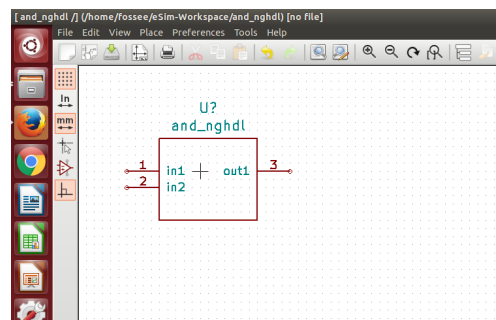


Figure 9.9: Placement of component on editor

- Now create the schematic as shown in Fig. 9.10, annotate, perform ERC, create the netlist and save the schematic by following the steps given in Chapter 5.

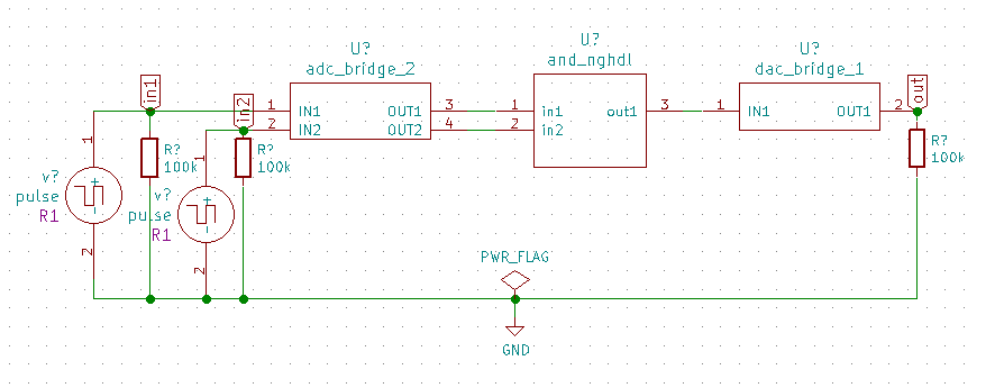


Figure 9.10: Example of an AND gate characteristics circuit

- After creating the schematic, click on **KiCad-to-Ngspice converter** and select the type of analysis as transient as shown in Fig. 9.11 and set the start, step and stop time as shown in Fig. 9.12

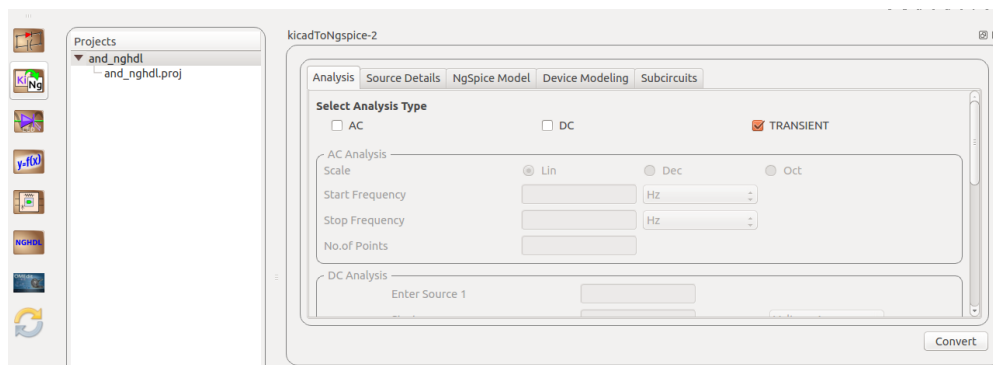


Figure 9.11: Analysis Part I

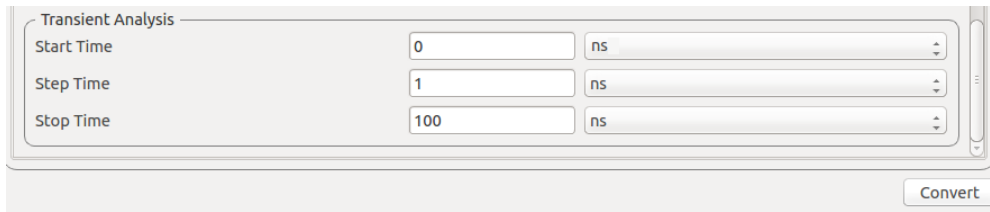


Figure 9.12: Analysis Part II

- Now click on **Source Details** and enter the values for Source v1 and source v2 as shown in figure Fig. 9.13 and Fig. 9.14

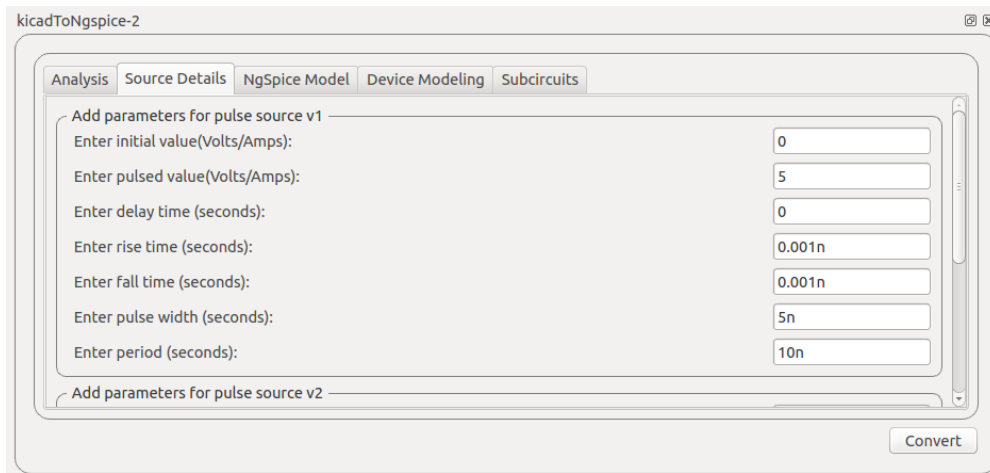


Figure 9.13: Value of Source v1

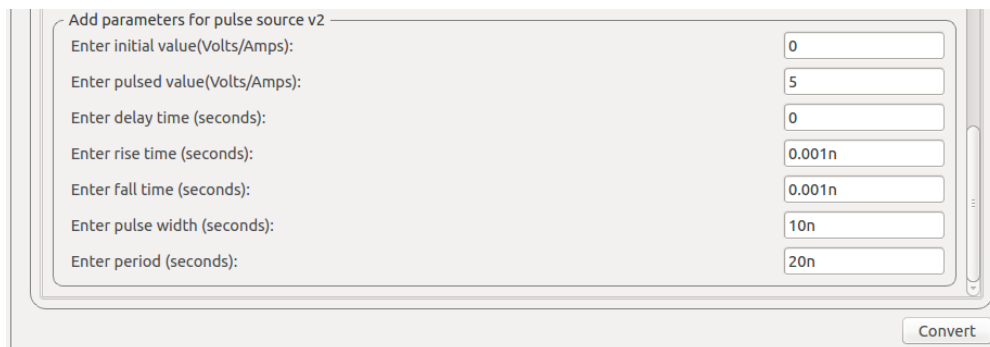
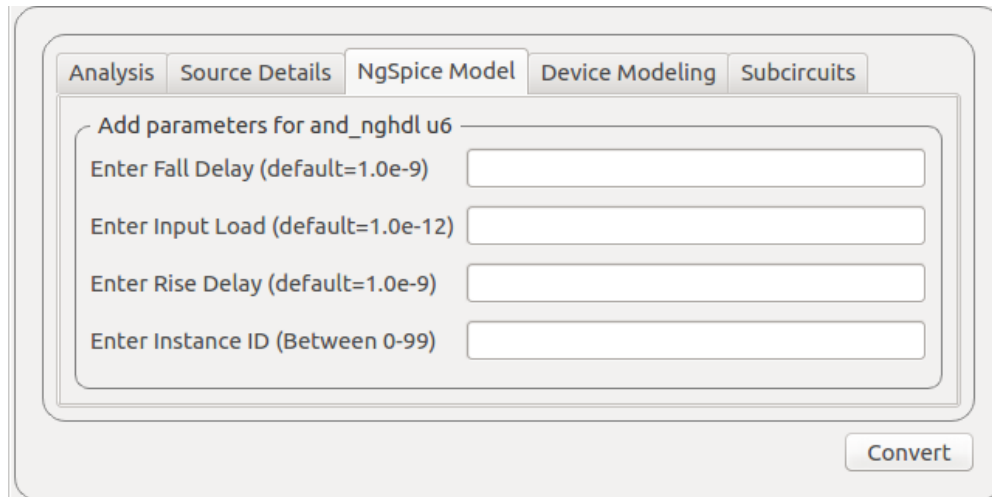


Figure 9.14: Value of Source v2

7. Now select the option **Ngspice Model**, window as shown in Fig. 9.15 will appear. The values of the parameters listed can be changed per user's requirement. If you have used any semiconductor devices and Subcircuits in your design, then please specify the Spice models and subcircuits in the **Device Modeling** and **Subcircuits** tabs of the **KiCad-to-Ngspice converter** window. After that click on **Convert** button. This step will create the simulation compatible netlist.



The image shows a software window titled "NgSpice Model" with five tabs: "Analysis", "Source Details", "NgSpice Model", "Device Modeling", and "Subcircuits". The "NgSpice Model" tab is active and contains a section titled "Add parameters for and_nghdl u6". This section has four input fields with labels: "Enter Fall Delay (default=1.0e-9)", "Enter Input Load (default=1.0e-12)", "Enter Rise Delay (default=1.0e-9)", and "Enter Instance ID (Between 0-99)". A "Convert" button is located at the bottom right of the window.

Figure 9.15: Model Parameters

8. Now click on **Simulation** button, it will display the following windows as shown in Fig. 9.16. This is the Ngspice terminal and Python plot window.

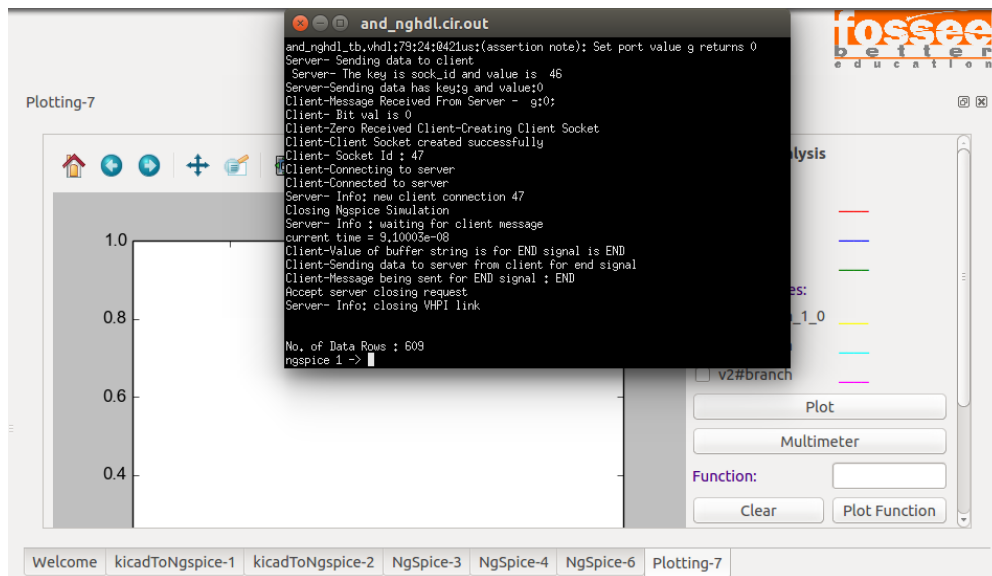


Figure 9.16: Simulation window

- Now select the required nodes and click on Plot button. You can see the plots of input source v1, input source v2 and output as shown in Fig. 9.17, Fig. 9.18, and Fig. 9.19 respectively.

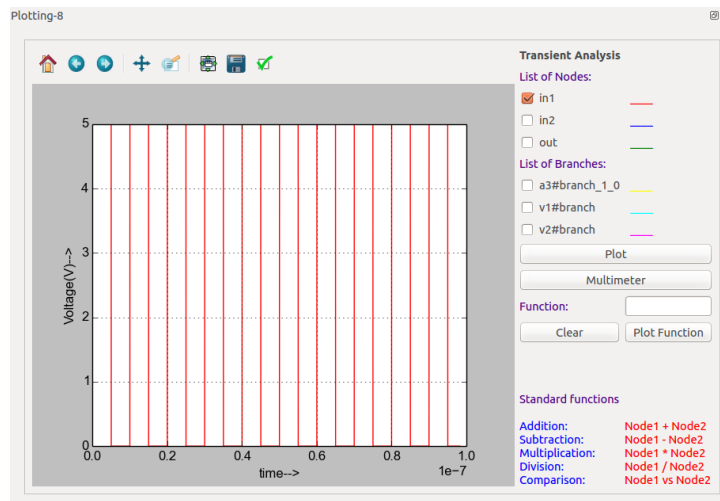


Figure 9.17: Plot of Source V1

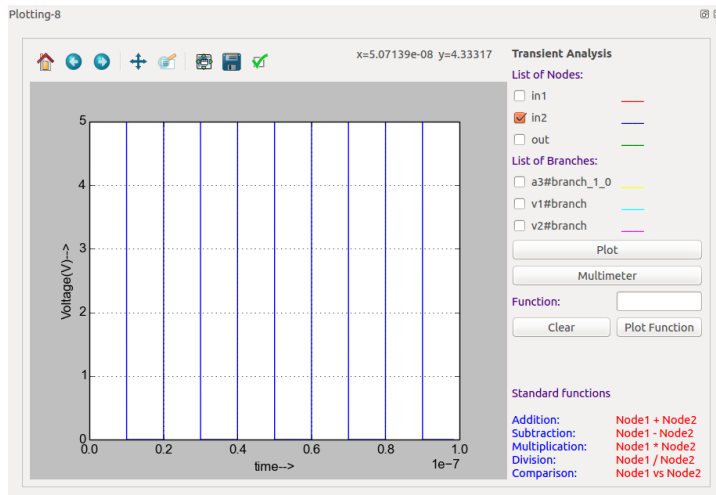


Figure 9.18: Plot of source V2

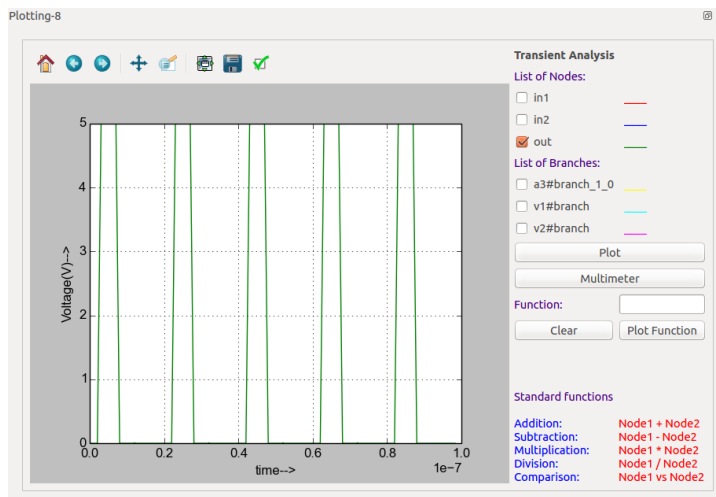


Figure 9.19: Plot of output

Chapter 10

OpenModelica

10.1 Introduction

OpenModelica (OM) is an open source modeling and simulation tool based on Modelica language. Modelica is an object oriented language. As a result, it has all the features of an object oriented language such as inheritance. Models or circuits are defined in the form of classes, with in which there are components, functions, connection and placement information. The OM suite has the following major tools.

10.1.1 OMEdit

An IDE for modeling and simulation. It supports a lot of electrical components. It has a good graphical interface to drag and drop components and create the circuit. One can only do transient simulation using this interface. An attractive feature of OMEdit is the plotting interface. All the parameters in the circuit like voltages and currents through each component, parameters like frequency, delay etc. will be displayed as a list, after simulation. The user can choose the variables to be plotted in an interactive manner from this list. On choosing the variable to plot, it will be plotted on the plot window. One can also create multiple plot windows.

10.1.2 OMOptim

An IDE for optimisation. It lists all the variables in the given model. One can choose the variables to be optimised from the list. Multiple models can be loaded for a given optimisation problem. One can do multi objective optimisations as well. It supports various optimisation algorithms such as Particle Swarm Optimisation (PSO) and Simulated Annealing (SA). The results are displayed graphically.

10.2 OpenModelica in eSim

The above two functionalities can be accessed through the **Modelica Converter** and **OM Optimisation** tools on the eSim left toolbar. The two examples given below illustrates how to use OpenModelica in eSim.

Low Pass Filter circuit

Let us now see how to simulate a low pass filter in OpenModelica.

1. Open the schematic and create the circuit as shown in Fig. 10.1.

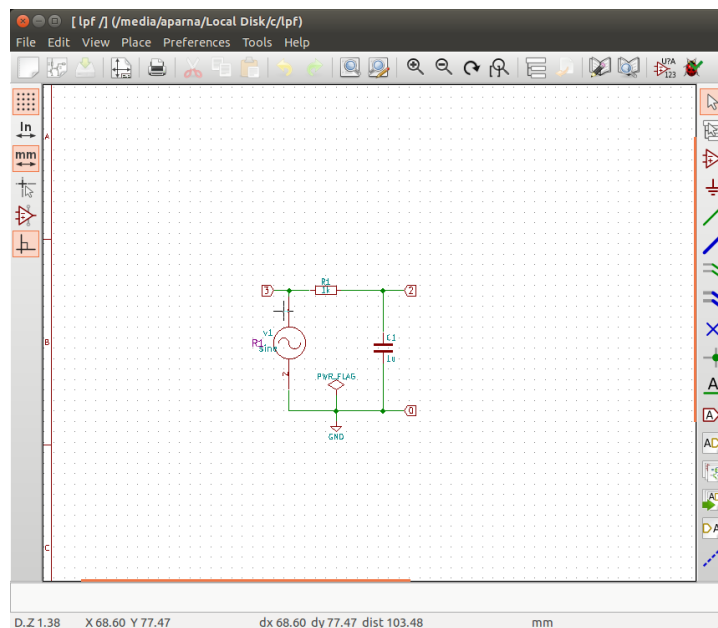


Figure 10.1: Circuit schematic: Low pass filter

2. Create the KiCad netlist. Now the analysis and analysis parameters are given as shown in Fig. 10.2.
3. The source details are given as in Fig. 10.3. The generated KiCad netlist is then converted to ngspice compatible netlist.
4. Simulate the ngspice netlist. The simulation curves are shown in Fig. 10.4.
5. Now to use OpenModelica, click on **Modelica Converter** in the bottom left of eSim left toolbar. Make sure you have OpenModelica installed in the system. This converter converts the spice netlist to Modelica format. Click on the LPF in the

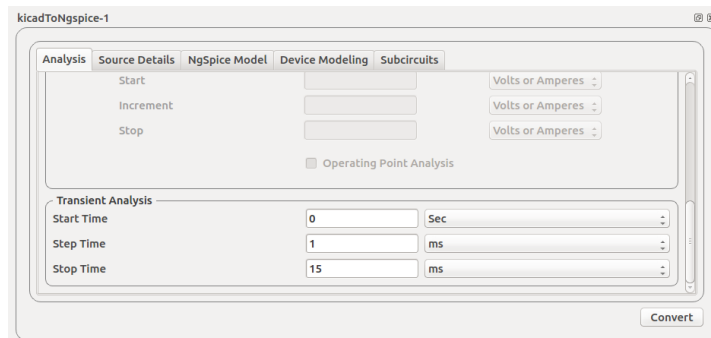


Figure 10.2: Analysis parameters: Low pass filter

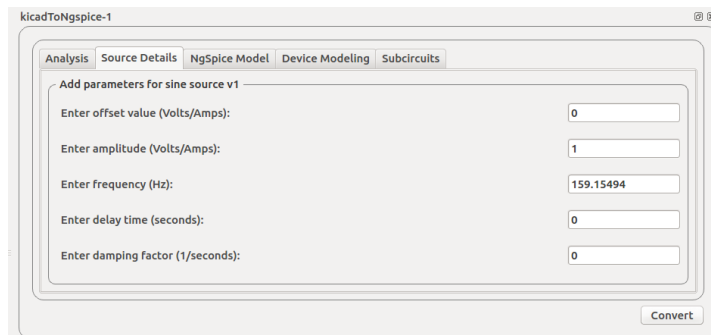


Figure 10.3: Source details: Low pass filter

left that is appended in OpenModelica main window. Make sure you are in text view to see the Modelica code as shown in Fig. 10.5 Figure shows that LPF circuit is being used as a model, the initialisation of sources and components are in the beginning followed by the connection information. n3, n0,n2 are the nodes.

Default Modelica library is used for electrical sources and components. This has to imported so that it can be used in the current circuit. This is available in the left side of main window.

6. Click on Simulation Setup on the toolbar at the top. A window opens as shown in Fig. 10.6. Give start and stop time. Click OK.
7. A plotting window opens. Click on the node at the right to display the waveform. The window is shown in Fig. 10.7.

10.2.1 OM Optimisation

Now let us explore how to use OpenModelica for optimisation through an example. Find the value of resistance R2 that maximises the power dissipated through it for the

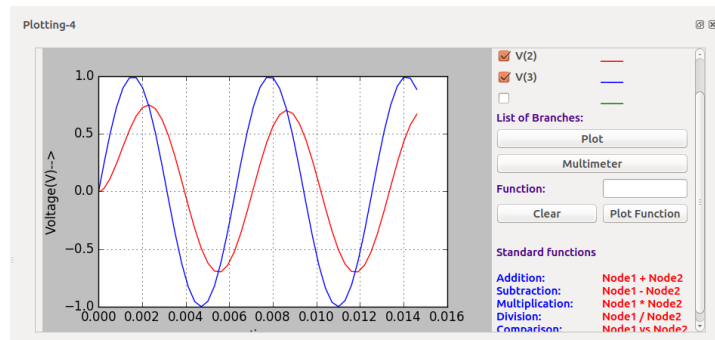


Figure 10.4: Simulation: Low pass filter

```

1 model lpf
2 import Modelica.Electrical.*;
3 Analog.Sources.SineVoltage v1(offset = 0, V = 1, freqHz =
4 159.15494, startTime = 0, phase = 0);
5 Analog.Basic.Resistor r1(R = 1000.0);
6 Analog.Basic.Capacitor c1(C = 1e-006);
7 Analog.Basic.Ground g;
8 protected
9 Modelica.Electrical.Analog.Interfaces.Pin n3,n0,n2;
10 equation
11 connect(v1.p,n3);
12 connect(v1.n,n0);
13 connect(r1.p,n3);
14 connect(r1.n,n2);
15 connect(c1.p,n2);
16 connect(c1.n,n0);
17 connect(g.p,n0);
18 end lpf;

```

Messages Browser
sh: 1: impact: not found

[1] 21:21:16 Translation Warning
Assuming fixed start value for the following 1 variables:
c1.v:VARIABLE(start = 0.0 unit = "V") "Voltage drop between the two pins (= p.v - n.v)" type: Real

Figure 10.5: OpenModelica: Text view

circuit in Fig. 10.8. This is an illustration of the Maximum Power Transfer Theorem. The power is maximum when $R_2 = R_1$, i.e., when $R_2 = 100$. So maximum power would be $P_{max} = 0.0625$. Let us now see the steps to be followed find the value of R_2 using eSim.

1. Follow all the steps as above and generate the Modelica model using the Ngspice to Modelica converter.
2. The objective function is $Power = i^2 \times R_2$. To define the objective function, the line $power := i^2 \times R_1 + i^2 \times R_2$ is added under the keyword algorithm, in the

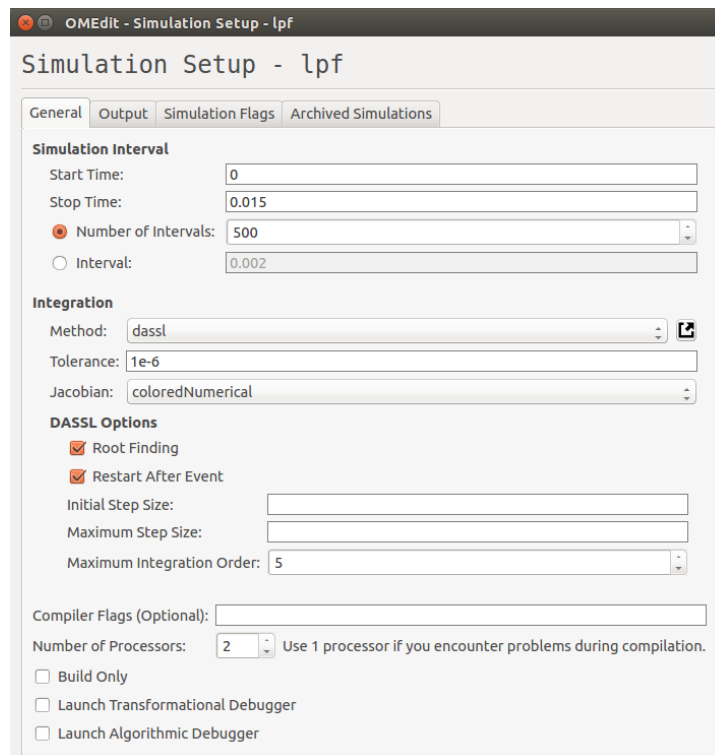


Figure 10.6: OpenModelica: Simulation setup

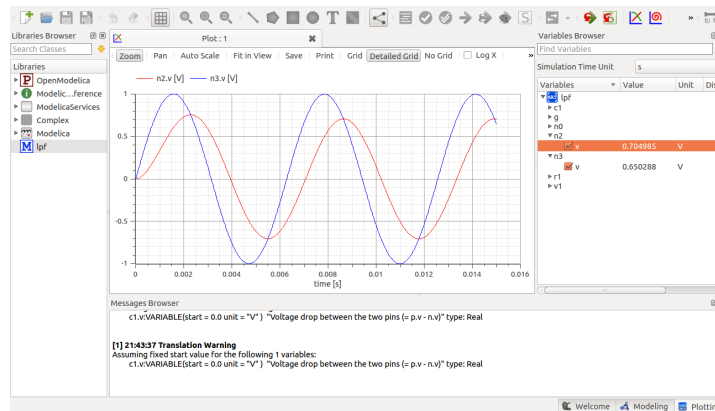


Figure 10.7: OpenModelica: Simulation

Modelica model file.

3. Select OMOptim from eSim left toolbar, in the displayed window click on New

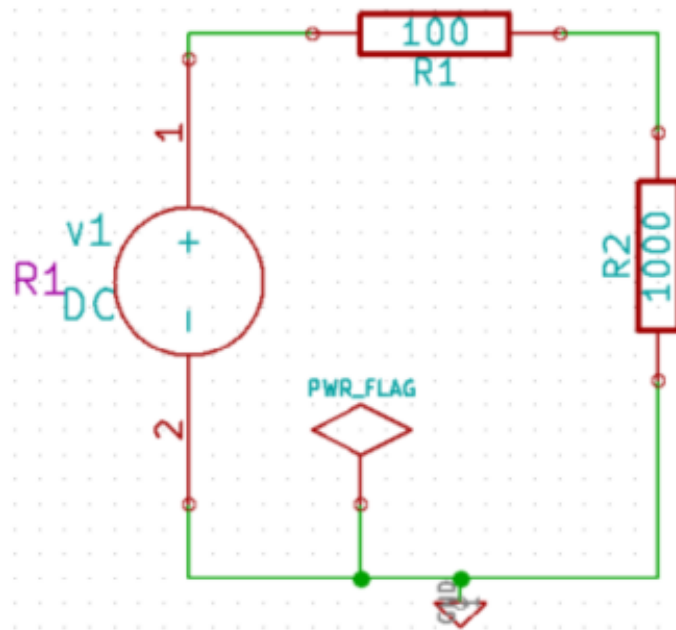


Figure 10.8: Circuit schematic for optimisation

Project. Then save the project. It is stored with an extension `.min`. Now select **Models** and then **Load Modelica Library**. Now select **Load mo file** under **Models**. It will be added on the left.

4. Click **Problems** and then **Optimisation**. Select the model to be optimised. *Note that for optimising, that model has to be loaded in OpenModelica as stated before.* Clicking blue turnover icon will display all the variables used in the model. Add details like optimisation variables and objective.

The OMOptim project for this problem is given in Fig. 10.9. Power is the objective function that has to be maximized. `r2.R` is the variable that will be varied. `r2.R` is limited between 0 and 1000.

5. Click on **Parameters** tab to select the type of algorithm and its parameters. In this example, the optimisation algorithm used is PSO (Particle Swarm Optimisation). The various parameter values given are as follows: population size as 50, Inertia factor as 1, Learning factor: alpha and beta as 2, Population saving frequency was 1. Iteration limit is also specified. Select the `.mo` file to be simulated from **Files** tab. Click on **Launch**. The results of optimisation for various values of Iteration Limit are given in Fig. 10.10.

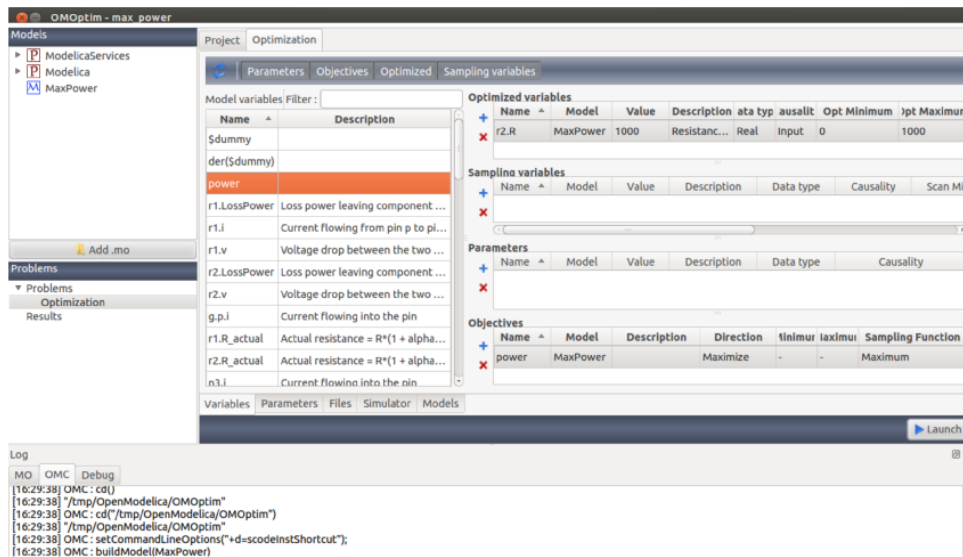


Figure 10.9: OMOptim project

Iteration Limit	$R_2(\Omega)$	Power (W)
100	102.652	0.0624893
200	99.9942	0.0625
300	99.9221	0.0625
400	98.6115	0.0624969
500	99.9923	0.0625
600	100.968	0.0624985
700	100.648	0.0624993

Figure 10.10: Optimisation values for various Iteration Limit

- Depending on the type of algorithm, the time for optimisation varies. Optimised result is graphically displayed as shown in Fig. 10.11.

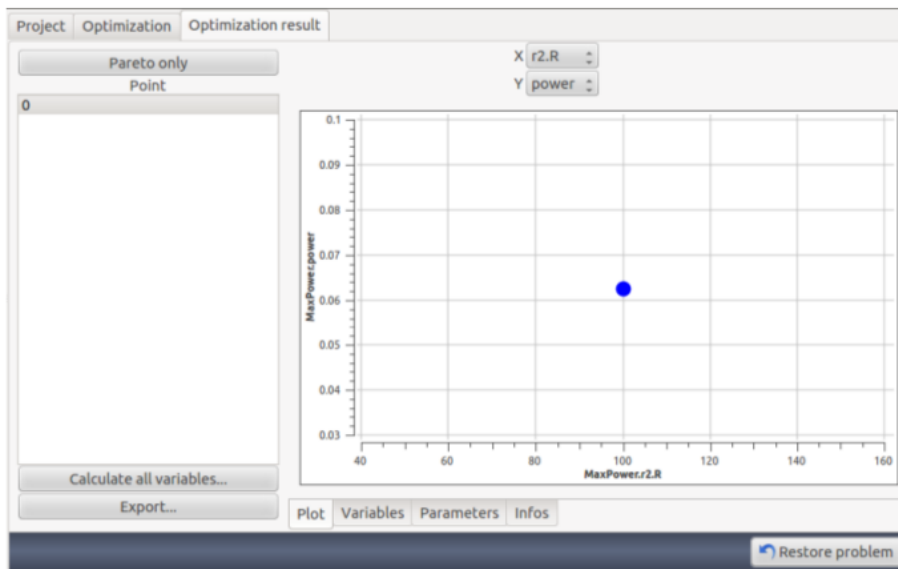


Figure 10.11: Optimised value of resistance for maximum power

Chapter 11

Solved Examples

11.1 Solved Examples

11.1.1 Basic RC Circuit

Problem Statement:

Plot the Input and Output Waveform of an RC circuit whose input voltage (V_s) is 50Hz, 3V peak to peak. The values of Resistor (R) and Capacitor(C) are $1k$ and $1\mu f$ respectively.

Solution:

- Creating a Project: The new project is created by clicking the **New** icon on the menubar. The name of the project is given in the pop up window as shown in Fig. 11.1.
- Creating the Schematic: To create the schematic, click the very first icon of the left toolbar as shown in the Fig. 11.2. This will open KiCad Eeschema.

To create a schematic in KiCad, we need to place the required components. Fig. 11.3 shows the icon on the right toolbar which opens the component library.

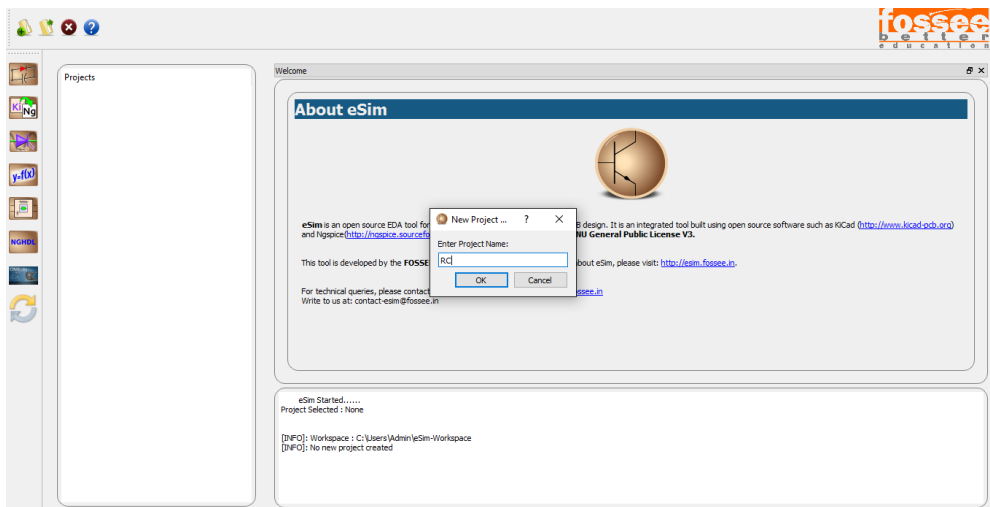


Figure 11.1: Creating New Project

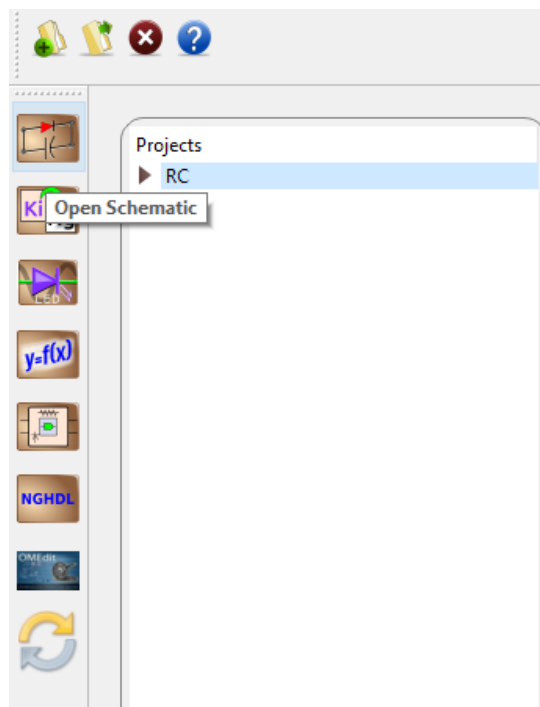


Figure 11.2: Open Schematic Editor

After all the required components of the simple RC circuit are placed, wiring is done using the Place Wire option as shown in the Fig. 11.4

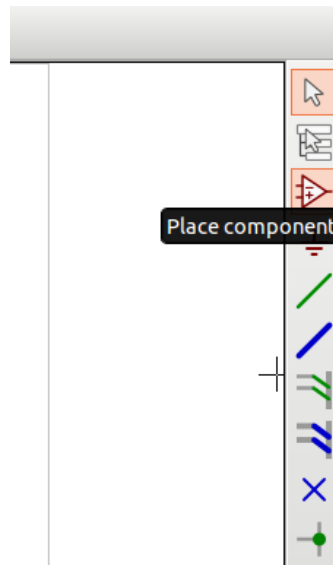


Figure 11.3: Place Component Icon

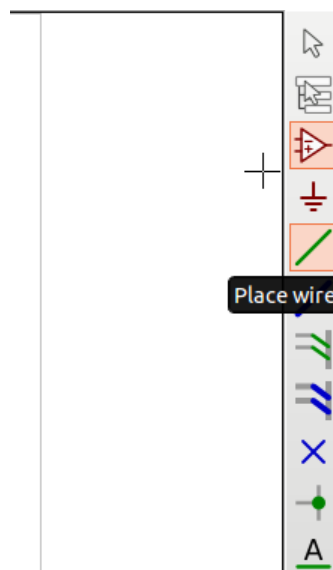


Figure 11.4: Place Wire Icon

Next step is ERC (Electric Rules Check). Fig. 11.5 shows the icon for ERC. Fig. 11.6 shows the RC circuit after connecting the components by wire.

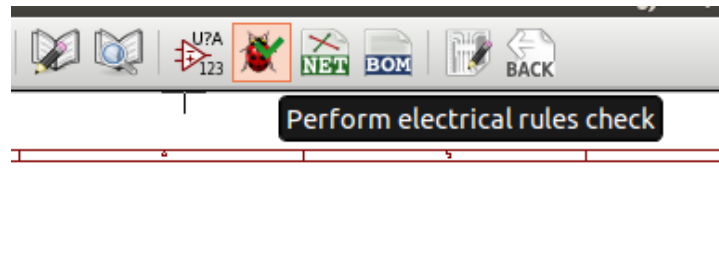


Figure 11.5: Electric Rules Check Icon

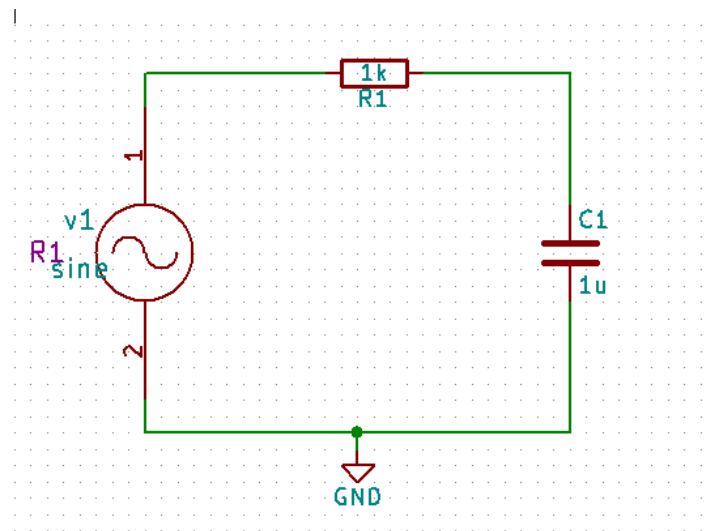
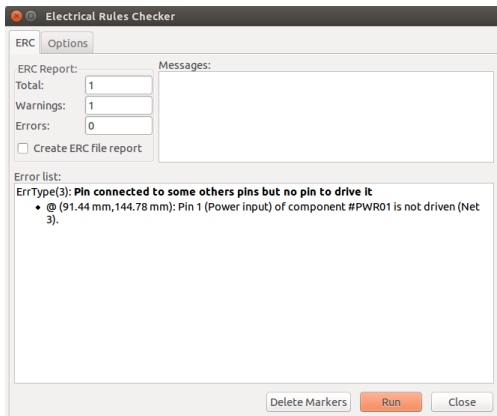


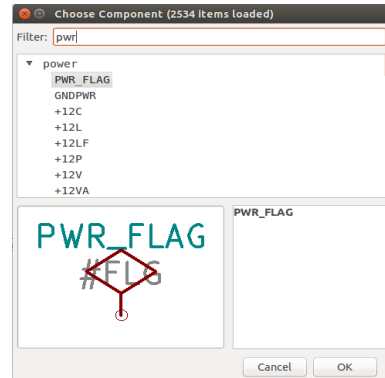
Figure 11.6: RC circuit

After clicking the ERC icon a window opens up. Click the Run button to run rules check. The errors are listed in as shown in Fig. 11.7a. This error is handled by adding Power Flag as shown in Fig. 11.7b.

After adding the Power Flag the completed RC circuit is shown in Fig. 11.8a and the netlist is generated as shown in Fig. 11.8b.

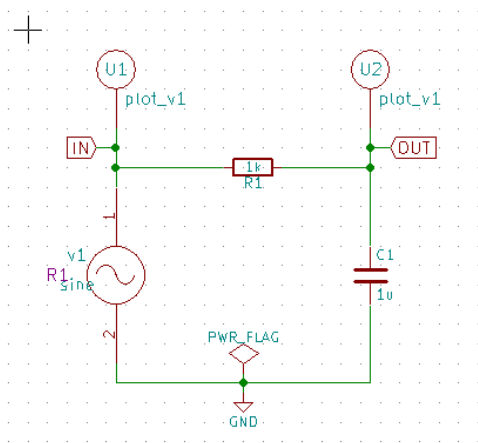


(a) ERC Run

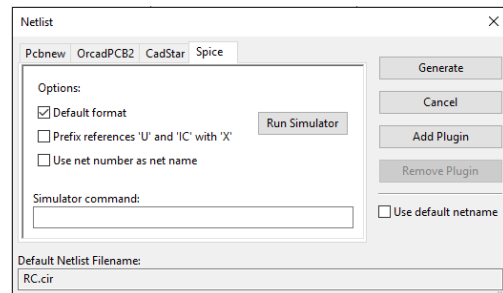


(b) Power Flag

Figure 11.7: ERC check and POWER FLAG



(a) Schematic of RC circuit



(b) Generating KiCad Netlist of RC circuit

Figure 11.8: RC Schematic and Netlist Generation

- Convert KiCad to Ngspice: To convert KiCad netlist of RC circuit to NgSpice compatible netlist click on KiCad to Ngspice icon as shown in Fig. 11.9.

Now you can enter the type of analysis and source details as shown in Fig. 11.10a and Fig. 11.10b respectively.

The other tab will be empty as RC circuit do not use any Ngspice model, device library and subcircuit.

After entering the value, press the convert button. It will convert the netlist into Ngspice compatible netlist.

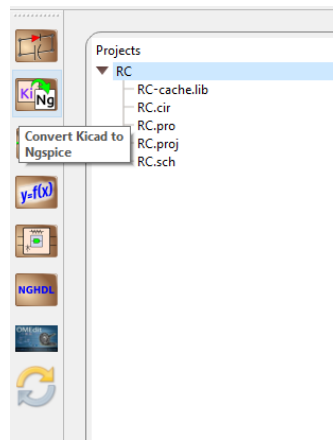
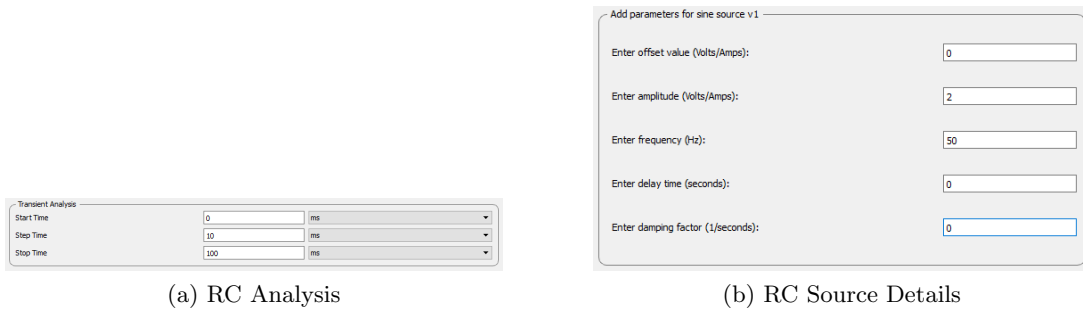


Figure 11.9: Convert KiCad to Ngspice Icon



(a) RC Analysis

(b) RC Source Details

Figure 11.10: RC Analysis and Source Detail

- **Simulation:** To run Ngspice simulation click the simulation icon in the tool bar as shown in the Fig. 11.11.

In eSim, there are two types of plot. First is normal Ngspice plot and second is interactive python plot as shown in Fig. 11.12a and Fig. 11.12b respectively.

In the interactive python plot you can select any node or branch to plot voltage or current across it. Also it has the facility to plot basic functions across the node like addition, subtraction, multiplication, division and v/s.

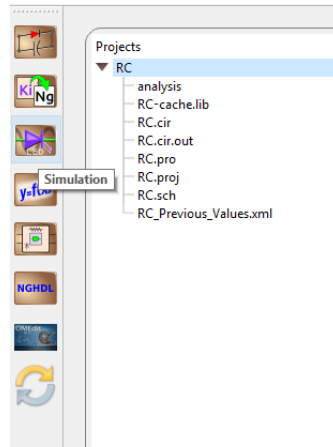
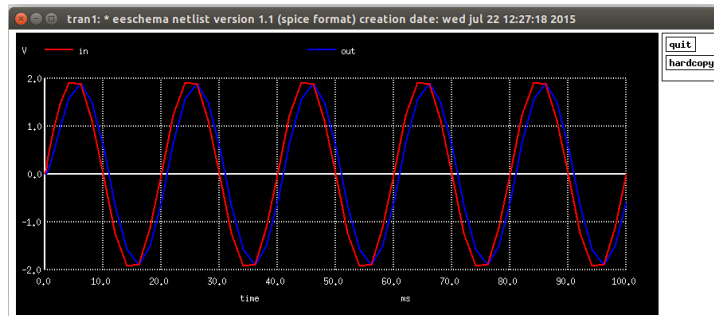
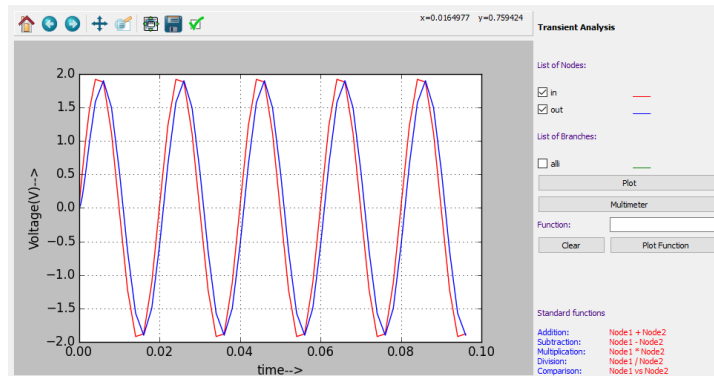


Figure 11.11: Simulation Icon



(a) Ngspice Plot of RC



(b) Python Plot of RC

Figure 11.12: Ngspice and Interactive Python Plotting

11.1.2 Half Wave Rectifier

Problem Statement:

Plot the Input and Output Waveform of Half Wave Rectifier circuit where the input voltage (V_s) is 50Hz, 2V peak to peak. The value for Resistor (R) is 1k.

Solution:

The new project is created by clicking the **New** icon on the menubar. The name of the project is given in the window shown in Fig. 11.1.

- **Creating Schematic:** To create the schematic, click the very first icon of the left toolbar as shown in the Fig. 11.2. This will open KiCad Eeschema.

After the KiCad window is opened, to create a schematic we need to place the required components. Fig. 11.3 shows the icon on the right toolbar which opens the component library.

After all the required components of the simple Half Wave rectifier circuits are placed, wiring is done using the **Place Wire** option as shown in the Fig. 11.4

Next step is **ERC (Electric Rules Check)**. Fig. 11.5 shows the icon for **ERC**. After completing all the above steps the final Half Wave Rectifier schematic will look like Fig. 11.13.

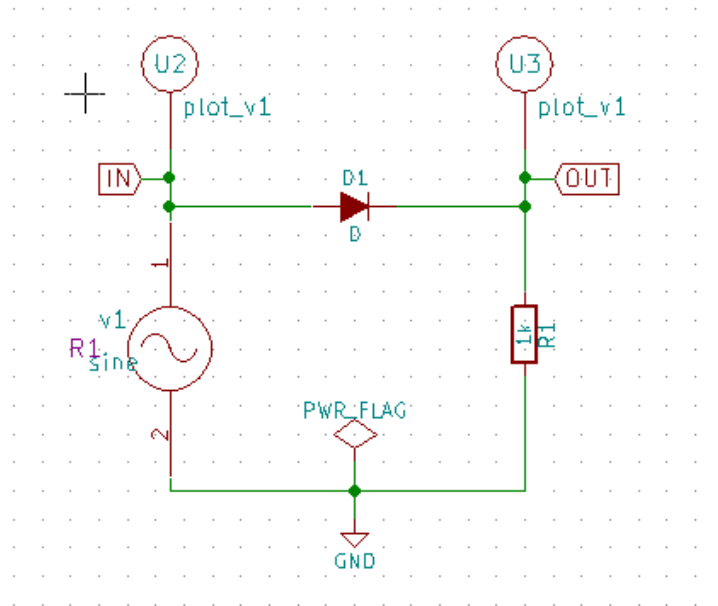


Figure 11.13: Schematic of Half Wave Rectifier circuit

KiCad netlist is generated as shown in the Fig. 11.14

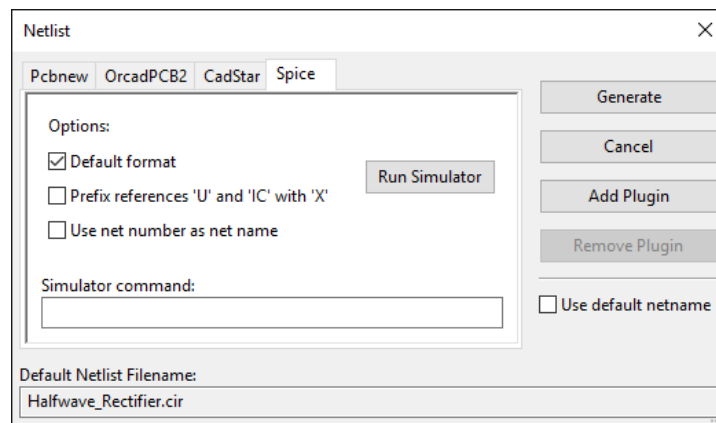


Figure 11.14: Half Wave Rectifier circuit Netlist Generation

- Convert KiCad to Ngspice: After creating KiCad netlist, click on the **KiCad-Ngspice converter** button. This will open converter window where you can enter details of Analysis, Source values and Device library.

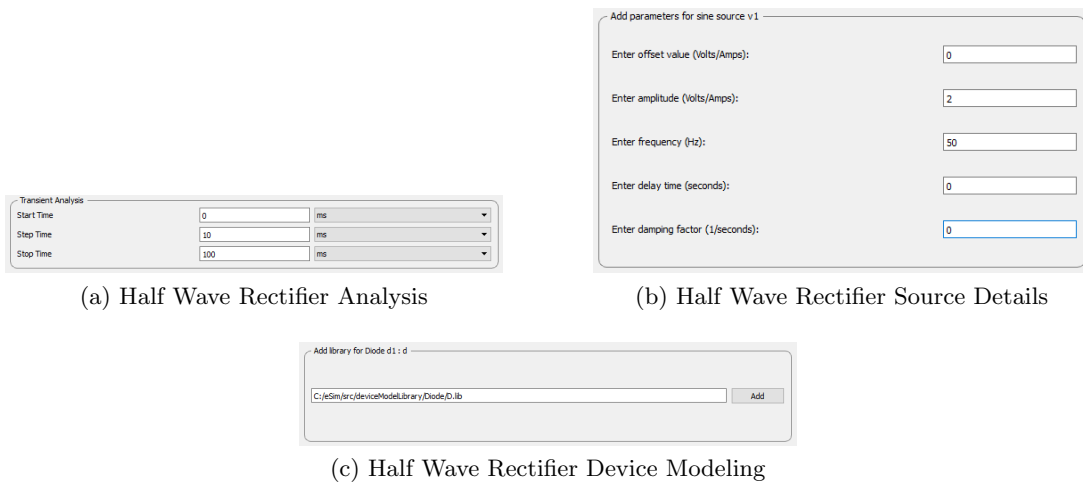
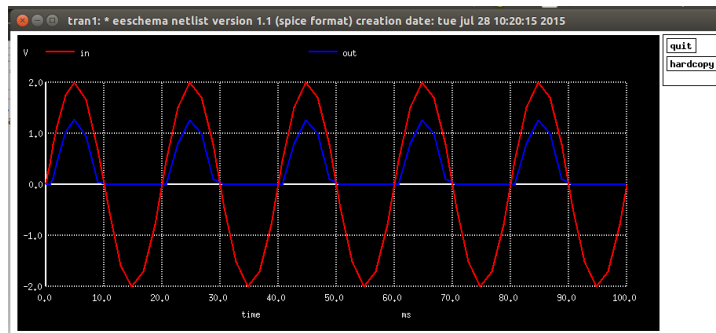


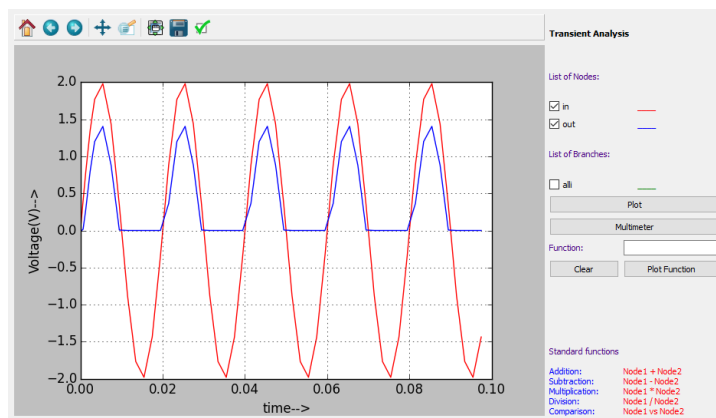
Figure 11.15: Analysis, Source and Device Tab

Under device library you can add the library for diode used in the circuit. If you do not add any library it will take default Ngspice model.

- Simulation: Once the KiCad-NGspice converter runs successfully, you can run simulation by clicking the simulation button in the toolbar.



(a) Ngspice Plot of Half Wave Rectifier



(b) Python Plot of Half Wave Rectifier

Figure 11.16: Half Wave Rectifier Simulation Output

11.1.3 Inverting Amplifier

Problem Statement:

Plot the Input and Output Waveform of Inverting Amplifier circuit where the input voltage (V_s) is $50Hz$, $2V$ peak to peak and gain is 2.

Solution:

- **Creating Schematic:** To create the schematic, click the very first icon of the left toolbar as shown in the Fig. 11.2. This will open KiCad Eeschema. After the KiCad window is opened, to create a schematic we need to place the required components. Fig. 11.3 shows the icon on the right toolbar which opens the component library. After all the required components of the inverting amplifier circuit are placed,

wiring is done using the Place Wire option as shown in the Fig. 11.4.
 Next step is ERC (Electric Rules Check). Fig. 11.5 shows the icon for ERC.
 The Fig. 11.17 shows the complete Precision Rectifier schematic after removing the errors.

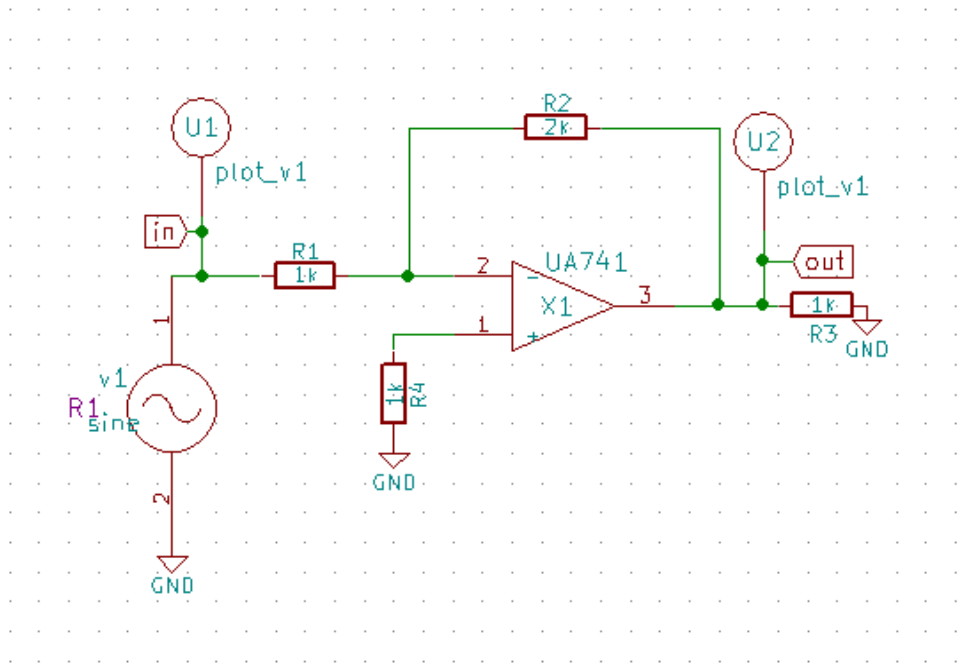


Figure 11.17: Schematic of Inverting Amplifier circuit

The KiCad netlist is generated as shown in Fig. 11.18.

- Convert KiCad to Ngspice: After creating KiCad netlist, click on KiCad-Ngspice converter button.

This will open converter window where you can enter details of Analysis, Source values, Device library and Subcircuit.

Subcircuit of Op-Amp is shown in Fig. 11.19d

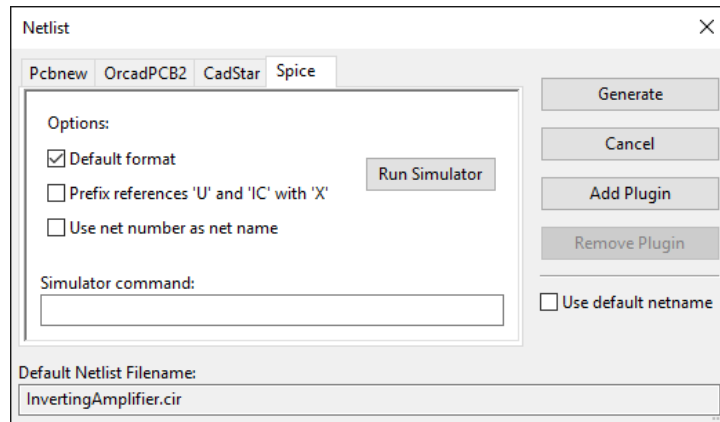
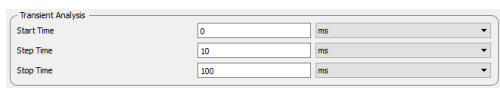
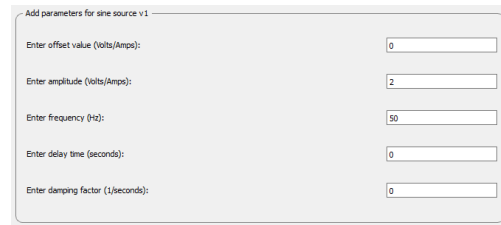


Figure 11.18: Inverting Amplifier circuit Netlist Generation



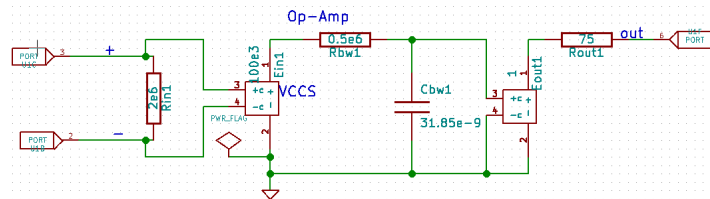
(a) Inverting Amplifier Analysis



(b) Inverting Amplifier Source Details



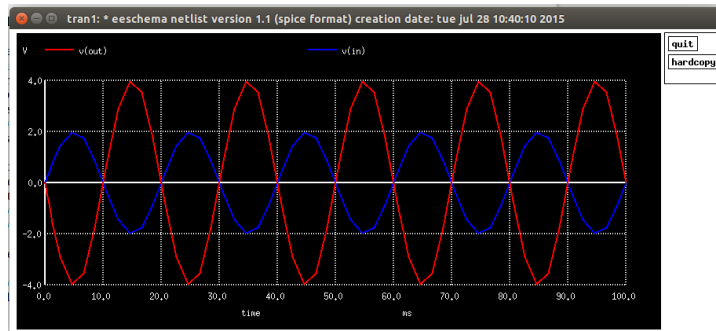
(c) Inverting Amplifier Subcircuit



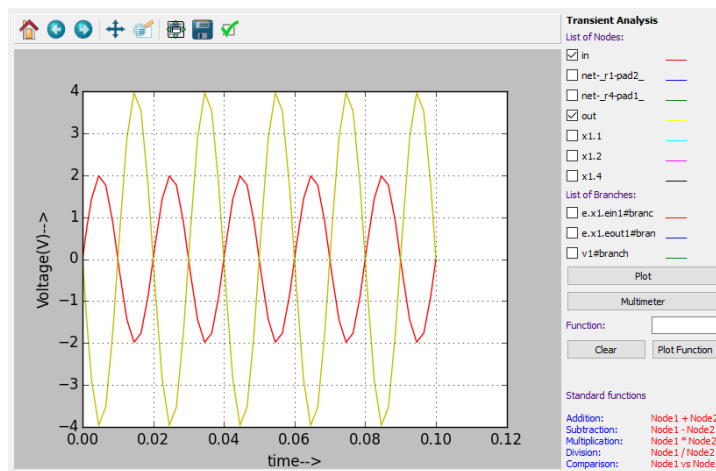
(d) Sub-Circuit of Op-Amp

Figure 11.19: Analysis, Source, and Subcircuit tab

Under subcircuit tab you have to add the subcircuit used in your circuit. If you forget to add subcircuit, it will throw an error.



(a) Inverting Amplifier Ngspice Plot



(b) Inverting Amplifier Python Plot

Figure 11.20: Inverting Amplifier Simulation Output

- Simulation: Once the KiCad-Ngspice converter runs successfully, you can run simulation by clicking the simulation button in the toolbar.

11.1.4 Half Adder

Problem Statement:

Plot the Input and Output Waveform of Half Adder circuit.

Solution:

- **Creating Schematic:** To create the schematic, click the very first icon of the left toolbar as shown in the Fig. 11.2. This will open KiCad Eeschema. After the KiCad window is opened, to create a schematic we need to place the required components. Fig. 11.3 shows the icon on the right toolbar which opens the component library. After all the required components of the Half Adder circuit are placed, wiring is done using the Place Wire option as shown in the Fig. 11.4. Next step is ERC (Electric Rules Check). Fig. 11.5 shows the icon for ERC. The Fig. 11.21 shows the complete Half Adder schematic after removing the errors.

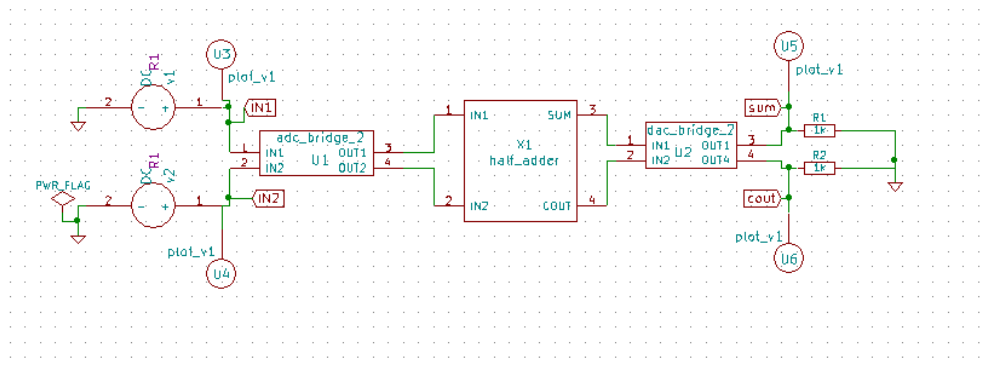


Figure 11.21: Schematic of Half Adder circuit

The KiCad netlist is generated as shown in Fig. 11.22.

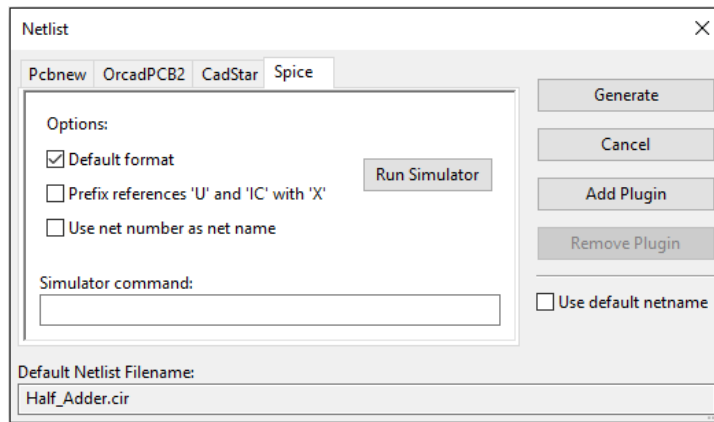
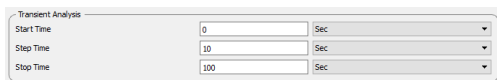


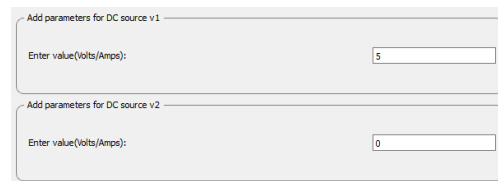
Figure 11.22: Half Adder circuit Netlist Generation

- Convert KiCad to Ngspice: After creating KiCad netlist click on KiCad-Ngspice converter button.

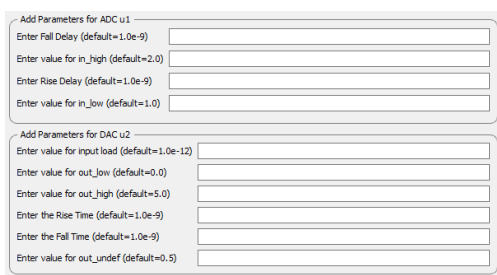
This will open converter window where you can enter details of Analysis, Source values, Ngspice model and Subcircuit.



(a) Half Adder Analysis



(b) Half Adder Source Details



(c) Half Adder Ngspice Model



(d) Half Adder Subcircuit Model

Figure 11.23: Analysis, Source, Ngspice Model and Subcircuit tab

Subcircuit of Half Adder in Fig. 11.24

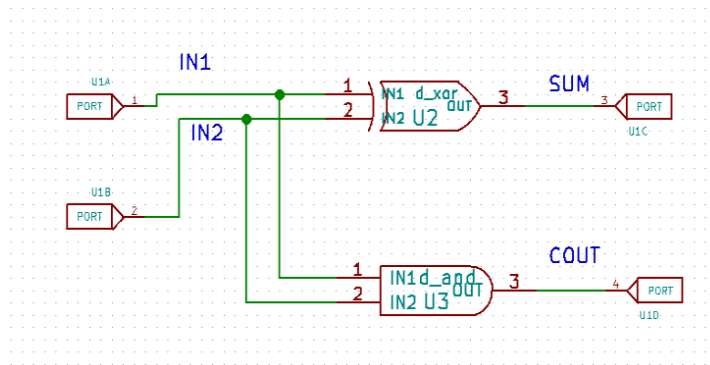
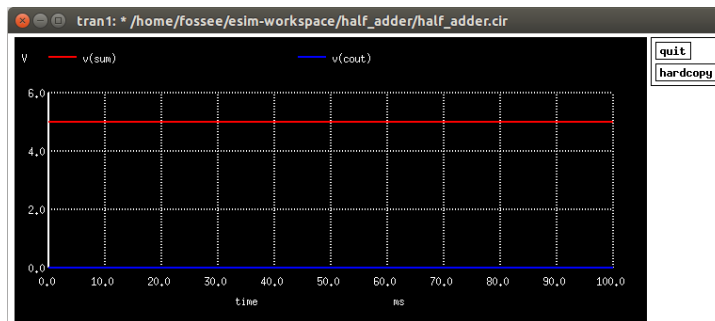
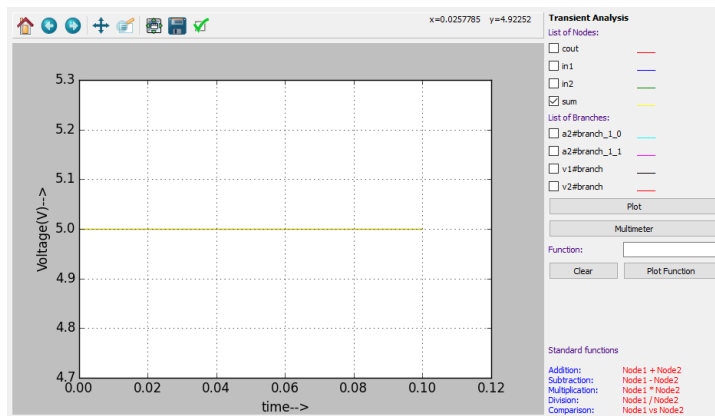


Figure 11.24: Half Adder Subcircuit

- Simulation: Once the KiCad-NGspice converter runs successfully, you can run simulation by clicking the simulation button in the toolbar.



(a) Half Adder Ngspice Plot



(b) Half Adder Python Plot

Figure 11.25: Half Adder Simulation Output

11.1.5 Full Wave Rectifier using SCR

Problem Statement:

Plot the Input and Output Waveform of Full Wave Rectifier using SCR.

Solution:

- **Creating Schematic:** To create the schematic, click the very first icon of the left toolbar as shown in the Fig. 11.2. This will open KiCad Eeschema. After the KiCad window is opened, to create a schematic we need to place the required components. Fig. 11.3 shows the icon on the right toolbar which opens the component library. After all the required components of the Full Wave Rectifier using SCR circuit are placed, wiring is done using the Place Wire option as shown in the Fig. 11.4. Next step is ERC (Electric Rules Check). Fig. 11.5 shows the icon for ERC. The Fig. 11.26 shows the complete Rectifier circuit using SCR after removing the errors.

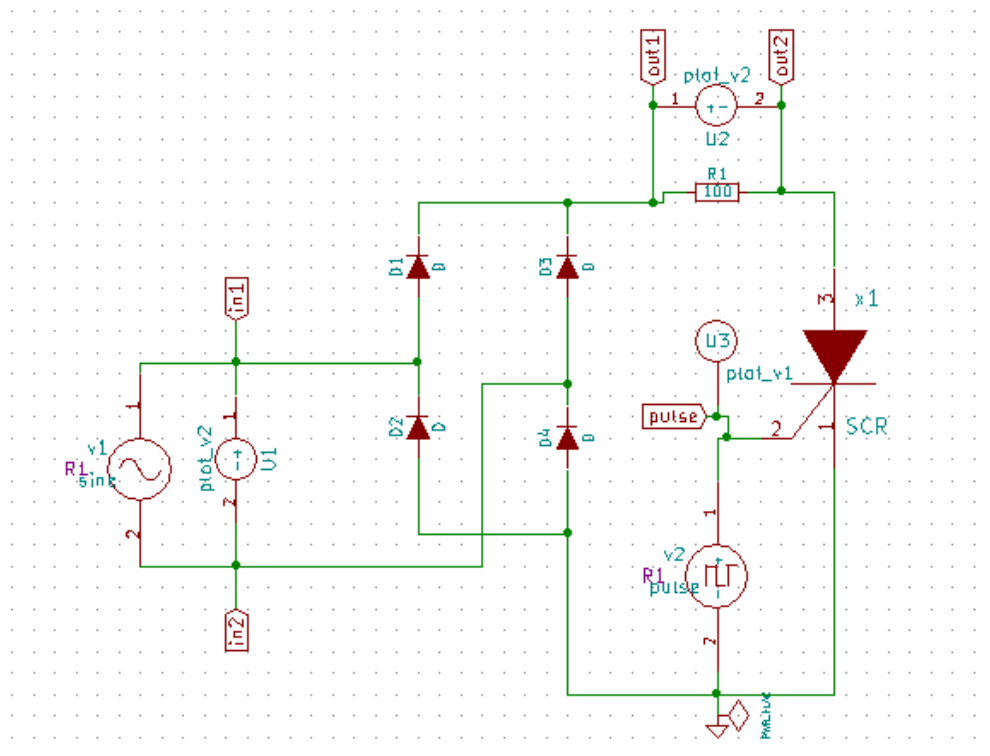


Figure 11.26: Schematic of Full Wave Rectifier using SCR

The KiCad netlist is generated as shown in Fig. 11.27.

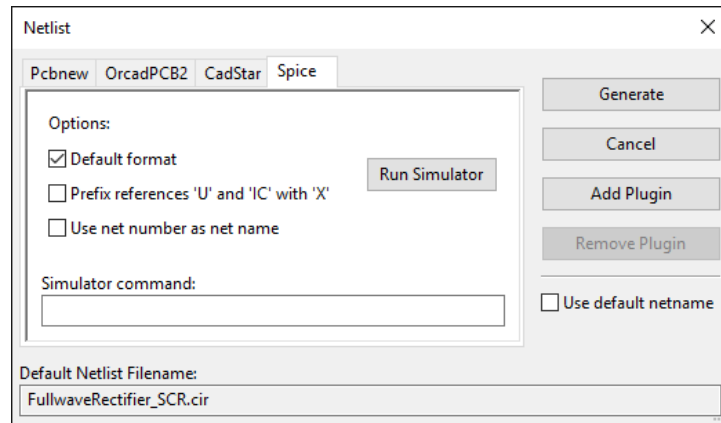


Figure 11.27: Full Wave Rectifier using SCR Netlist Generation

- Convert KiCad to Ngspice: After creating KiCad netlist click on KiCad-Ngspice converter button.

This will open converter window where you can enter details of Analysis, Source values, Ngspice model and Subcircuit.

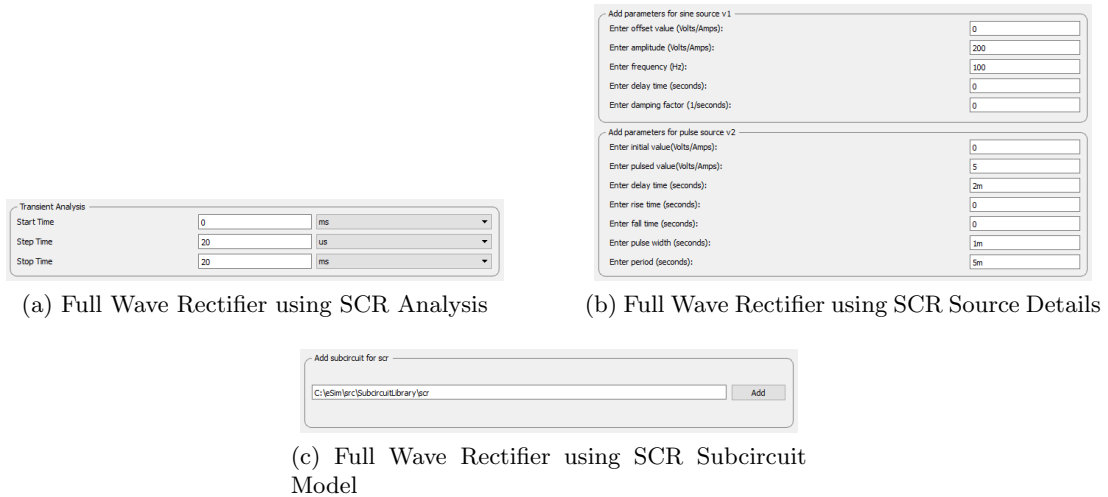


Figure 11.28: Analysis, Source and Subcircuit tab

Subcircuit of SCR in Fig. 11.29

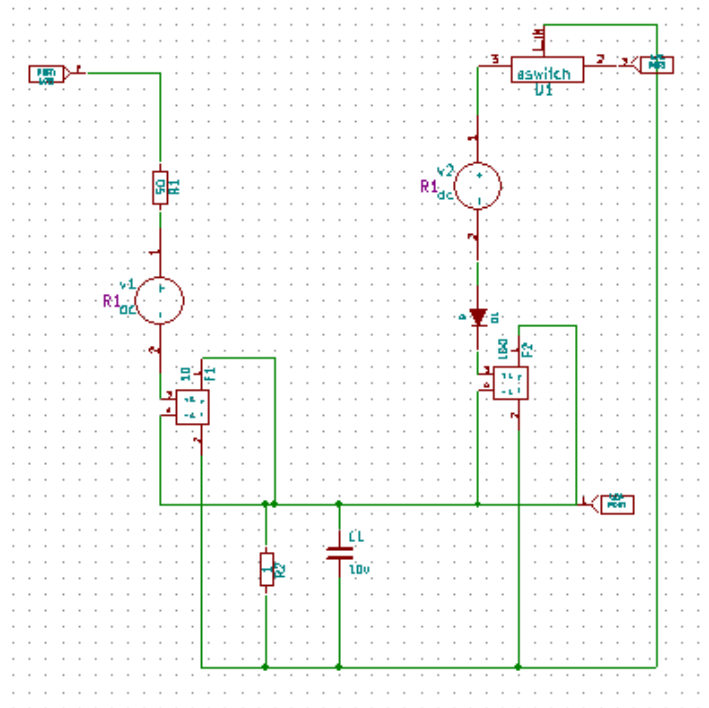
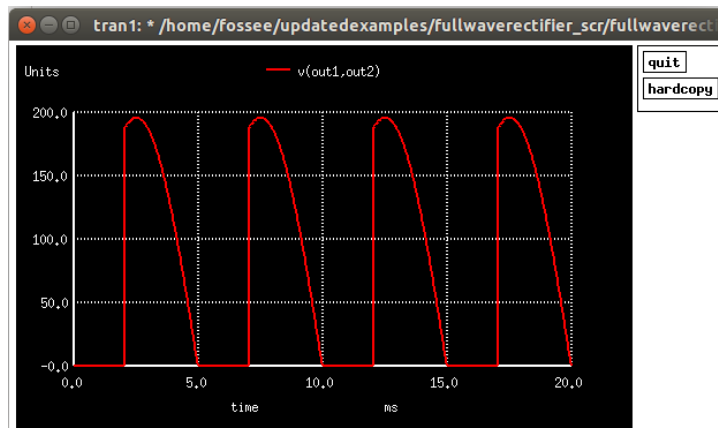
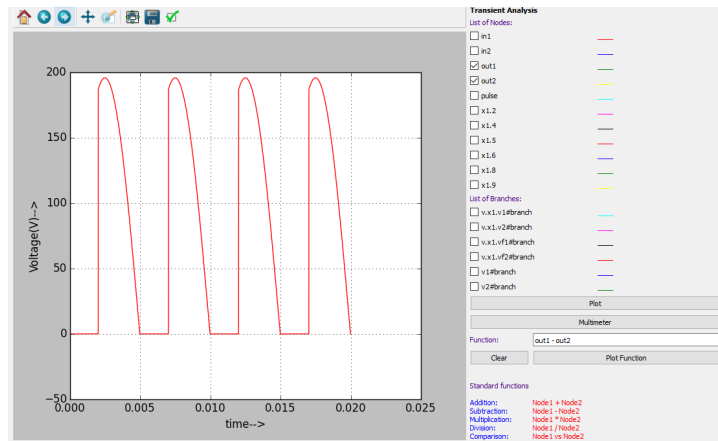


Figure 11.29: SCR Subcircuit

- Simulation: Once the KiCad-Ngspice converter runs successfully, you can run simulation by clicking the simulation button in the toolbar.



(a) Full Wave Rectifier using SCR Ngspice Plot



(b) Full Wave Rectifier using SCR Python Plot

Figure 11.30: Full Wave Rectifier using SCR Simulation Output

11.1.6 Oscillator Circuit

Problem Statement:

Plot the Oscillation Waveforms for Phase Shift Oscillator circuit.

Solution:

The new project is created by clicking the New icon on the menubar. The name of the project is given in the window shown in Fig. 11.1.

- Creating Schematic: To create the schematic, click the very first icon of the left

toolbar as shown in the Fig. 11.2. This will open KiCad Eeschema.

After the KiCad window is opened, to create a schematic we need to place the required components. Fig. 11.3 shows the icon on the right toolbar which opens the component library.

After all the required components of the Oscillator circuits are placed, wiring is done using the Place Wire option as shown in the Fig. 11.4

sss

Next step is ERC (Electric Rules Check). Fig. 11.5 shows the icon for ERC. After completing all the above steps the Oscillator schematic will look like Fig. 11.31.

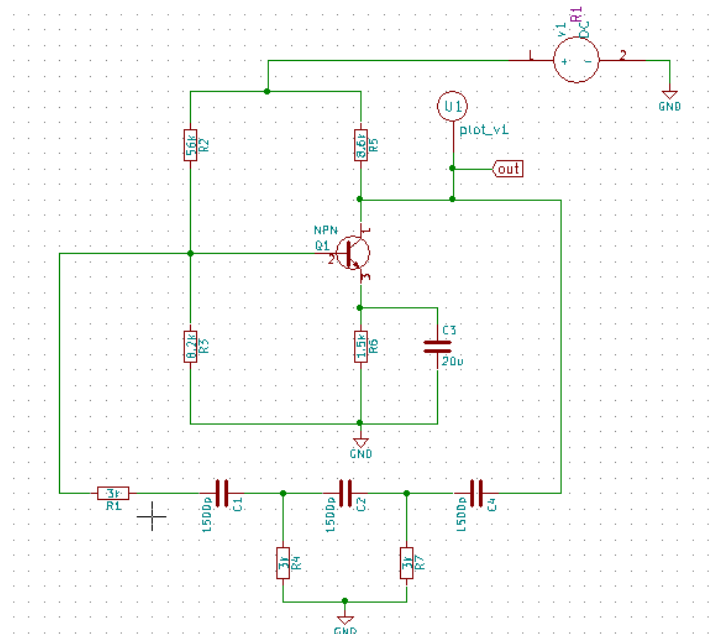


Figure 11.31: Schematic of Phase Shift Oscillator circuit

KiCad netlist is generated as shown in the Fig. 11.32

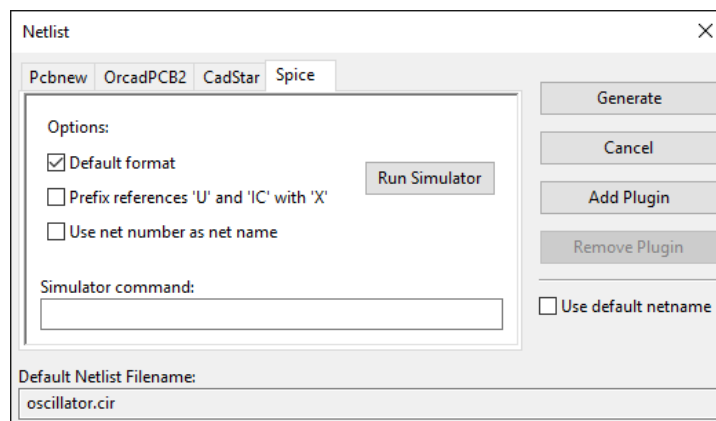
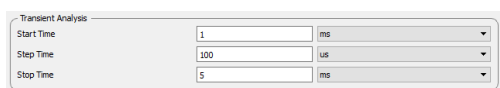
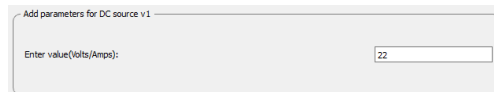


Figure 11.32: Phase Shift Oscillator circuit Netlist Generation

- Convert KiCad to Ngspice: After creating KiCad netlist, click on the **KiCad-Ngspice converter** button. This will open converter window where you can enter details of Analysis, Source values and Device library.



(a) Phase Shift Oscillator Analysis



(b) Phase Shift Oscillator Details

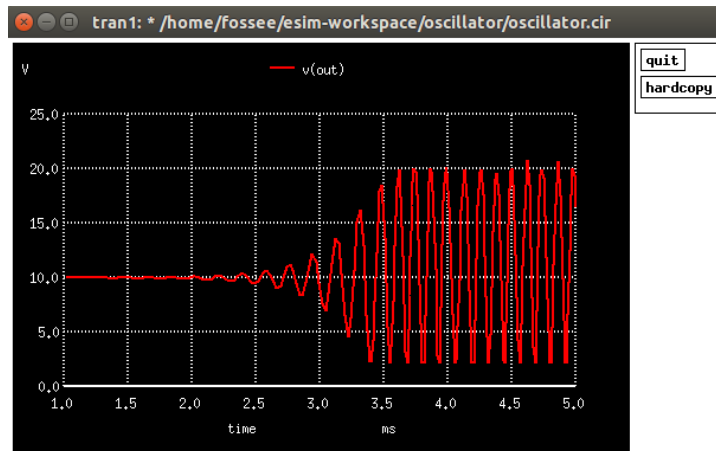


(c) Phase Shift Oscillator Device Modeling

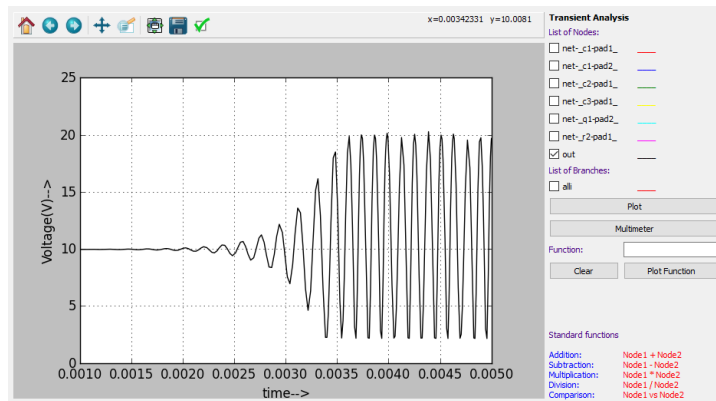
Figure 11.33: Analysis, Source and Device Tab

Under device library you can add the library for diode used in the circuit. If you do not add any library it will take default Ngspice model.

- Simulation: Once the KiCad-Ngspice converter runs successfully, you can run simulation by clicking the simulation button in the toolbar.



(a) Ngspice Plot of Phase Shift Oscillator



(b) Python Plot of Phase Shift Oscillator

Figure 11.34: Phase Shift Oscillator Simulation Output

11.1.7 Characteristics of BJT in Common Base Configuration

Problem Statement:

Plot Characteristics of BJT in Common Base Configuration.

Solution:

The new project is created by clicking the **New** icon on the menubar. The name of the project is given in the window shown in Fig. 11.1.

- **Creating Schematic:** To create the schematic, click the very first icon of the left toolbar as shown in the Fig. 11.2. This will open KiCad Eeschema.

After the KiCad window is opened, to create a schematic we need to place the required components. Fig. 11.3 shows the icon on the right toolbar which opens the component library.

After all the required components of the simple Half Wave rectifier circuits are placed, wiring is done using the Place Wire option as shown in the Fig. 11.4

Next step is ERC (Electric Rules Check). Fig. 11.5 shows the icon for ERC. After completing all the above steps the BJT in CB Configuration schematic will look like Fig. 11.35.

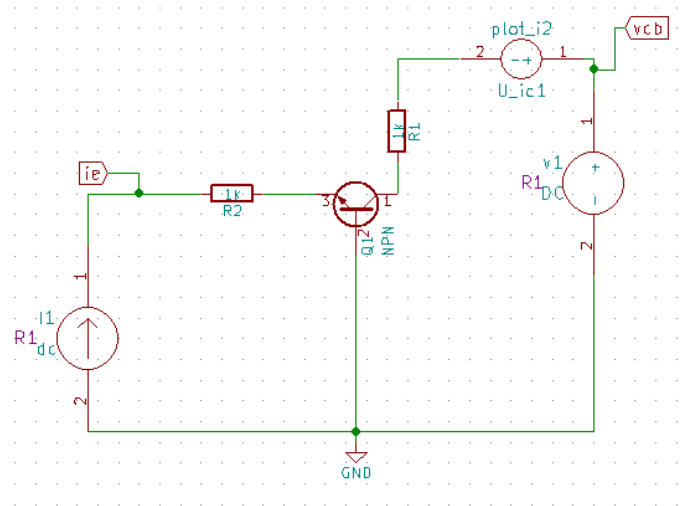


Figure 11.35: Schematic of BJT in CB Configuration circuit

KiCad netlist is generated as shown in the Fig. 11.36

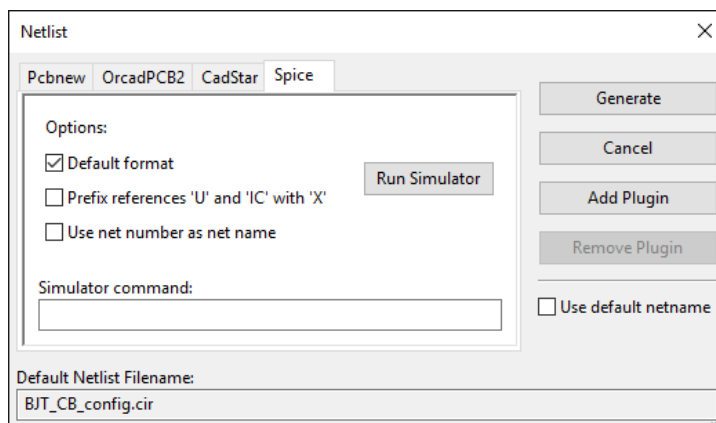
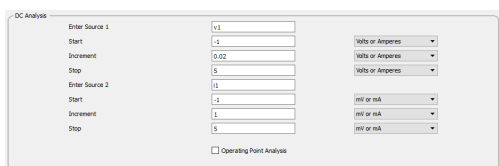
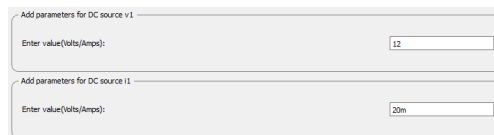


Figure 11.36: BJT in CB Configuration circuit Netlist Generation

- Convert KiCad to Ngspice: After creating KiCad netlist, click on the **KiCad-Ngspice converter** button. This will open converter window where you can enter details of Analysis, Source values and Device library.



(a) BJT in CB Configuration Analysis



(b) BJT in CB Configuration Source Details

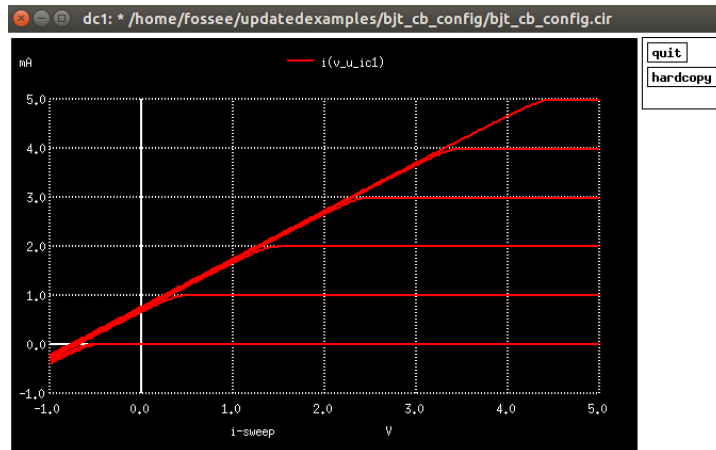


(c) BJT in CB Configuration Device Modeling

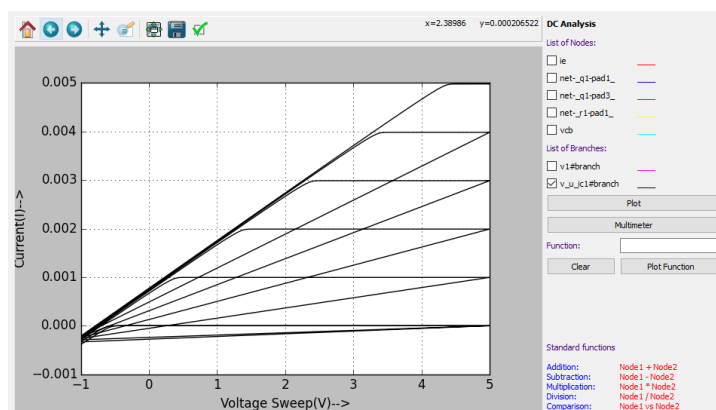
Figure 11.37: Analysis, Source and Device Tab

Under device library you can add the library for diode used in the circuit. If you do not add any library it will take default Ngspice model.

- Simulation: Once the KiCad-Ngspice converter runs successfully, you can run simulation by clicking the simulation button in the toolbar.



(a) Ngspice Plot of BJT in CB Configuration



(b) Python Plot of BJT in CB Configuration

Figure 11.38: BJT in CB Configuration Simulation Output

Chapter 12

PCB Design

Printed Circuit Board (PCB) design is an important step in electronic system design. Every component of the circuit needs to be placed and connections routed to minimise delay and area. Each component has an associated footprint. Footprint refers to the physical layout of a component that is required to mount it on the PCB. PCB design involves associating footprints to all components, placing them appropriately to minimise wire length and area, connecting the footprints using tracks or vias and finally extracting the required files needed for printing the PCB. Let us see the steps to design PCB using eSim.

12.1 Schematic creation for PCB design

In Chapter 5, we have seen the differences between schematic for simulation and schematic for PCB design. Let us design a PCB Layout for a 'constant 5V DC supply' circuit named as `7805VoltageRegulator`. First, we will simulate the circuit. Refer to Fig. 12.1 for the schematic used for simulation. After satisfying simulation results, we will move to PCB design. For this, we will remove the Source(s), Probes (`plot_v` , `plot_db` etc.), and global labels connected solely for the purpose of viewing simulation plots conveniently.

Connectors are the physical components that are used to interface/connect the board to external peripherals or sources.

12.1.1 Removing components required for simulation from the schematic

We will remove the components which were placed for simulation purpose only.

Components that will be placed on the board need to be added in the schematic.

Modify the circuit schematic as shown in Fig. 12.2. The two pin female connector (`Conn_01x02_Female`) is placed for the taking the 5V output supply meanwhile a 2 pin

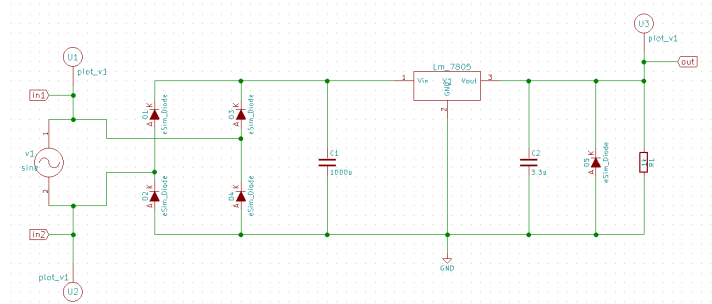


Figure 12.1: Schematic for simulation of the constant 5V DC supply circuit

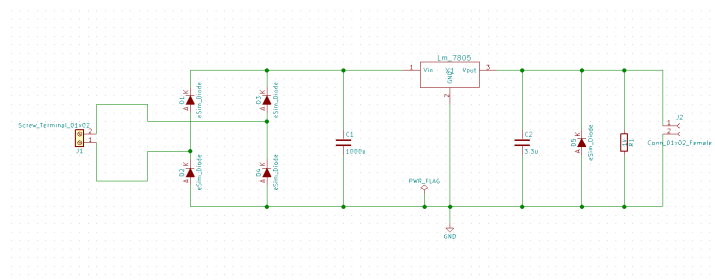


Figure 12.2: Schematic after adding connectors and removing the probes and sources.

Screw Terminal (Screw_Terminal_01x02) is used to transmit the input signal on board. Do the annotation and test for ERC. Refer to Chapter 5 to know more about basic steps in schematic creation.

12.1.2 Mapping of components using Cvpcb

Once the schematic for PCB Design is created, one needs to map each component in the schematic to the appropriate footprint. The tool Cvpcb is used for this.

Cvpcb can be launched by clicking the icon Run Cvpcb to associate footprints and components in Eeschema or by going under the Tools menu and selecting Assign Component Footprint option.

12.1.3 Familiarising with Cvpcb Window

I. When one opens Cvpcb after annotating and running ERC on the schematic intended for PCB Design a window as shown in Fig. 12.3 will be obtained. The Toolbar for using Cvpcb will be available in the top-most left corner.

II. The left pane has a list of all footprint libraries in the database.

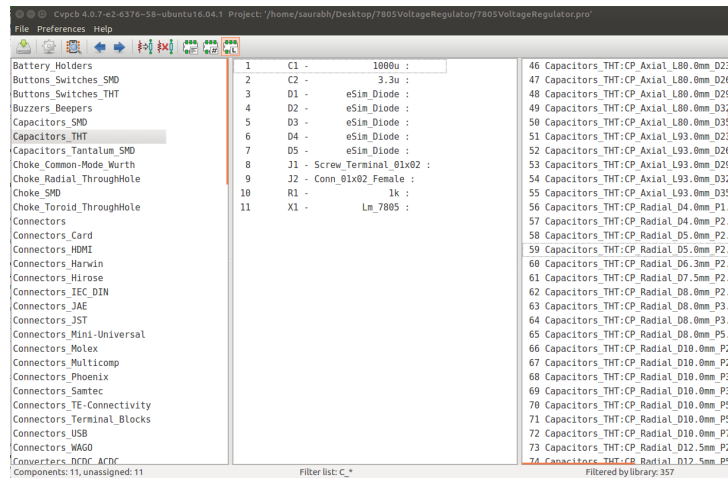


Figure 12.3: Cvcpcb window



Figure 12.4: Cvcpcb Toolbar

III. The middle pane displays the list of components present in the schematic and if any footprint is assigned/associated to them.

IV. The right pane has a list of available footprints for each component depending upon how of libraries.

Cvcpcb Toolbar

Some of the important tools in the toolbar are shown in Fig. 12.4. They are explained below (Order of operation should ideally be from RIGHT to LEFT):

1. Filter footprints list by library : We recommend the use of only this as a filtering method if you are completely new to eSim and/or PCB Design as it narrows down footprints based on libraries of the type of the component. When a filter is selected, it's icon will be highlighted in light red color as seen in Fig. 12.4.
2. Filter footprints list by pin count : This will filter the footprints based on number of pins the footprint has. This can be used to narrow down your search after sorting footprints by their library type.
3. Filter footprints list by keyword - This filters the footprints in the database based on keywords.
4. Automatic footprint association - Perform footprint association for each component automatically. Footprints will be selected from the list of footprints available.

Note: This method of association is not recommended at all.

5. Delete all associations - Delete all the footprint associations made. This will erase all your association till now so be very careful in selecting this.
6. Select next unlinked component: Using this you can go to the next component in the list of components for associating a footprint.
7. Select previous unlinked component: Using this you can go to the previous component in the list of components for associating a footprint.
8. View selected footprint - View the selected footprint in 2D. See Sec. 12.1.4 for more details.

Before clicking on this, make sure that a footprint is selected. Order of this operation should be

1. Selection of footprint library from the left-most pane
 2. Selecting a footprint from the right-most pane
 3. Click on View selected footprint
9. Edit footprint library table - One should familiarize themselves with Cvpcb first and then only choose to use this. This impacts the footprints that you can choose, so be careful before making any severe changes.
 10. Save netlist and footprint files - Save the netlist and the footprints that are associated with it. One ought to save the association after having assigned proper footprints to all the components.

12.1.4 Viewing footprints in 2D and 3D

To view a footprint in 2D, select the component for which you wish to view the available footprints, then select the library from left-most pane and now from the right pane and click on the desired footprint and click on **View selected footprint** from the menu bar. Let us view a footprint for C1 from the `Capacitors_THT` footprint library. Choose C1 from the middle pane as shown, click on `Capacitors_THT` in the left-most pane and select the *View selected footprint* tool. On clicking the **View selected footprint** tool, the Footprint window with the view in 2D will be displayed. 2D view of the footprint `CP_Radial_D5.0mm_P2.50mm` is shown in Fig. 12.6.

Click on the 3D Display icon in the Footprint window, as shown in Fig. 12.6. A top view of the selected footprint in 3D is obtained. Click on the footprint and rotate it using the computer mouse to get 3D views from various angles. One such view of the footprint in 3D is shown in Fig. 12.7.

12.1.5 Mapping of components in the circuit

1. Click on C1 from the middle pane. Choose the footprint library *Capacitors_THT* from the left pane and locate the footprint `CP_Radial_D5.0mm_P2.50mm`. By double clicking on it, the said footprint will be assigned to C1.

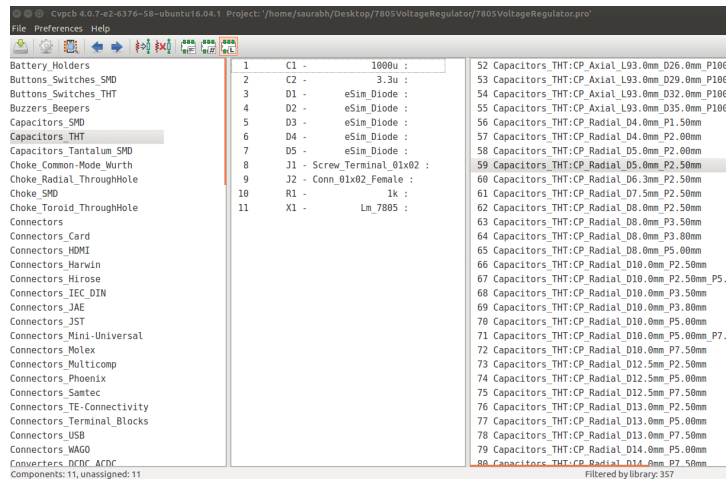


Figure 12.5: Viewing footprint for C1

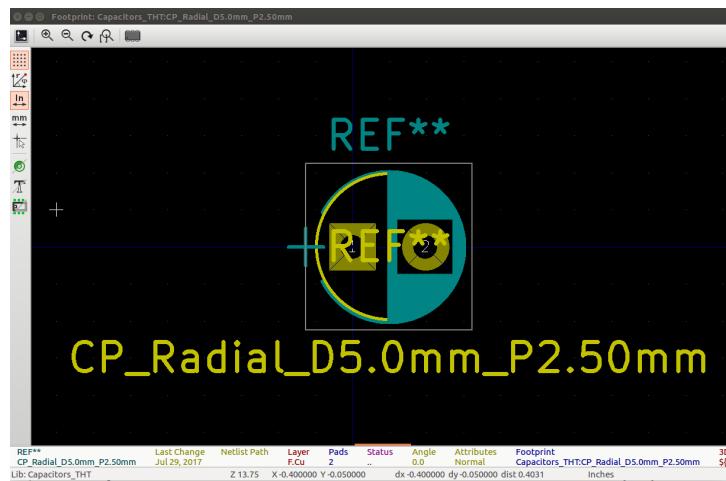


Figure 12.6: Footprint CP_Radial_D5.0mm_P2.50mm's view in 2D.

2. Similarly choose the footprints per Fig. 12.8 where the footprint association for all the footprints is shown in Fig. 12.8. Save the footprint association by clicking on the Save footprint association in schematic component footprint fields tool from the CvPcb toolbar.

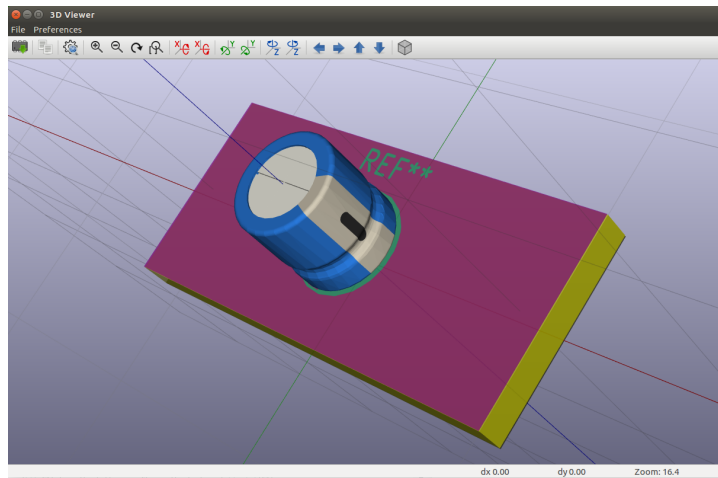


Figure 12.7: 3D view of the footprint

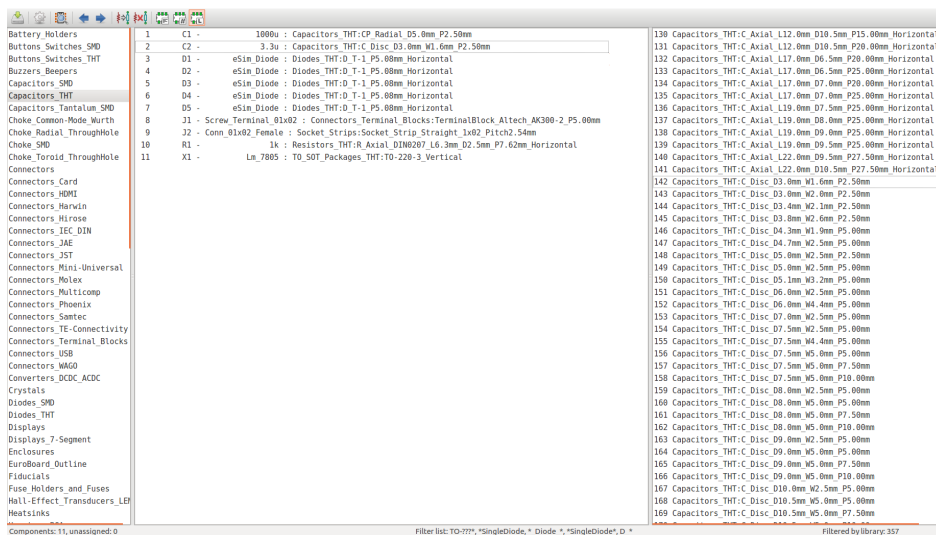


Figure 12.8: Footprint mapping completed for the circuit

12.1.6 Netlist generation for PCB

1. After having saved your footprint association, switch back to the Eeschema window and press Ctrl+S.
2. The netlist for PCB is different from that for simulation. To generate netlist for PCB, click on the *Generate netlist* tool from the top toolbar in Schematic editor.
3. In the Netlist window, under the tab *Pcbnew*, Select the option **Default** format. This is shown in Fig. 12.9. Click on **Generate** option.

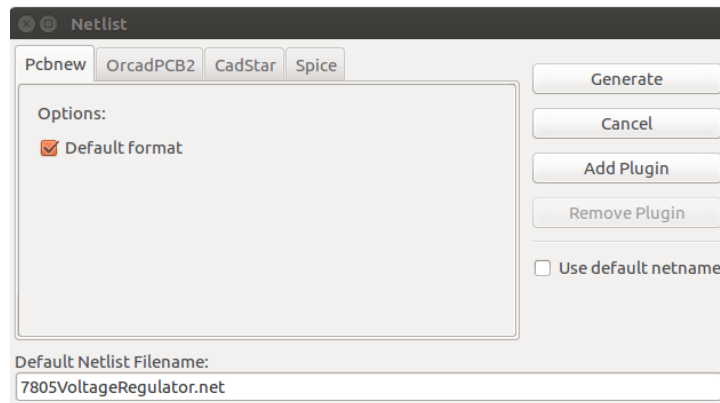


Figure 12.9: Netlist generation for PCB

4. Click on **Save** in the Save netlist file dialog box that opens up. Do not change the directory or the name of the netlist file. Note that the netlist for PCB has an extension *.net*. The netlist created for simulation has an extension *.cir*.

12.2 Creation of PCB layout

The next step is to place the footprints and lay tracks between them to get the layout. This is done using the *Layout Editor* tool. eSim uses Pcbnew, the layout creation tool in KiCad, as its layout editor.

12.2.1 Launching Pcbnew

1. To Launch the layout editor, Pcbnew, click on the **Run Pcbnew to layout printed circuit board** icon on the top right corner of the Schematic window.
2. Similarly, you can also click on **Tools**, and select the **Layout printed circuit board** option.
3. After doing either of the steps above, click **yes** on the *Confirmation Box* that will appear on the screen.

12.2.2 Familiarizing the Layout Editor tool

The layout editor with the various menu bar and toolbars is shown in Fig. 12.10.

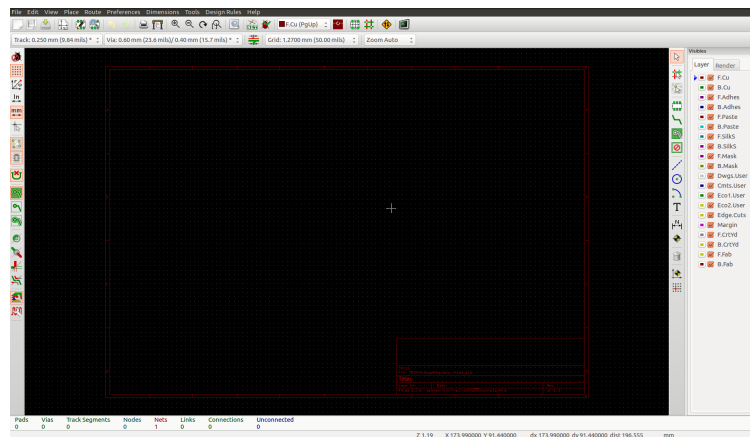


Figure 12.10: Layout editor with menu bar, toolbars and layer options

Top toolbar

Some of the important menu options in the top menu bar are shown in Fig. ???. They are explained below:

1. Save board - Save the printed circuit board
2. Plot - This enables users to import their design in Gerber, PDF, SVG and few more formats depending on the requirement.
3. Read netlist - Import the netlist whose layout needs to be created.
4. Perform design rules check - Check for design rules, unconnected nets, etc., in the layout.
5. Select working layer - Selection of working layer.

Note: Selection of working layer can also be done from the **Layers** toolbar on the right-most side of the Pcbnew tool window.

12.2.3 Hotkeys

A list of few important hotkeys is given below:

1. F1 - Zoom in
2. F2 - Zoom out
3. Delete - Delete Track or Footprint
4. X - Add new track
5. V - Add Via
6. M - Move Item
7. F - Flip Footprint
8. R - Rotate Item
9. G - Drag Footprint
10. Ctrl+Z - Undo

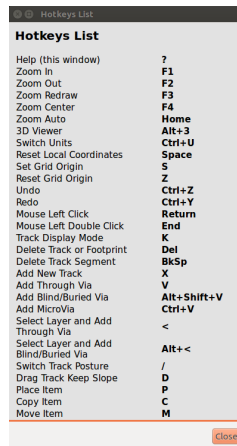


Figure 12.11: Default Hotkeys

11. E - Edit Item

The entire list of Hotkeys can be viewed by selecting *Preferences* from the top menu bar and choosing *List Current Keys* from the option *Hotkeys*.

12.2.4 Designing PCB layout for 7805VoltageRegulator circuit

Click on *Read Netlist* tool from the top toolbar of Pcbnew. Click on *Browse Netlist files* on the Netlist window that opens up. Select the **.net** file that was modified **after** assigning footprints. Click on *Open*. Now Click on *Read Current Netlist* on the Netlist window. The sequence of operations is shown in Fig. 12.12.

Arranging the footprints

1. After clicking on Read Netlist button and closing the Read Netlist window, the footprints that we assigned will appear on the Pcbnew screen in a cluttered fashion, stacked on top of each other as shown in Fig. 12.13
2. Let us separate these footprints and place them in proper orientation per the requirement of the circuit. Let us start with Screw_Terminal_01x02 footprint.
3. Right Click on the text Screw_Terminal_01x02 in the Pcbnew window, and select **Footprint J1 on F.Cu.** and select the **Move** option from the list.
4. The footprint will be glued to the cursor and it can be placed in the location of one's choice by moving the cursor at the desired location and clicking once to place it there.
5. We have moved the Screw_Terminal_01x02 footprint to the left side of the Pcbnew window.
6. Once again right click on the text Screw_Terminal_01x02 in the Pcbnew window,

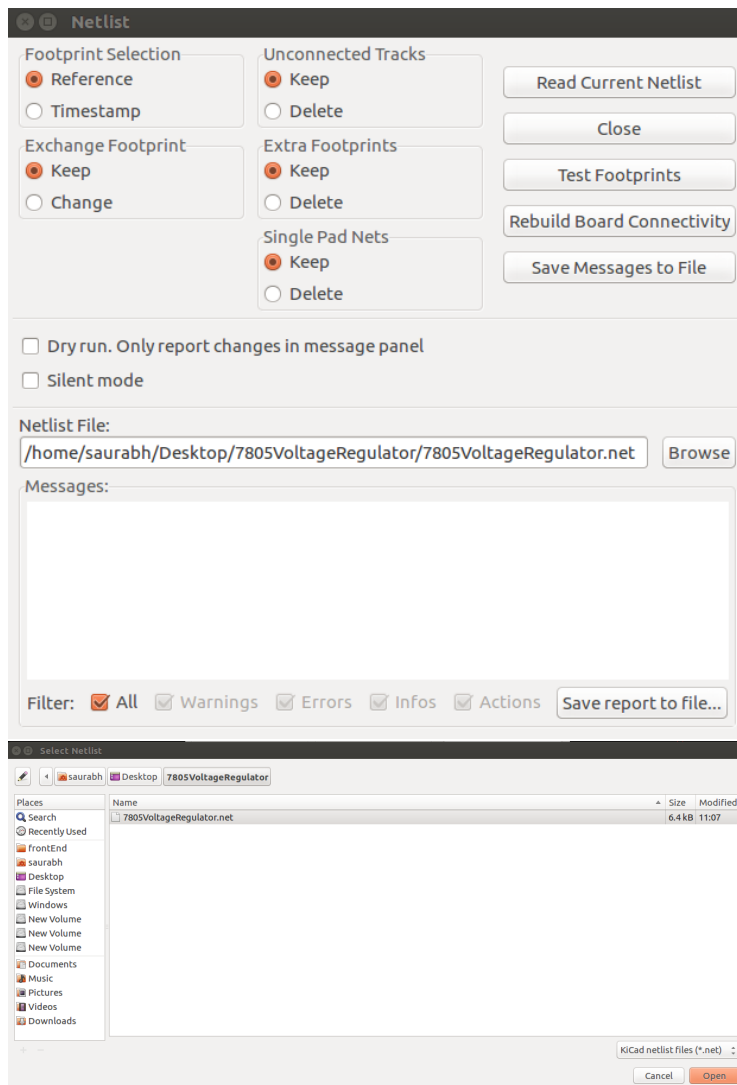


Figure 12.12: Importing netlist file to layout editor: 1. Browse netlist Files, 2. Choose the appropriate .net file, 3. Read Netlist file, 4. Close

and select Footprint J1 on F.Cu. and select the Rotate + option from the list as shown in Fig. 12.15

7. Using similar methods, we have moved and rotated all other footprints as shown in Fig. 12.16



Figure 12.13: Cluttered footprints

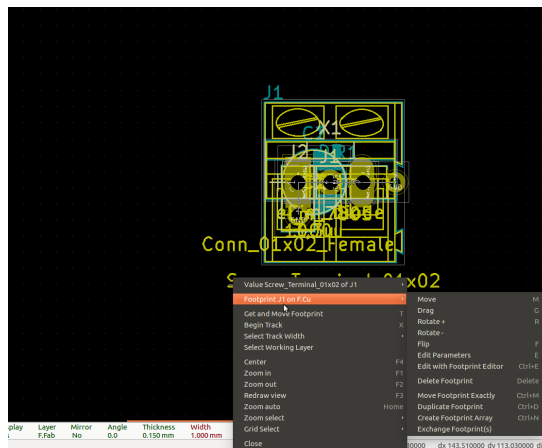


Figure 12.14: Moving the footprint

Setting Design Rules

1. Click on **Design Rules** on top of the Pcbnew window, select **Design Rules** option from the drop down menu there.
2. **Design Rules Editor** window will open, Under the **Net Classes Editor**, locate the **Track Width** box, erase the default value from the window placed under the **Track Width** box and enter 1.25 as the track width.
3. Click on **Global Design Rules**, under **Minimum Allowed Values**, locate **Min track width**, erase the default value and enter 1.25 in the data entry field on the right side of it as shown in Fig. 12.17. This will ensure that all tracks placed are of width 1.25mm and that when we perform **Design Rules Check**, the checks

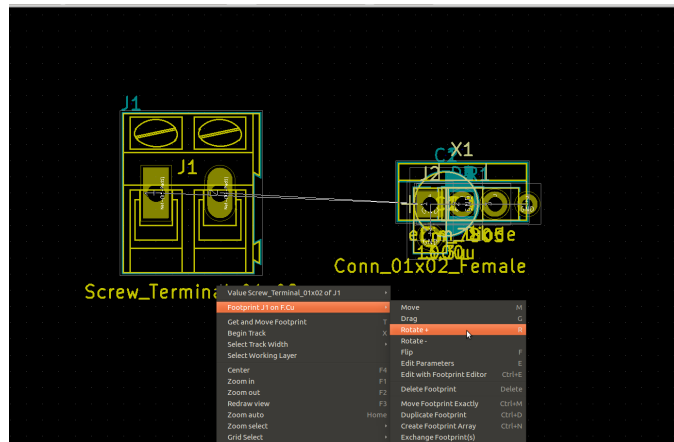


Figure 12.15: Rotating the footprint

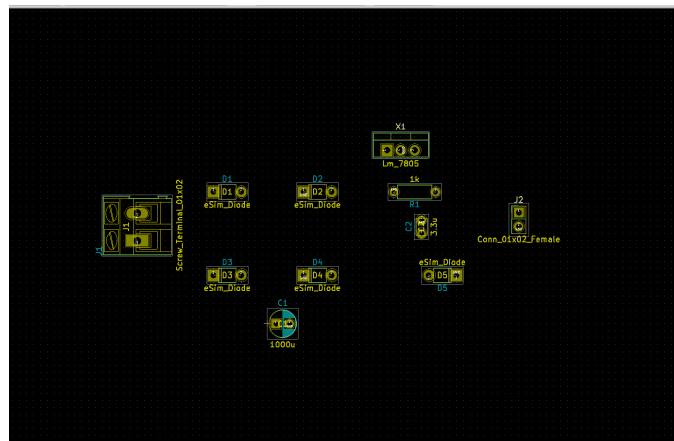


Figure 12.16: All footprints moved and rotated

- will be made such that all tracks are of the width 1.25mm will be checked.
4. Click on Ok button and close the Design Editor Rules window.

Drawing the Board Outline

1. Board outline defines the physical dimensions of your board. After the fabricator is done placing tracks and other processes, he/she will cut your design from the copper cladded sheet or the material used per your choice, as per your board outline dimensions. Say, if your board outline is of rectangular shape with dimensions 80mmx50mm, the fabricator will cut the copper sheet of the said dimension. Its important to know that all the tracks(physical electrically conductive connections

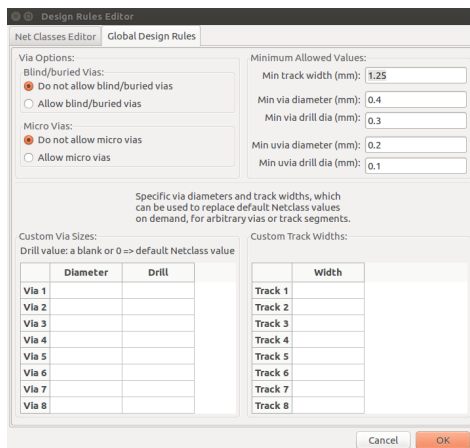


Figure 12.17: Design Rules Editor Window: Global Design Rules

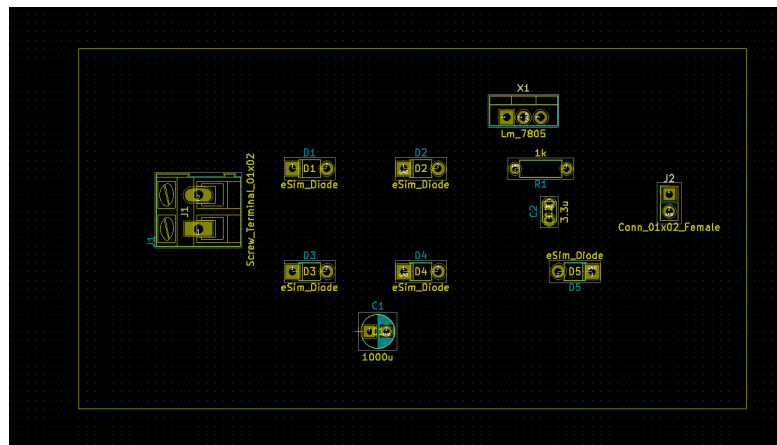


Figure 12.18: Drawing a board outline

- between two nodes or points on a PCB) must lie inside this board outline.
2. We will also choose a board outline of rectangular shape. Select working layer as `Edge.Cuts` from the Layers menu on the far-right side of Pcbnew.
 3. Click on `Place` from the top-left tool bar of the Pcbnew window and select `Line` or `Polygon`. A pencil icon will appear to be tied to the cursor.
 4. Click once on the layout editor to start drawing the outline. Drag the cursor either horizontally or vertically. When it comes to the corner of the board, click once and drag the cursor in perpendicular direction. Do this till you reach the origin of the outline, and double click to finish drawing the rectangular outline. Completed outline is as shown in Fig. 12.18.

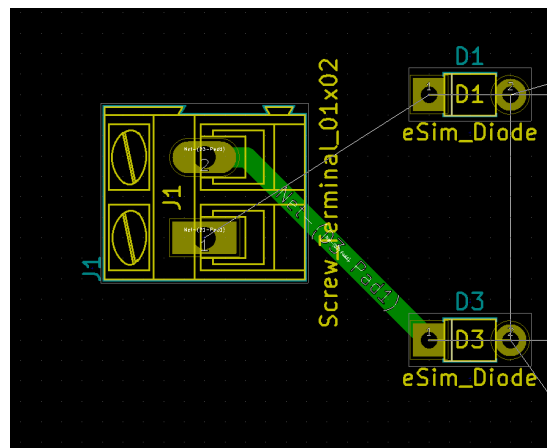


Figure 12.19: Track placed on B.Cu. between Screw_Terminal_01x02 connector and D3 Diode

Placing Tracks

1. Select the working layer as B.Cu from the Layers menu on the far-right side of Pcbnew.
2. Click on Place from the top-left tool bar of the Pcbnew window and select Track. A pencil icon will appear to be tied to the cursor.
3. The procedure to place a track between Node 2 of Screw_Terminal_01x02 to Node 1 of D3 diode, as shown in Fig. 12.18 is described in below steps.
4. Working layer is B.Cu., Place Track tool is selected earlier. Click the pencil icon tied to cursor on the Node 2 of Screw_Terminal_01x02 and drag the cursor till Node 1 of D3 diode and double click on Node 2 of D3. By double clicking the track will end at Node 2 of D3. Please refer Fig. 12.19 for the mentioned track being placed.
5. Similarly, all the tracks have been placed as shown in Fig. 12.20. Please note that tracks shown in green color are on B.Cu. layer whereas the tracks in red color are placed on the F.Cu. layer.

Performing Design Rules Check(DRC)

1. After tracks are placed, it is important that the design created by used should not violate any design rules set earlier.
2. Click on Perform Design Rules check button from the top menu bar of Pcbnew. DRC Control Window will pop-up as shown in Fig. 12.21.
3. Click on Start DRC, and observe if any messages/warnings appear in the error messages window at the bottom of the DRC Control window. If there are no

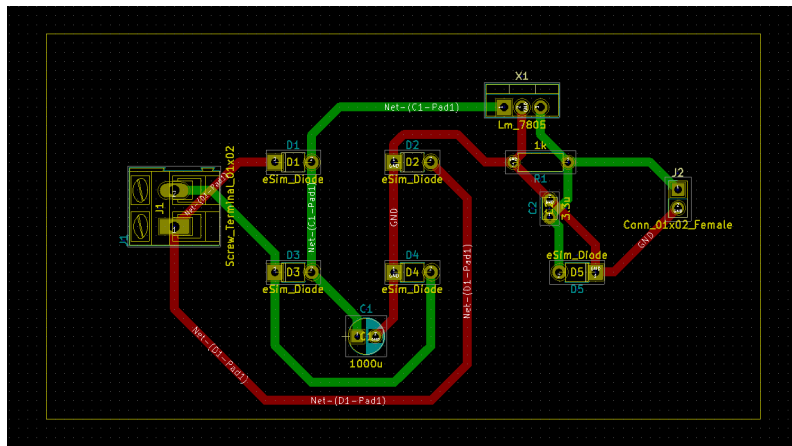


Figure 12.20: All tracks placed

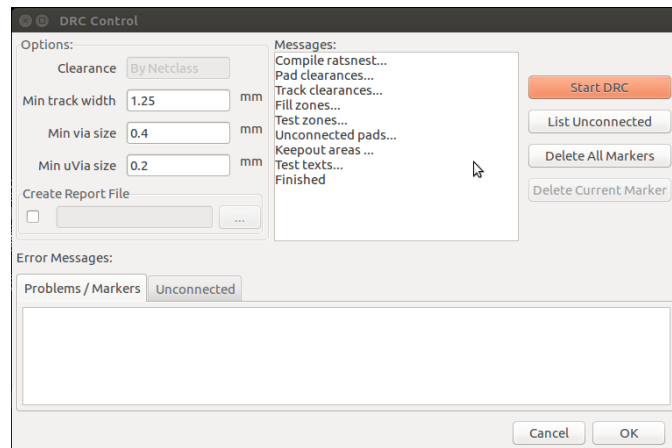


Figure 12.21: DRC Control Window

errors in the design present, there will not be any errors in the message window as shown in Fig. 12.21

Exporting the Design to Gerber format

1. Click on Plot tool from the top toolbar, select the Plot Format as gerber from the drop down menu of Plot Format.
2. Select the directory in which the user wishes to save the gerber files.
3. Select F.Cu, B.Cu, B.Silks, F.Mask, B.Mask, Margin and Edge.Cuts from the Layers on the left side of the Plot window as shown in Fig. 12.22.
4. After clicking on 'Plot' button, acknowledgment messages can be seen in the 'Mes-

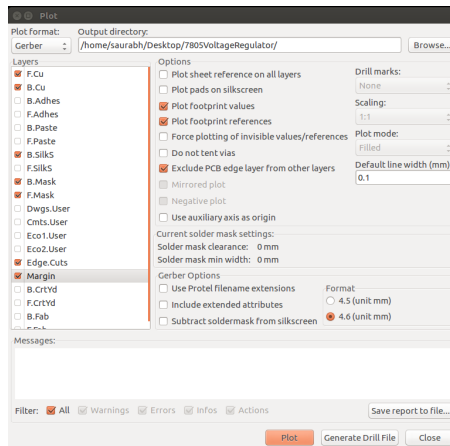


Figure 12.22: Plot Window before generating gerber files

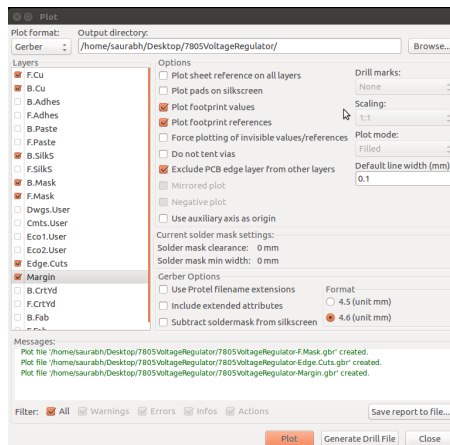


Figure 12.23: Plot window after generating gerber files

sages' window at the bottom of the Plot tool window as shown in Fig. 12.23.

Viewing the Gerber files generated

1. Open the terminal by Ctrl+Alt+T keys, and type `gerbview` and press enter. Gerbview tool of KiCad will open up. For windows OS users, search for `gerbview` application through Windows' search application option.
2. Click on File from top-left menu, and select Load Gerber File option.
3. Go to the directory where you have stored the earlier created gerber files as shown in Fig. 12.24 and click on Open.
4. The design created earlier will appear in the gerbview window as shown in Fig. 12.25.

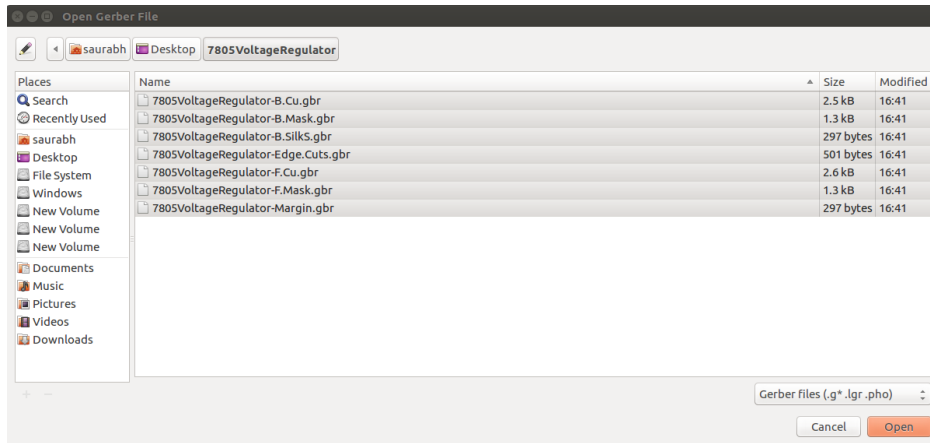


Figure 12.24: Loading gerber files in the gerbview

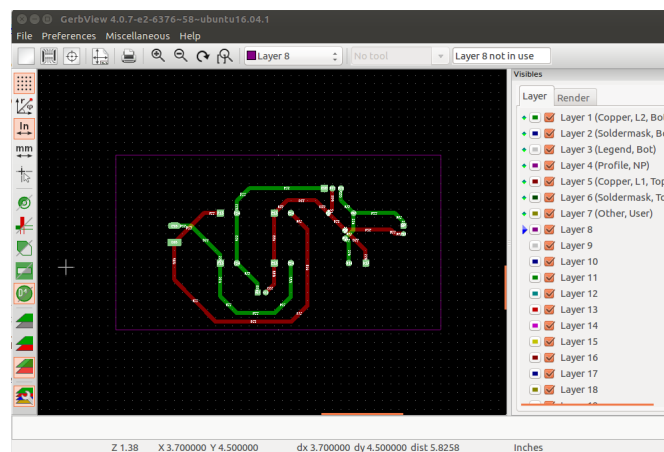


Figure 12.25: Observing the design in Gerber format

Chapter 13

Appendix

13.1 Appendix A

13.1.1 A.1: Pin types in KiCad

- **Input:** is a unidirectional input.
- **Output:** is a unidirectional output that can drive high or low.
- **Bidirectional:** can act as an input or an output. The I/O pins on microcontrollers are bidirectional.
- **Tri-state:** is an output that can drive high or low, but can also be placed in a high-impedance state where it floats. The 74125 is a chip with tri-state outputs (sometimes called three-state outputs: high, low, and high-impedance).
- **Passive:** is an unpowered connection, like resistors, capacitors and inductors.
- **Unspecified:** is, unspecified. User would use that when no other classification fits.
- **Power input:** is a pin where power comes in to a chip. Both the VCC and GND pins of chips would be classified as power inputs.
- **Power outputs:** are where power comes out of a chip. The outputs of voltage regulators are the most common example of this pin type.
- **Open collector output pins:** are outputs that can be driven low, but float otherwise. These are good for wired-AND connections where the output goes low if any of the attached open-collector pins goes low, but the output is pulled high by a pull-up resistor if all the pins are floating. The 7401 is a NAND gate chip with open-collector outputs.

- **Open emitter output pins:** can be driven high, but float otherwise. These are good for wired-OR connections where the output goes high if any of the attached open-emitter pins goes high, but the output is pulled low by a pull-down resistor if all the pins are floating.
- **Not-connected:** pins are pins which have no function. Think of these as package pins that are not bonded to the IC inside.

13.1.2 A.2: ERC Table

- User can actually decide what you want to be told about, by setting the table below accordingly. For instance if the user wanted the ERC to throw an error if an input was connected to an input then the user would change the topmost box from green (no message) to yellow (warning) or red (error) as shown in Fig. ??

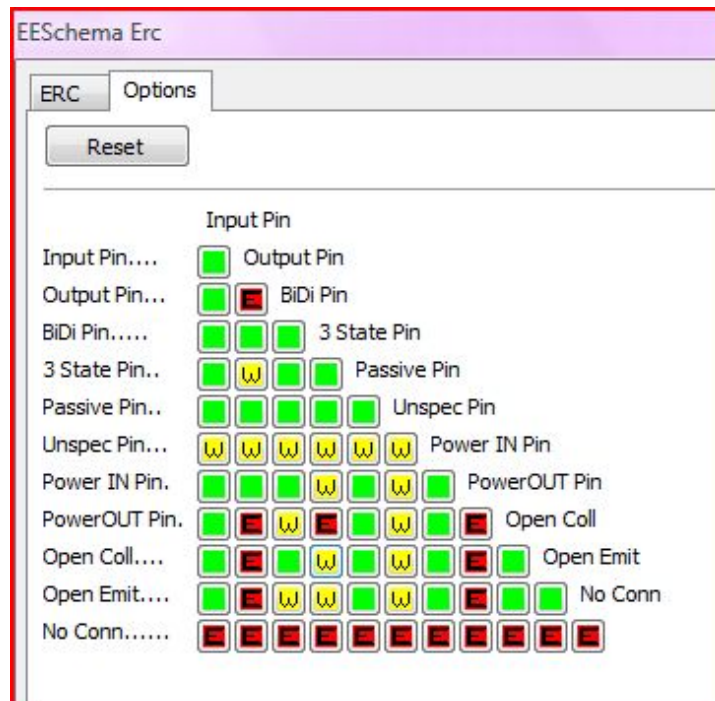


Figure 13.1: ERC Table

13.2 Appendix B

13.2.1 B.1: Shortcut keys in Schematic editor

- Open the schematic editor and press Shift and ? keys simultaneously. This will display the total shortcut keys, also called as Hotkeys. Please note that, if the shortcut key is related to a component, for example, changing its value or its orientation etc, then your cursor must be located on that component.
- **V**: This edits the Component's value.
- **R**: This rotates a component.
- **A**: This calls the place component tool through which you can add components in your schematic.
- **M**: This moves a component. After pressing M key, the component you chose will be tied to the cursor and you can place it anywhere in the schematic by clicking once on the schematic editor.
- **C**: This copies a component. After pressing C key, the component you chose will be tied to the cursor and you can place it anywhere in the schematic by clicking once on the schematic editor.
- **Ctrl + H**: This is to create a Global label. After pressing Ctrl + H keys simultaneously, the global label will be tied to the cursor and you can place it anywhere in the schematic by clicking once on the schematic editor.
- **W**: This calls the place wire tool through which you can add components in your schematic.

13.2.2 B.2: Shortcut keys in PCB editor

- The shortcuts that can be used in the Pcbnew Layout Editor .Open the Pcbnew Layout editor and press Shift and ? keys simultaneously.
- **X**: This calls the Place Track tool.
- **R**: This rotates a component.
- **B**: Fill or Refill All Zones.

13.3 Appendix C: ERC errors

- **ErrType(1):** Duplicate sheet names within a given sheet. Review sheet names in hierarchy and remove duplicates.
- **ErrType(2):** Pin not connected and no No Connect Symbol. Check the pin and wire overlaps or place No connect symbol if pin should be left unconnected.
- **ErrType(3):** Pin connected to some others pins but no pin to drive it. This means there is a power input pin and there is no power connected to the pin. This is typically solved by adding a PWR FLAG symbol to the schematic.
- **ErrType(4):** Conflict problem between pins. Severity: warning. Two pins connected but their function needs complementary signals (for ex. input -i output). You can have many power input pins connected to power output but no two power output pins should be connected together.
- **ErrType(5):** Conflict Problem between pins, Severity: Error. This is because you can only have one output or power output on the same net.
- **ErrType(6):** Mismatch between hierarchical labels and pins sheets. There is a mismatch between hierarchical label and existing pin sheet, try to re-import hierarchical pins to replace wrong pin sheet.
- **ErrType(7):** A no connect symbol is connected to more than 1 pin. "No connect" symbol should be put at the end of the pin, and this pin should be left unconnected at all costs.
- **ErrType(8):** Global label not connected to any other global label. There is a global label which has no pair in other sheet(s).
- **ErrType(9):** Two labels are equal for case insensitive comparisons Review schematic labels to find possible duplicates, watch for similarity of large and small letters.
- **ErrType(10):** Two global labels are equal for case insensitive comparisons. Review global labels in hierarchy to find possible duplicates, watch for similarity of large and small letters.

13.4 Appendix D: Checks to be done before Simulation in NGHDL

1. VHDL filename should be in small letters without any space or special characters (Underscore is allowed).
2. Entity name, architecture declaration and the VHDL file name should match exactly.
3. Declaration of each port should be done on a new line. See **nghdl/Example/** for further reference.
4. Port declaration can be either **std_logic** or **std_logic_vector**. No other declarations are allowed.
5. All **in** ports should be declared before **out** ports.
6. Maximum number of output ports that a VHDL entity under simulation can have is 64, provided the port names are not too lengthy to overflow the buffer.
7. Be extremely careful while dealing with Arithmetic Operations. (See **nghdl/Example/counter/counter.vhdl** for further reference)
8. If structural style is used, then the main entity of your VHDL code which is to be simulated, should be declared first in the file with inclusion of libraries for subsequent declaration of each supporting entity. See **nghdl/Example/full_adder/full_adder_structural.vhdl** for further reference.
9. Do not use **sudo** or root permissions while working Mixed-Mode Simulation and eSim.
10. If there are more than one VHDL file to be uploaded, then do it **one-by-one**, as described below:
 - (a) Click on NGHDL button on eSim or type **nghdl/** in terminal. A new window will be opened.
 - (b) Upload your first VHDL file and wait for the process to be completed.
 - (c) Check if there are any Errors on the console. If possible, try to debug it and report your error and its solution to us. Otherwise, you can send the error to us. If there are no errors, upload your second model and repeat the steps mentioned above.
You can upload as many models as required.
11. **Do not upload two or more VHDL files simultaneously :**
Add **files** option allow you to use a smaller entity / subpart / submodule to support the main VHDL file. That is, a digital model will be generated corresponding to that file that has been browsed. The file that has been **added** to Nghdl upload window will only be placed along with the model under model's DUTghdl folder to support the model.
Hence, **browsing** one file and **adding** several files won't create that many number models, but only model will be created corresponding to the browsed file.
12. Maximum number of NGHDL models that can be simulated at once is restricted

to 512.

13. Next simulation should be started only after the completion of the previous/current simulation. No two simulations should be executed at once.
14. While providing parameters to the adc-dac bridges that correspond to any NGHDL model, make sure that the **rise and fall delays of ADC and DAC bridges** are comparable to the simulation time parameters passed. Some examples are given below:
 - (a) **Circuits involving both Analog and NGHDL Components** - If step time is 10 ms and simulation time is 200 ms, then DAC-ADC delays should be atleast 1 us.
 - (b) **Circuits involving only NGHDL Components** - If step time is 10 ms and simulation time is 200 ms, then DAC-ADC delays should be atleast 500 us.
 - (c) inverter subcircuit [INVCMOS] has a delay of 6 ms(can be changed by changing capacitor value inside the CMOS subcircuit). NGHDL model created, ADC and DAC bridges has rise and fall time 1 ns. You are simulating this circuit for 100 ms, it won't work. Increase the rise and fall delay for the ADC-DAC models from 1 nanosecond to 1 microsecond (1/1000th of the analog delay).

In general (**a thumb rule to follow**), delay value can be set to at least 1/500th part of the stop time.

15. If there is a need to use multiple instances of same NGHDL model in a given project and if even one of these instances need to have a different parameter value than the rest of the instances, then a separate NGHDL model needs to be generated with a different name.

13.5 Appendix E: Common Errors in NGHDL

Before concluding anything about NGHDL's working or about eSim's Mixed-Mode Simulation, do check the console for outputs and logs. Kindly see the following errors on User's end that can be rectified there itself :

13.5.1 NGHDL Upload Errors

- **Error while opening NGHDL. Please make sure NGHDL is installed :**

As the error indicates, NGHDL is not installed at all or there has been some error during installation which was not resolved effectively. However, if the installation was done correctly, then open a terminal and type :

```
$ sudo ln -s <your_path_to_nghdl>/nghdl/src/ngspice_ghdl.py /usr/local/bin/nghdl
```

Now type `nghdl` in terminal and check if the NGHDL Digital Model Creator window opens or not.

- **Error - select a *.vhdl file :**

This type of error can occur due to a variety of underlying user issues. Check terminal from which eSim is launched for more detailed errors. However, following is a list of common mistakes that a user may face :

- **Permission Denied** - Change the permission of `ngspice-nghdl` folder recursively to be used by all the users. To do so, open a terminal and type:

```
$ sudo chown $USER:$USER -R $HOME/ngspice-nghdl/
```

13.5.2 Simulation Related Errors

- **GHDL compilation error :**

The VHDL code itself is incorrect, as a result the corresponding model generated is incorrect and no simulation will be done. Kindly upload a correct VHDL code.

- **Warning : There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es) :**

Such warnings are difficult to find in xterm outputs. However, it indicates that there is some logical error in your VHDL code regarding the data types / arithmetic operations / type conversions, etc. Kindly upload a logically correct VHDL code.

- **Unknown model name <your_nghdl_model> - Ngspice :**

If this error occurs on xterm window while simulating with Ngspice, then check

whether the Ngspice engine used is of system built or that of the NGHDL. To check the same, follow the steps:

1. Open terminal and type : `$ whereis ngspice`
2. Go to the location where ngspice executable is found.
3. Now, check if this ngspice is a link to:
`ngspice-nghdl/install_dir/bin/ngspice`
4. If it is not a link, then uninstall the system's installed ngspice and create a link to the above mentioned path by typing the command in terminal as:
`$ sudo ln -s $HOME/ngspice-nghdl/install_dir/bin/ngspice/<previous_ngpsice_location>/ngspice`
5. If output of step 1 is empty, then run above command by replacing `<previous_ngpsice_location>` with `/usr/bin`

- **Unknown model name `<your_nghdl_model>` - KiCad-to-Ngspice :**

If this error occurs during KiCad-to-Ngspice conversion, then check whether the uploaded VHDL file had any Uppercase characters or any other special characters in its filename. Note that only lowercase characters and underscores are allowed.

- **Warning : component instance uut of xyz is not bound :**

This logical error is related to the VHDL code which is shown as a Warning and simulation plots may also appear. However, these plots are incorrect as the VHDL model itself is incorrect. Following are the examples that can cause this error:

- If a vhd1 file is saved as `dummycode.vhd1` and the entity and architecture are declared as for example, `codedummy` or `dummy` or something other than the name of the actual vhd1 file itself, one will get the above error.
- If structural style is being used and above error is seen, then kindly make the necessary changes by referring our example found at:
`nghdl/Example/full_adder/full_adder_structural.vhd1`

Kindly check with the GHDL documentation and online resources too are available regarding this GHDL error.

- **Warning : Too many analog/event-driven solution alternations**
Warning : Convergence problems at node (net-*).

.....

Transient solution failed -
doAnalyses: iteration limit reached :

As the error says itself that if too many analog components are connected to digital model due to which there can be many analog alternations (or if too many

events are generated rapidly due to which the convergence would fail for those models), then the initial conditions won't converge and the transient solution will fail. Follow these steps to resolve it:

1. Open the corresponding project's cir.out file (`*.cir.out`).
 2. Just below the **“.control”** statement and above the **“run”** statement, insert a new line.
 3. On this new line, type **“option noopalter”**.
 4. Save the file and exit.
 5. Run the simulation once again.
- **doAnalyses: TRAN : Timestep too small; time = ... , timestep = ... ; trouble with node ... run simulation(s) aborted :**

As the error says :

- Check if the time-step is too small as compared to the stop-time.
 - If the time-step is of the same order (scalable) as that of the stop-time, then check the delays of the adc-dac bridges and make them comparable to simulation stop-time.
 - If the delays are comparable, then check the parameters provided to the digital and analog models and set them appropriately.
- **chmod : changing permissions of ‘any_file’: Operation not permitted :**
This error, displayed on xterm by Ngspice, is similar to that of **Permission Denied** error. Kindly refer **section 13.4.1** for the same.

13.5.3 Model Deletion

If you want to delete a model from your file system or is deleted due to unavoidable circumstances, perform the following steps (to ensure consistency within the software) :

1. Delete the folders found at path :
 - `ngspice-nghdl/src/xspice/icm/ghdl/<your_model>/`
 - `ngspice-nghdl/release/src/xspice/icm/ghdl/<your_model>/`
2. Delete the name and description of that model from the files :
 - `ngspice-nghdl/src/xspice/icm/ghdl/modpath.lst`
 - `eSim.Nghdl.lib`

Realign the content of these files by removing any extra spaces or empty lines found between any two subsequent remaining model names after deletion.

3. Delete the file found at path :
eSim-version/src/modelParamXML/Nghdl/<your.model>.xml